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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions. SoCs combine a central

#### **Details**

Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I <sup>2</sup> C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	700MHz
Primary Attributes	FPGA - 462K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA, FC (40x40)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5asxbb5d6f40c6n">https://www.e-xfl.com/product-detail/intel/5asxbb5d6f40c6n</a>

Advantage	Supporting Feature
Lowest system cost	<ul style="list-style-type: none"> <li>Requires as few as four power supplies to operate</li> <li>Available in thermal composite flip chip ball-grid array (BGA) packaging</li> <li>Includes innovative features such as Configuration via Protocol (CvP), partial reconfiguration, and design security</li> </ul>

## Summary of Arria V Features

Table 2: Summary of Features for Arria V Devices

Feature	Description
Technology	<ul style="list-style-type: none"> <li>TSMC's 28-nm process technology:               <ul style="list-style-type: none"> <li>Arria V GX, GT, SX, and ST—28-nm low power (28LP) process</li> <li>Arria V GZ—28-nm high performance (28HP) process</li> </ul> </li> <li>Lowest static power in its class (less than 1.2 W for 500K logic elements (LEs) at 85°C junction under typical conditions)</li> <li>0.85 V, 1.1 V, or 1.15 V core nominal voltage</li> </ul>
Packaging	<ul style="list-style-type: none"> <li>Thermal composite flip chip BGA packaging</li> <li>Multiple device densities with identical package footprints for seamless migration between different device densities</li> <li>Leaded<sup>(1)</sup>, lead-free (Pb-free), and RoHS-compliant options</li> </ul>
High-performance FPGA fabric	<ul style="list-style-type: none"> <li>Enhanced 8-input ALM with four registers</li> <li>Improved routing architecture to reduce congestion and improve compilation time</li> </ul>
Internal memory blocks	<ul style="list-style-type: none"> <li>M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC) ( Arria V GX, GT, SX, and ST devices only)</li> <li>M20K—20-Kb memory blocks with hard ECC ( Arria V GZ devices only)</li> <li>Memory logic array block (MLAB)-640-bit distributed LUTRAM where you can use up to 50% of the ALMs as MLAB memory</li> </ul>

<sup>(1)</sup> Contact Altera for availability.

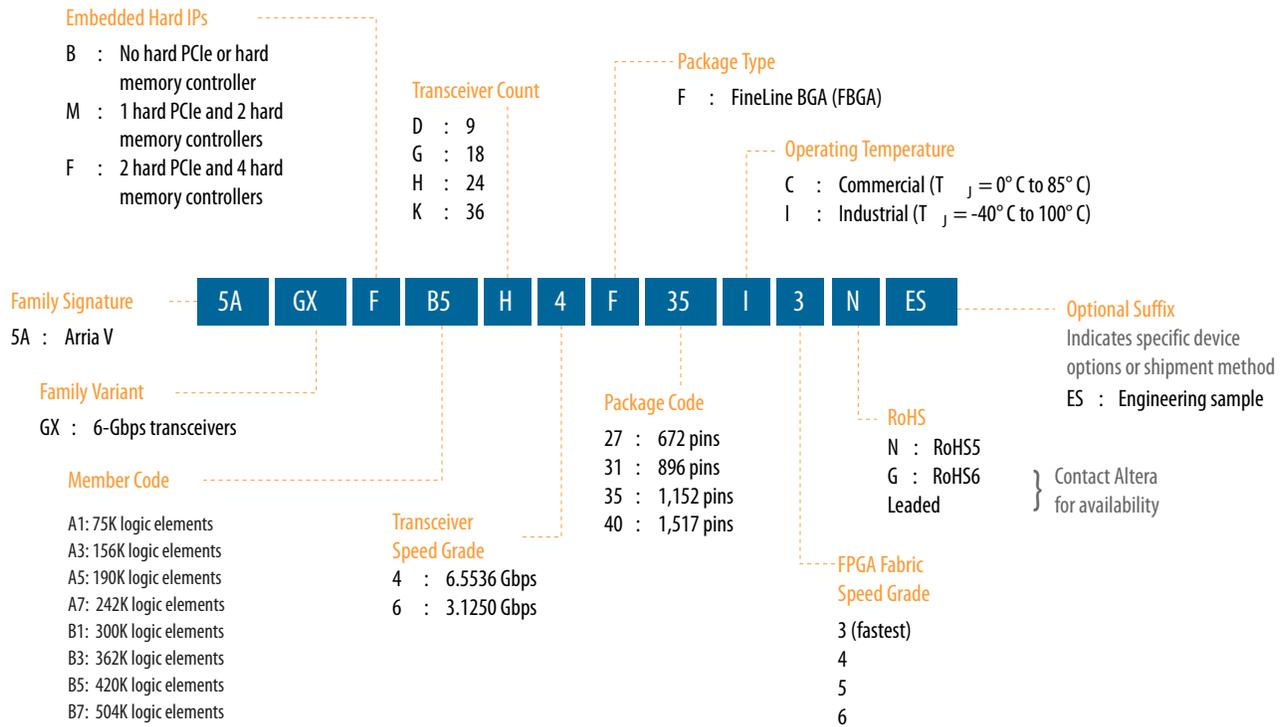
Feature	Description	
Embedded Hard IP blocks	Variable-precision DSP	<ul style="list-style-type: none"> <li>• Native support for up to four signal processing precision levels:               <ul style="list-style-type: none"> <li>• Three 9 x 9, two 18 x 18, or one 27 x 27 multiplier in the same variable-precision DSP block</li> <li>• One 36 x 36 multiplier using two variable-precision DSP blocks ( Arria V GZ devices only)</li> </ul> </li> <li>• 64-bit accumulator and cascade for systolic finite impulse responses (FIRs)</li> <li>• Embedded internal coefficient memory</li> <li>• Preadder/subtractor for improved efficiency</li> </ul>
	Memory controller ( Arria V GX, GT, SX, and ST only)	DDR3 and DDR2
	Embedded transceiver I/O	<ul style="list-style-type: none"> <li>• Custom implementation:               <ul style="list-style-type: none"> <li>• Arria V GX and SX devices—up to 6.5536 Gbps</li> <li>• Arria V GT and ST devices—up to 10.3125 Gbps</li> <li>• Arria V GZ devices—up to 12.5 Gbps</li> </ul> </li> <li>• PCI Express® (PCIe®) Gen2 (x1, x2, or x4) and Gen1 (x1, x2, x4, or x8) hard IP with multifunction support, endpoint, and root port</li> <li>• PCIe Gen3 (x1, x2, x4, or x8) support ( Arria V GZ only)</li> <li>• Gbps Ethernet (GbE) and XAUI physical coding sublayer (PCS)</li> <li>• Common Public Radio Interface (CPRI) PCS</li> <li>• Gigabit-capable passive optical network (GPON) PCS</li> <li>• 10-Gbps Ethernet (10GbE) PCS ( Arria V GZ only)</li> <li>• Serial RapidIO® (SRIO) PCS</li> <li>• Interlaken PCS ( Arria V GZ only)</li> </ul>
Clock networks	<ul style="list-style-type: none"> <li>• Up to 650 MHz global clock network</li> <li>• Global, quadrant, and peripheral clock networks</li> <li>• Clock networks that are not used can be powered down to reduce dynamic power</li> </ul>	
Phase-locked loops (PLLs)	<ul style="list-style-type: none"> <li>• High-resolution fractional PLLs</li> <li>• Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB)</li> <li>• Integer mode and fractional mode</li> <li>• LC oscillator ATX transmitter PLLs ( Arria V GZ only)</li> </ul>	

Feature	Description
FPGA General-purpose I/Os (GPIOs)	<ul style="list-style-type: none"> <li>• 1.6 Gbps LVDS receiver and transmitter</li> <li>• 800 MHz/1.6 Gbps external memory interface</li> <li>• On-chip termination (OCT)</li> <li>• 3.3 V support <sup>(2)</sup></li> </ul>
External Memory Interface	<p>Memory interfaces with low latency:</p> <ul style="list-style-type: none"> <li>• Hard memory controller-up to 1.066 Gbps</li> <li>• Soft memory controller-up to 1.6 Gbps</li> </ul>
Low-power high-speed serial interface	<ul style="list-style-type: none"> <li>• 600 Mbps to 12.5 Gbps integrated transceiver speed</li> <li>• Less than 105 mW per channel at 6 Gbps, less than 165 mW per channel at 10 Gbps, and less than 170 mW per channel at 12.5 Gbps</li> <li>• Transmit pre-emphasis and receiver equalization</li> <li>• Dynamic partial reconfiguration of individual channels</li> <li>• Physical medium attachment (PMA) with soft PCS that supports 9.8304 Gbps CPRI ( Arria V GT and ST only)</li> <li>• PMA with hard PCS that supports up to 9.8 Gbps CPRI ( Arria V GZ only)</li> <li>• Hard PCS that supports 10GBASE-R and 10GBASE-KR ( Arria V GZ only)</li> </ul>
HPS ( Arria V SX and ST devices only)	<ul style="list-style-type: none"> <li>• Dual-core ARM Cortex-A9 MPCore processor—up to 1.05 GHz maximum frequency with support for symmetric and asymmetric multiprocessing</li> <li>• Interface peripherals—10/100/1000 Ethernet media access control (EMAC), USB 2.0 On-The-GO (OTG) controller, quad serial peripheral interface (QSPI) flash controller, NAND flash controller, Secure Digital/MultiMediaCard (SD/MMC) controller, UART, serial peripheral interface (SPI), I2C interface, and up to 85 HPS GPIO interfaces</li> <li>• System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers</li> <li>• On-chip RAM and boot ROM</li> <li>• HPS-FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa</li> <li>• FPGA-to-HPS SDRAM controller subsystem—provides a configurable interface to the multiport front end (MPFE) of the HPS SDRAM controller</li> <li>• ARM CoreSight™ JTAG debug access port, trace port, and on-chip trace storage</li> </ul>

<sup>(2)</sup> Arria V GZ devices support 3.3 V with a 3.0 V  $V_{CCIO}$ .

## Available Options

Figure 1: Sample Ordering Code and Available Options for Arria V GX Devices



## Maximum Resources

Table 4: Maximum Resource Counts for Arria V GX Devices

Resource	Member Code								
	A1	A3	A5	A7	B1	B3	B5	B7	
Logic Elements (LE) (K)	75	156	190	242	300	362	420	504	
ALM	28,302	58,900	71,698	91,680	113,208	136,880	158,491	190,240	
Register	113,208	235,600	286,792	366,720	452,832	547,520	633,964	760,960	
Memory (Kb)	M10K	8,000	10,510	11,800	13,660	15,100	17,260	20,540	24,140
	MLAB	463	961	1,173	1,448	1,852	2,098	2,532	2,906
Variable-precision DSP Block	240	396	600	800	920	1,045	1,092	1,156	
18 x 18 Multiplier	480	792	1,200	1,600	1,840	2,090	2,184	2,312	
PLL	10	10	12	12	12	12	16	16	

Resource	Member Code							
	A1	A3	A5	A7	B1	B3	B5	B7
6 Gbps Transceiver	9	9	24	24	24	24	36	36
GPIO <sup>(3)</sup>	416	416	544	544	704	704	704	704
LVDS	Transmitter	67	67	120	120	160	160	160
	Receiver	80	80	136	136	176	176	176
PCIe Hard IP Block	1	1	2	2	2	2	2	2
Hard Memory Controller	2	2	4	4	4	4	4	4

**Related Information****[High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook](#)**

Provides the number of LVDS channels in each device package.

**Package Plan****Table 5: Package Plan for Arria V GX Devices**

Member Code	F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)		F1517 (40 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
A1	336	9	416	9	—	—	—	—
A3	336	9	416	9	—	—	—	—
A5	336	9	384	18	544	24	—	—
A7	336	9	384	18	544	24	—	—
B1	—	—	384	18	544	24	704	24
B3	—	—	384	18	544	24	704	24
B5	—	—	—	—	544	24	704	36
B7	—	—	—	—	544	24	704	36

**Arria V GT**

This section provides the available options, maximum resource counts, and package plan for the Arria V GT devices.

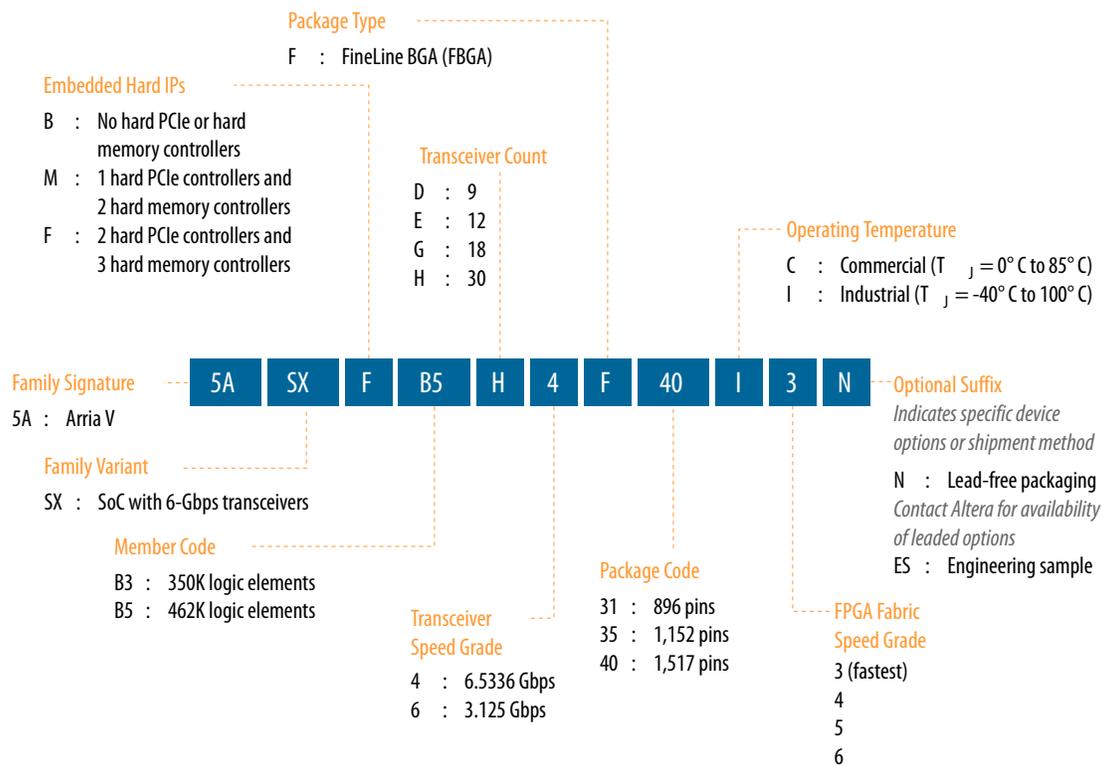
<sup>(3)</sup> The number of GPIOs does not include transceiver I/Os. In the Quartus® Prime software, the number of user I/Os includes transceiver I/Os.

**Related Information****Altera Product Selector**

Provides the latest information about Altera products.

**Available Options****Figure 4: Sample Ordering Code and Available Options for Arria V SX Devices**

The –3 FPGA fabric speed grade is available only for industrial temperature devices.

**Maximum Resources****Table 10: Maximum Resource Counts for Arria V SX Devices**

Resource	Member Code	
	B3	B5
Logic Elements (LE) (K)	350	462
ALM	132,075	174,340
Register	528,300	697,360
Memory (Kb)	M10K	22,820
	MLAB	2,658
Variable-precision DSP Block	809	1,090
18 x 18 Multiplier	1,618	2,180

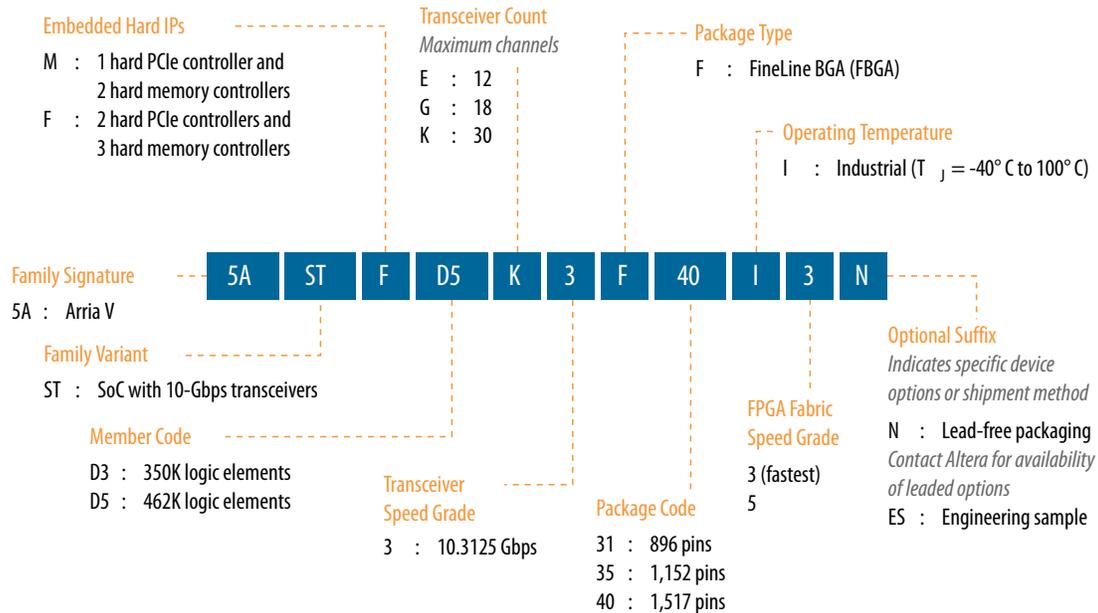
## Related Information

[Altera Product Selector](#)

Provides the latest information about Altera products.

## Available Options

Figure 5: Sample Ordering Code and Available Options for Arria V ST Devices



## Maximum Resources

Table 12: Maximum Resource Counts for Arria V ST Devices

Resource	Member Code	
	D3	D5
Logic Elements (LE) (K)	350	462
ALM	132,075	174,340
Register	528,300	697,360
Memory (Kb)	M10K	22,820
	MLAB	2,658
Variable-precision DSP Block	809	1,090
18 x 18 Multiplier	1,618	2,180
FPGA PLL	14	14
HPS PLL	3	3
Transceiver	6-Gbps	30
	10-Gbps <sup>(9)</sup>	16

Resource		Member Code	
		D3	D5
FPGA GPIO <sup>(10)</sup>		540	540
HPS I/O		208	208
LVDS	Transmitter	120	120
	Receiver	136	136
PCIe Hard IP Block		2	2
FPGA Hard Memory Controller		3	3
HPS Hard Memory Controller		1	1
ARM Cortex-A9 MPCore Processor		Dual-core	Dual-core

**Related Information**

- [High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook](#)  
Provides the number of LVDS channels in each device package.
- [Transceiver Architecture in Arria V Devices](#)  
Describes 10 Gbps channels usage conditions and SFF-8431 compliance requirements.

**Package Plan**

**Table 13: Package Plan for Arria V ST Devices**

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	F896 (31 mm)				F1152 (35 mm)				F1517 (40 mm)			
	FPGA GPIO	HPS I/O	XCVR		FPGA GPIO	HPS I/O	XCVR		FPGA GPIO	HPS I/O	XCVR	
			6 Gbps	10 Gbps			6 Gbps	10 Gbps			6 Gbps	10 Gbps
	D3	250	208	12	6	385	208	18	8	540	208	30
D5	250	208	12	6	385	208	18	8	540	208	30	16

<sup>(9)</sup> Chip-to-chip connections only. For 10 Gbps channel usage conditions, refer to the Transceiver Architecture in Arria V Devices chapter.

<sup>(10)</sup> The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

## I/O Vertical Migration for Arria V Devices

**Figure 6: Vertical Migration Capability Across Arria V Device Packages and Densities**

The arrows indicate the vertical migration paths. Some packages have several migration paths. The devices included in each vertical migration path are shaded. You can also migrate your design across device densities in the same package option if the devices have the same dedicated pins, configuration pins, and power pins.

Variant	Member Code	Package				
		F672	F780	F896	F 1152	F1517
Arria V GX	A1					
	A3					
	A5					
	A7					
	B1					
	B3					
	B5					
	B7					
Arria V GT	C3					
	C7					
	D3					
	D7					
Arria V GZ	E1					
	E3					
	E5					
	E7					
Arria V SX	B3					
	B5					
Arria V ST	D3					
	D5					

You can achieve the vertical migration shaded in red if you use only up to 320 GPIOs, up to nine 6 Gbps transceiver channels, and up to four 10 Gbps transceiver (for Arria V GT devices). This migration path is not shown in the Quartus Prime software Pin Migration View.

**Note:** To verify the pin migration compatibility, use the Pin Migration View window in the Quartus Prime software Pin Planner.

**Note:** Except for Arria V GX A5 and A7, and Arria V GT C7 devices, all other Arria V GX and GT devices require a specific power-up sequence. If you plan to migrate your design from Arria V GX A5 and A7, and Arria V GT C7 devices to other Arria V devices, your design must adhere to the same required power-up sequence.

## Variable-Precision DSP Block

Arria V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18, 27 x 27, and 36 x 36 bits natively
- A 64-bit accumulator
- Double accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Dynamic coefficients
- 18-bit internal coefficient register banks
- Enhanced independent multiplier operation
- Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Quartus Prime design software

**Table 14: Variable-Precision DSP Block Configurations for Arria V Devices**

Usage Example	Multiplier Size (Bit)	DSP Block Resource
Low precision fixed point for video applications	Three 9 x 9	1
Medium precision fixed point in FIR filters	Two 18 x 18	1
FIR filters	Two 18 x 18 with accumulate	1
Single-precision floating-point implementations	One 27 x 27	1
Very high precision fixed point implementations	One 36 x 36	2

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 18, or one 27 x 27 multipliers. Using two DSP block resources, you can also configure a 36 x 36 multiplier for high-precision applications. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

**Table 15: Number of Multipliers in Arria V Devices**

The table lists the variable-precision DSP resources by bit precision for each Arria V device.

Variant	Member Code	Variable-precision DSP Block	Independent Input and Output Multiplications Operator				18 x 18 Multiplier Adder Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			9 x 9 Multiplier	18 x 18 Multiplier	27 x 27 Multiplier	36 x 36 Multiplier		
Arria V GX	A1	240	720	480	240	—	240	240
	A3	396	1,188	792	396	—	396	396
	A5	600	1,800	1,200	600	—	600	600
	A7	800	2,400	1,600	800	—	800	800
	B1	920	2,760	1,840	920	—	920	920
	B3	1,045	3,135	2,090	1,045	—	1,045	1,045
	B5	1,092	3,276	2,184	1,092	—	1,092	1,092
	B7	1,156	3,468	2,312	1,156	—	1,156	1,156
Arria V GT	C3	396	1,188	792	396	—	396	396
	C7	800	2,400	1,600	800	—	800	800
	D3	1,045	3,135	2,090	1,045	—	1,045	1,045
	D7	1,156	3,468	2,312	1,156	—	1,156	1,156
Arria V GZ	E1	800	2,400	1,600	800	400	800	800
	E3	1,044	3,132	2,088	1,044	522	1,044	1,044
	E5	1,092	3,276	2,184	1,092	546	1,092	1,092
	E7	1,139	3,417	2,278	1,139	569	1,139	1,139
Arria V SX	B3	809	2,427	1,618	809	—	809	809
	B5	1,090	3,270	2,180	1,090	—	1,090	1,090
Arria V ST	D3	809	2,427	1,618	809	—	809	809
	D5	1,090	3,270	2,180	1,090	—	1,090	1,090

## Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.

## External Memory Performance

Table 18: External Memory Interface Performance in Arria V Devices

Interface	Voltage (V)	Hard Controller (MHz)	Soft Controller (MHz)	
		Arria V GX, GT, SX, and ST	Arria V GX, GT, SX, and ST	Arria V GZ
DDR3 SDRAM	1.5	533	667	800
	1.35	533	600	800
DDR2 SDRAM	1.8	400	400	400
LPDDR2 SDRAM	1.2	—	400	—
RLDRAM 3	1.2	—	—	667
RLDRAM II	1.8	—	400	533
	1.5	—	400	533
QDR II+ SRAM	1.8	—	400	500
	1.5	—	400	500
QDR II SRAM	1.8	—	400	333
	1.5	—	400	333
DDR II+ SRAM <sup>(12)</sup>	1.8	—	400	—
	1.5	—	400	—

### Related Information

#### [External Memory Interface Spec Estimator](#)

For the latest information and to estimate the external memory system performance specification, use Altera's External Memory Interface Spec Estimator tool.

## HPS External Memory Performance

Table 19: HPS External Memory Interface Performance

The hard processor system (HPS) is available in Arria V SoC devices only.

Interface	Voltage (V)	HPS Hard Controller (MHz)
DDR3 SDRAM	1.5	533
	1.35	533
LPDDR2 SDRAM	1.2	333

<sup>(12)</sup> Not available as Altera® IP.

### Related Information

#### [External Memory Interface Spec Estimator](#)

For the latest information and to estimate the external memory system performance specification, use Altera's External Memory Interface Spec Estimator tool.

## Low-Power Serial Transceivers

Arria V devices deliver the industry's lowest power consumption per transceiver channel:

- 12.5 Gbps transceivers at less than 170 mW
- 10 Gbps transceivers at less than 165 mW
- 6 Gbps transceivers at less than 105 mW

Arria V transceivers are designed to be compliant with a wide range of protocols and data rates.

## Transceiver Channels

The transceivers are positioned on the left and right outer edges of the device. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks.

The following figures are graphical representations of a top view of the silicon die, which corresponds to a reverse view for flip chip packages. Different Arria V devices may have different floorplans than the ones shown in the figures.

Features	Capability
PLL-based clock recovery	Superior jitter tolerance
Programmable serializer and deserializer (SERDES)	Flexible SERDES width
Equalization and pre-emphasis	<ul style="list-style-type: none"> <li>• Arria V GX, GT, SX, and ST devices—Up to 14.37 dB of pre-emphasis and up to 4.7 dB of equalization</li> <li>• Arria V GZ devices—4-tap pre-emphasis and de-emphasis</li> </ul>
Ring oscillator transmit PLLs	611 Mbps to 10.3125 Gbps
LC oscillator ATX transmit PLLs (Arria V GZ devices only)	600 Mbps to 12.5 Gbps
Input reference clock range	27 MHz to 710 MHz
Transceiver dynamic reconfiguration	Allows the reconfiguration of a single channel without affecting the operation of other channels

## PCS Features

The Arria V core logic connects to the PCS through an 8, 10, 16, 20, 32, 40, 64, 66, or 67 bit interface, depending on the transceiver data rate and protocol. Arria V devices contain PCS hard IP to support PCIe Gen1, Gen2, and Gen3, GbE, Serial RapidIO (SRIO), GPON, and CPRI.

All other standard and proprietary protocols within the following speed ranges are also supported:

- 611 Mbps to 6.5536 Gbps—supported through the custom double-width mode (up to 6.5536 Gbps) and custom single-width mode (up to 3.75 Gbps) of the transceiver PCS hard IP.
- 6.5536 Gbps to 10.3125 Gbps—supported through dedicated 80 or 64 bit interface that bypass the PCS hard IP and connects the PMA directly to the core logic. In Arria V GZ, this is supported in the transceiver PCS hard IP.

**Table 21: Transceiver PCS Features for Arria V GX, GT, ST, and SX Devices**

PCS Support <sup>(13)</sup>	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
Custom single- and double-width modes	0.611 to ~6.5536	<ul style="list-style-type: none"> <li>• Phase compensation FIFO</li> <li>• Byte serializer</li> <li>• 8B/10B encoder</li> </ul>	<ul style="list-style-type: none"> <li>• Word aligner</li> <li>• 8B/10B decoder</li> <li>• Byte deserializer</li> <li>• Phase compensation FIFO</li> </ul>
SRIO	1.25 to 6.25		
Serial ATA	1.5, 3.0, 6.0		

<sup>(13)</sup> Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through the soft PCS.

PCS Support <sup>(13)</sup>	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
PCIe Gen1 (x1, x2, x4, x8)	2.5 and 5.0	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> <li>8B/10B encoder</li> <li>PIPE 2.0 interface to the core logic</li> </ul>	<ul style="list-style-type: none"> <li>Word aligner</li> <li>8B/10B decoder</li> <li>Byte deserializer</li> <li>Phase compensation FIFO</li> <li>Rate match FIFO</li> <li>PIPE 2.0 interface to the core logic</li> </ul>
PCIe Gen2 <sup>(14)</sup> (x1, x2, x4)			
GbE	1.25	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> <li>8B/10B encoder</li> </ul>	<ul style="list-style-type: none"> <li>Word aligner</li> <li>8B/10B decoder</li> <li>Byte deserializer</li> <li>Phase compensation FIFO</li> <li>Rate match FIFO</li> </ul>
XAUI <sup>(15)</sup>	3.125	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> <li>8B/10B encoder</li> <li>XAUI state machine for bonding four channels</li> </ul>	<ul style="list-style-type: none"> <li>Word aligner</li> <li>8B/10B decoder</li> <li>Byte deserializer</li> <li>Phase compensation FIFO</li> <li>XAUI state machine for realigning four channels</li> <li>Deskew FIFO circuitry</li> </ul>
SDI	0.27 <sup>(16)</sup> , 1.485, 2.97	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> </ul>	<ul style="list-style-type: none"> <li>Byte deserializer</li> <li>Phase compensation FIFO</li> </ul>
GPON <sup>(17)</sup>	1.25 and 2.5		
CPRI <sup>(18)</sup>	0.6144 to 6.144	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> <li>8B/10B encoder</li> <li>TX deterministic latency</li> </ul>	<ul style="list-style-type: none"> <li>Word aligner</li> <li>8B/10B decoder</li> <li>Byte deserializer</li> <li>Phase compensation FIFO</li> <li>RX deterministic latency</li> </ul>

<sup>(13)</sup> Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through the soft PCS.

<sup>(14)</sup> PCIe Gen2 is supported only through the PCIe hard IP.

<sup>(15)</sup> XAUI is supported through the soft PCS.

<sup>(16)</sup> The 0.27 Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

<sup>(17)</sup> The GPON standard does not support burst mode.

<sup>(18)</sup> CPRI data rates above 6.5536 Gbps, such as 9.8304 Gbps, are supported through the soft PCS.

## Partial Reconfiguration

**Note:** Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

Partial reconfiguration allows you to reconfigure part of the device while other sections of the device remain operational. This capability is important in systems with critical uptime requirements because it allows you to make updates or adjust functionality without disrupting services.

Apart from lowering cost and power consumption, partial reconfiguration increases the effective logic density of the device because placing device functions that do not operate simultaneously is not necessary. Instead, you can store these functions in external memory and load them whenever the functions are required. This capability reduces the size of the device because it allows multiple applications on a single device—saving the board space and reducing the power consumption.

Altera simplifies the time-intensive task of partial reconfiguration by building this capability on top of the proven incremental compile and design flow in the Quartus Prime design software. With the Altera solution, you do not need to know all the intricate device architecture details to perform a partial reconfiguration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable simultaneous partial reconfiguration of both the device core and transceivers.

## Enhanced Configuration and Configuration via Protocol

**Table 23: Configuration Modes and Features of Arria V Devices**

Arria V devices support 1.8 V, 2.5 V, 3.0 V, and 3.3 V<sup>(19)</sup> programming voltages and several configuration modes.

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompression	Design Security	Partial Reconfiguration <sup>(20)</sup>	Remote System Update
AS through the EPCS and EPCQ serial configuration device	1 bit, 4 bits	100	—	Yes	Yes	—	Yes
PS through CPLD or external microcontroller	1 bit	125	125	Yes	Yes	—	—

<sup>(19)</sup> Arria V GZ does not support 3.3 V.

<sup>(20)</sup> Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompression	Design Security	Partial Reconfiguration <sup>(20)</sup>	Remote System Update
FPP	8 bits	125	—	Yes	Yes	—	Parallel flash loader
	16 bits	125	—	Yes	Yes	Yes <sup>(21)</sup>	
	32 bits <sup>(22)</sup>	100	—	Yes	Yes	—	
CvP (PCIe)	x1, x2, x4, and x8 lanes	—	—	Yes	Yes	Yes	—
JTAG	1 bit	33	33	—	—	—	—
Configuration via HPS	16 bits	125	—	Yes	Yes	Yes <sup>(21)</sup>	Parallel flash loader
	32 bits	100	—	Yes	Yes	—	

Instead of using an external flash or ROM, you can configure the Arria V devices through PCIe using CvP. The CvP mode offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. The Arria V CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

**Note:** Although Arria V GZ devices support PCIe Gen3, you can use only PCIe Gen1 and PCIe Gen2 for CvP configuration scheme.

#### Related Information

#### [Configuration via Protocol \(CvP\) Implementation in Altera FPGAs User Guide](#)

Provides more information about CvP.

## Power Management

Leveraging the FPGA architectural features, process technology advancements, and transceivers that are designed for power efficiency, the Arria V devices consume less power than previous generation Arria V FPGAs:

- Total device core power consumption—less by up to 50%.
- Transceiver channel power consumption—less by up to 50%.

Additionally, Arria V devices contain several hard IP blocks, including PCIe Gen1, Gen2, and Gen3, GbE, SRIO, GPON, and CPRI protocols, that reduce logic resources and deliver substantial power savings of up to 25% less power than equivalent soft implementations.

<sup>(20)</sup> Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

<sup>(21)</sup> Supported at a maximum clock rate of 62.5 MHz.

<sup>(22)</sup> Arria V GZ only

## Document Revision History

Date	Version	Changes
December 2015	2015.12.21	<ul style="list-style-type: none"> <li>Updated RoHS and optional suffix information in sample ordering code and available options diagrams for Arria V GX and GT devices.</li> <li>Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.</li> </ul>
January 2015	2015.01.23	<ul style="list-style-type: none"> <li>Updated package dimension for Arria V GZ H780 package from 29 mm to 33 mm.</li> <li>Updated dual-core ARM Cortex-A9 MPCore processor maximum frequency from 800 MHz to 1.05 GHz.</li> </ul>
December 2013	2013.12.26	<ul style="list-style-type: none"> <li>10-Gbps Ethernet (10GbE) PCS and Interlaken PCS are for Arria V GZ only.</li> <li>Removed "Preliminary" texts from Ordering Code figures, Maximum Resources, Package Plan and I/O Vertical Migration tables.</li> <li>Added link to <a href="#">Altera Product Selector</a> for each device variant.</li> <li>Added leaded package options.</li> <li>Removed the note "The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs." for all PLLs in the Maximum Resource Counts table.</li> <li>Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F896 package from 170 to 250.</li> <li>Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F1152 package from 350 to 385.</li> <li>Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F1517 package from 528 to 540.</li> <li>Corrected LVDS Transmitter for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 devices from 121 to 120.</li> <li>Added links to Altera's <a href="#">External Memory Spec Estimator</a> tool to the topics listing the external memory interface performance.</li> <li>Added x2 for PCIe Gen3, Gen 2, and Gen 1.</li> </ul>
August 2013	2013.08.19	<ul style="list-style-type: none"> <li>Removed the note about the PCIe hard IP on the right side of the device in the F896 package of the Arria V GX variant. These devices do not have PCIe hard IP on the right side.</li> <li>Added transceiver speed grade 6 to the available options of the Arria V SX variant.</li> <li>Corrected the maximum LVDS transmitter channel counts for the Arria V GX A1 and A3 devices from 68 to 67.</li> <li>Corrected the maximum FPGA GPIO count for Arria V ST D5 devices from 540 to 528.</li> </ul>

Date	Version	Changes
June 2013	2013.06.03	<ul style="list-style-type: none"> <li>Removed statements about contacting Altera for SFF-8431 compliance requirements. Refer to the <a href="#">Transceiver Architecture in Arria V Devices</a> chapter for the requirements.</li> </ul>
May 2013	2013.05.06	<ul style="list-style-type: none"> <li>Moved all links to the Related Information section of respective topics for easy reference.</li> <li>Added link to the known document issues in the Knowledge Base.</li> <li>Updated the available options, maximum resource counts, and per package information for the Arria V SX and ST device variants.</li> <li>Updated the variable DSP multipliers counts for the Arria V SX and ST device variants.</li> <li>Clarified that partial reconfiguration is an advanced feature. Contact Altera for support of the feature.</li> <li>Added footnote to clarify that MLAB 64 bits depth is available only for Arria V GZ devices.</li> <li>Updated description about power-up sequence requirement for device migration to improve clarity.</li> </ul>
January 2013	2013.01.11	<ul style="list-style-type: none"> <li>Added the L optional suffix to the Arria V GZ ordering code for the – I3 speed grade.</li> <li>Added a note about the power-up sequence requirement if you plan to migrate your design from the Arria V GX A5 and A7, and Arria V GT C7 devices to other Arria V devices.</li> </ul>
November 2012	2012.11.19	<ul style="list-style-type: none"> <li>Updated the summary of features.</li> <li>Updated Arria V GZ information regarding 3.3 V I/O support.</li> <li>Removed Arria V GZ engineering sample ordering code.</li> <li>Updated the maximum resource counts for Arria V GX and GZ.</li> <li>Updated Arria V ST ordering codes for transceiver count.</li> <li>Updated transceiver counts for Arria V ST packages.</li> <li>Added simplified floorplan diagrams for Arria V GZ, SX, and ST.</li> <li>Added FPP x32 configuration mode for Arria V GZ only.</li> <li>Updated CvP (PCIe) remote system update support information.</li> <li>Added HPS external memory performance information.</li> <li>Updated template.</li> </ul>
October 2012	3.0	<ul style="list-style-type: none"> <li>Added Arria V GZ information.</li> <li>Updated Table 1, Table 2, Table 3, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, and Table 21.</li> <li>Added the “Arria V GZ” section.</li> <li>Added Table 8, Table 9 and Table 22.</li> </ul>

Date	Version	Changes
July 2012	2.1	<ul style="list-style-type: none"> <li>Added -I3 speed grade to Figure 1 for Arria V GX devices.</li> <li>Updated the 6-Gbps transceiver speed from 6.553 Gbps to 6.5536 Gbps in Figure 3 and Figure 1.</li> </ul>
June 2012	2.0	<ul style="list-style-type: none"> <li>Restructured the document.</li> <li>Added the “Embedded Memory Capacity” and “Embedded Memory Configurations” sections.</li> <li>Added Table 1, Table 3, Table 12, Table 15, and Table 16.</li> <li>Updated Table 2, Table 4, Table 5, Table 6, Table 7, Table 8, Table 9, Table 10, Table 11, Table 13, Table 14, and Table 19.</li> <li>Updated Figure 1, Figure 2, Figure 3, Figure 4, and Figure 8.</li> <li>Updated the “FPGA Configuration and Processor Booting” and “Hardware and Software Development” sections.</li> <li>Text edits throughout the document.</li> </ul>
February 2012	1.3	<ul style="list-style-type: none"> <li>Updated Table 1–7 and Table 1–8.</li> <li>Updated Figure 1–9 and Figure 1–10.</li> <li>Minor text edits.</li> </ul>
December 2011	1.2	Minor text edits.
November 2011	1.1	<ul style="list-style-type: none"> <li>Updated Table 1–1, Table 1–2, Table 1–3, Table 1–4, Table 1–6, Table 1–7, Table 1–9, and Table 1–10.</li> <li>Added “SoC FPGA with HPS” section.</li> <li>Updated “Clock Networks and PLL Clock Sources” and “Ordering Information” sections.</li> <li>Updated Figure 1–5.</li> <li>Added Figure 1–6.</li> <li>Minor text edits.</li> </ul>
August 2011	1.0	Initial release.