E·XFL

Intel - 5ASXFB3G4F35C5N Datasheet



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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions. SoCs combine a central

Details

Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore [™] with CoreSight [™]
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	800MHz
Primary Attributes	FPGA - 350K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA, FC (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5asxfb3g4f35c5n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Advantage	Supporting Feature
Lowest system cost	 Requires as few as four power supplies to operate Available in thermal composite flip chip ball-grid array (BGA) packaging Includes innovative features such as Configuration via Protocol (CvP), partial reconfiguration, and design security

Summary of Arria V Features

Table 2: Summary of Features for Arria V Devices

Feature	Description
Technology	TSMC's 28-nm process technology:
	 Arria V GX, GT, SX, and ST—28-nm low power (28LP) process Arria V GZ—28-nm high performance (28HP) process Lowest static power in its class (less than 1.2 W for 500K logic elements (LEs) at
	 0.85 V, 1.1 V, or 1.15 V core nominal voltage
Packaging	 Thermal composite flip chip BGA packaging Multiple device densities with identical package footprints for seamless migration between different device densities Leaded⁽¹⁾, lead-free (Pb-free), and RoHS-compliant options
High-performance FPGA fabric	 Enhanced 8-input ALM with four registers Improved routing architecture to reduce congestion and improve compilation time
Internal memory blocks	 M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC) (Arria V GX, GT, SX, and ST devices only) M20K—20-Kb memory blocks with hard ECC (Arria V GZ devices only) Memory logic array block (MLAB)-640-bit distributed LUTRAM where you can use up to 50% of the ALMs as MLAB memory





⁽¹⁾ Contact Altera for availability.

Available Options

Figure 1: Sample Ordering Code and Available Options for Arria V GX Devices



Maximum Resources

Table 4: Maximum Resource Counts for Arria V GX Devices

Pasaurea		Member Code							
neso	urce	A1	A3	A5	A7	B1	B3	B5	Β7
Logic I (LE) (I	Elements K)	75	156	190	242	300	362	420	504
ALM	ALM		58,900	71,698	91,680	113,208	136,880	158,491	190,240
Registe	er	113,208	235,600	286,792	366,720	452,832	547,520	633,964	760,960
Mem	M10K	8,000	10,510	11,800	13,660	15,100	17,260	20,540	24,140
ory (Kb)	MLAB	463	961	1,173	1,448	1,852	2,098	2,532	2,906
Variab precisi Block	le- on DSP	240	396	600	800	920	1,045	1,092	1,156
18 x 18 Multip	3 llier	480	792	1,200	1,600	1,840	2,090	2,184	2,312
PLL		10	10	12	12	12	12	16	16

Arria V Device Overview



Pesource		Member Code					
Neso	uice	C3	С7	D3	D7		
Transceiver	6 Gbps ⁽⁴⁾	3 (9)	6 (24)	6 (24)	6 (36)		
Transcerver	10 Gbps ⁽⁵⁾	4	12	12	20		
GPIO ⁽⁶⁾		416	544	704	704		
LVDS	Transmitter	68	120	160	160		
LVDS	Receiver	80	136	176	176		
PCIe Hard IP Block		1	2	2	2		
Hard Memory Controller		2	4	4	4		

Related Information

High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook

Provides the number of LVDS channels in each device package.

• **Transceiver Architecture in Arria V Devices** Describes 10 Gbps channels usage conditions and SFF-8431 compliance requirements.

Package Plan

Memb		F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)		F1517 (40 mm)		7 n)		
er Code		ХС	VR		хс	VR		ХС	VR		2	KCVR
	GPIO	6- Gbps	10- Gbps	GPIO	6- Gbps	10- Gbps	GPIO	6- Gbps	10- Gbps	GPIO	6- Gbps	10-Gbps
C3	336	3 (9)	4	416	3 (9)	4	_	_	_	_		
C7				384	6 (18)	8	544	6 (24)	12			
D3			—	384	6 (18)	8	544	6 (24)	12	704	6 (24)	12
D7					_		544	6 (24)	12	704	6 (36)	20

Table 7: Package Plan for Arria V GT Devices

The 6-Gbps transceiver counts are for dedicated 6-Gbps channels. You can also configure any pair of 10-Gbps channels as three 6-Gbps channels—the total number of 6-Gbps channels are shown in brackets. For example, you can also configure the Arria V GT D7 device in the F1517 package with nine 6-Gbps



⁽⁴⁾ The 6 Gbps transceiver counts are for dedicated 6-Gbps channels. You can also configure any pair of 10 Gbps channels as three 6 Gbps channels-the total number of 6 Gbps channels are shown in brackets.

⁽⁵⁾ Chip-to-chip connections only. For 10 Gbps channel usage conditions, refer to the Transceiver Architecture in Arria V Devices chapter.

⁽⁶⁾ The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

10 Arria V GZ

and eighteen 10-Gbps, twelve 6-Gbps and sixteen 10-Gbps, fifteen 6-Gbps and fourteen 10-Gbps, or up to thirty-six 6-Gbps with no 10-Gbps channels.

Arria V GZ

This section provides the available options, maximum resource counts, and package plan for the Arria V GZ devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

Related Information

Altera Product Selector

Provides the latest information about Altera products.

Available Options



Figure 3: Sample Ordering Code and Available Options for Arria V GZ Devices

Maximum Resources

Table 8: Maximum Resource Counts for Arria V GZ Devices

Pasource	Member Code					
Nesource	E1	E3	E5	E7		
Logic Elements (LE) (K)	220	360	400	450		
ALM	83,020	135,840	150,960	169,800		
Register	332,080	543,360	603,840	679,200		

Arria V Device Overview



12 Available Options

Related Information

Altera Product Selector

Provides the latest information about Altera products.

Available Options

Figure 4: Sample Ordering Code and Available Options for Arria V SX Devices

The –3 FPGA fabric speed grade is available only for industrial temperature devices.



Maximum Resources

Table 10: Maximum Resource Counts for Arria V SX Devices

Poso		Member Code			
nesu	uice	B3	B5		
Logic Elements (LE)	(K)	350	462		
ALM		132,075	174,340		
Register	Register		697,360		
Memory (Kb)	M10K	17,290	22,820		
Welliory (RD)	MLAB	2,014	2,658		
Variable-precision DSP Block		809	1,090		
18 x 18 Multiplier		1,618	2,180		

Arria V Device Overview



Poso		Member Code			
Nesc		B3	B5		
FPGA PLL		14	14		
HPS PLL		3	3		
6 Gbps Transceiver		30	30		
FPGA GPIO ⁽⁸⁾		540	540		
HPS I/O	HPS I/O		208		
	Transmitter	120	120		
	Receiver	136	136		
PCIe Hard IP Block		2	2		
FPGA Hard Memory Controller		3	3		
HPS Hard Memory C	Controller	1	1		
ARM Cortex-A9 MP	Core Processor	Dual-core	Dual-core		

Related Information

High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook

Provides the number of LVDS channels in each device package.

Package Plan

Table 11: Package Plan for Arria V SX Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

	F896		F1152			F1517			
Member	(31 mm)		(35 mm)		(40 mm)				
Code	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR
B3	250	208	12	385	208	18	540	208	30
B5	250	208	12	385	208	18	540	208	30

Arria V ST

This section provides the available options, maximum resource counts, and package plan for the Arria V ST devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.



⁽⁸⁾ The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

Related Information

Altera Product Selector

Provides the latest information about Altera products.

Available Options

Figure 5: Sample Ordering Code and Available Options for Arria V ST Devices



Maximum Resources

Table 12: Maximum Resource Counts for Arria V ST Devices

Doco		Member Code			
Reso	ource	D3	D5		
Logic Elements (LE)	(K)	350	462		
ALM		132,075	174,340		
Register		528,300	697,360		
Momory (Kb)	M10K	17,290	22,820		
Memory (RD)	MLAB	2,014	2,658		
Variable-precision D	SP Block	809	1,090		
18 x 18 Multiplier		1,618	2,180		
FPGA PLL		14	14		
HPS PLL		3	3		
Transceiver	6-Gbps	30	30		
114115001701	10-Gbps ⁽⁹⁾	16	16		

Altera Corporation

Arria V Device Overview



Pasource		Member Code			
nesu	Resource		D5		
FPGA GPIO ⁽¹⁰⁾		540	540		
HPS I/O		208	208		
LVDS	Transmitter	120	120		
L V D 3	Receiver	136	136		
PCIe Hard IP Block		2	2		
FPGA Hard Memory Controller		3	3		
HPS Hard Memory C	Controller	1	1		
ARM Cortex-A9 MP	Core Processor	Dual-core	Dual-core		

Related Information

• High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook

Provides the number of LVDS channels in each device package.

• Transceiver Architecture in Arria V Devices Describes 10 Gbps channels usage conditions and SFF-8431 compliance requirements.

Package Plan

Table 13: Package Plan for Arria V ST Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Memb	F896 (31 mm)				F1152 (35 mm)				F1517 (40 mm)			
er Code	FPGA GPIO	црс	ХС	VR	FPGA GPIO	HPS I/O	XCVR		EDCA	Прс	XCVR	
		I/O	6 Gbps	10 Gbps			6 Gbps	10 Gbps	GPIO	I/O	6 Gbps	10 Gbps
D3	250	208	12	6	385	208	18	8	540	208	30	16
D5	250	208	12	6	385	208	18	8	540	208	30	16

⁽⁹⁾ Chip-to-chip connections only. For 10 Gbps channel usage conditions, refer to the Transceiver Architecture in Arria V Devices chapter.

⁽¹⁰⁾ The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

I/O Vertical Migration for Arria V Devices

Figure 6: Vertical Migration Capability Across Arria V Device Packages and Densities

The arrows indicate the vertical migration paths. Some packages have several migration paths. The devices included in each vertical migration path are shaded. You can also migrate your design across device densities in the same package option if the devices have the same dedicated pins, configuration pins, and power pins.

Mariant	Member	Package								
variant	Code	F6	72	F780	F896	F 1152	F1517			
	A1									
	A3									
	A5					1				
Arria V CY	A7	•								
Allia V GA	B1						1			
	B3									
	B5									
	B7									
	C3		•		•					
Arria V GT	С7									
	D3									
	D7					•	•			
	E1					•				
Arria V G7	E3			•						
	E5						•			
	E7					•				
Arria V SX	B3					•				
	B5									
Arria V ST	D3									
	D5				•	•	•			

You can achieve the vertical migration shaded in red if you use only up to 320 GPIOs, up to nine 6 Gbps transceiver channels, and up to four 10 Gbps transceiver (for Arria V GT devices). This migration path is not shown in the Quartus Prime software Pin Migration View.

- **Note:** To verify the pin migration compatibility, use the Pin Migration View window in the Quartus Prime software Pin Planner.
- **Note:** Except for Arria V GX A5 and A7, and Arria V GT C7 devices, all other Arria V GX and GT devices require a specific power-up sequence. If you plan to migrate your design from Arria V GX A5 and A7, and Arria V GT C7 devices to other Arria V devices, your design must adhere to the same required power-up sequence.

Arria V Device Overview



Related Information

- Managing Device I/O Pins chapter, Quartus Prime Handbook Provides more information about vertical I/O migrations.
- **Power Management in Arria V Devices** Describes the power-up sequence required for Arria V GX and GT devices.

Adaptive Logic Module

Arria V devices use a 28 nm ALM as the basic building block of the logic fabric.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than previous generations.

Figure 7: ALM for Arria V Devices



You can configure up to 50% of the ALMs in the Arria V devices as distributed memory using MLABs.

Related Information

Embedded Memory Capacity in Arria V Devices on page 20 Lists the embedded memory capacity for each device.



Types of Embedded Memory

The Arria V devices contain two types of memory blocks:

- 20 Kb M20K or 10 Kb M10K blocks—blocks of dedicated memory resources. The M20K and M10K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dualpurpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Arria V devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB. You can also configure these ALMs, in Arria V GZ devices, as ten 64 x 1 blocks, giving you one 64 x 10 simple dual-port SRAM block per MLAB.

Embedded Memory Capacity in Arria V Devices

		M20K		M1	0К	ML	AB	
Variant	Membe r Code	Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	Total RAM Bit (Kb)
	A1	_	_	800	8,000	741	463	8,463
	A3			1,051	10,510	1538	961	11,471
	A5	_		1,180	11,800	1877	1,173	12,973
Arria V CX	A7			1,366	13,660	2317	1,448	15,108
	B1	_	_	1,510	15,100	2964	1,852	16,952
	B3	_	—	1,726	17,260	3357	2,098	19,358
	B5	_	_	2,054	20,540	4052	2,532	23,072
	B7	—	_	2,414	24,140	4650	2,906	27,046
	C3		_	1,051	10,510	1538	961	11,471
Arria V CT	C7	_	—	1,366	13,660	2317	1,448	15,108
Allia v GI	D3			1,726	17,260	3357	2,098	19,358
	D7			2,414	24,140	4650	2,906	27,046
	E1	585	11,700	_		4,151	2,594	14,294
Arrio V CZ	E3	957	19,140	_		6,792	4,245	23,385
Arna v GZ	E5	1,440	28,800	_		7,548	4,718	33,518
	E7	1,700	34,000	_	_	8,490	5,306	39,306
Arria V SX	B3	_		1,729	17,290	3223	2,014	19,304
	B5	_	_	2,282	22,820	4253	2,658	25,478

Table 16: Embedded Memory Capacity and Distribution in Arria V Devices

Arria V Device Overview



PCIe Gen1, Gen2, and Gen 3 Hard IP

Arria V devices contain PCIe hard IP that is designed for performance and ease-of-use. The PCIe hard IP consists of the MAC, data link, and transaction layers.

The PCIe hard IP supports PCIe Gen3, Gen 2, and Gen 1 end point and root port for up to x8 lane configuration.

The PCIe endpoint support includes multifunction support for up to eight functions, as shown in the following figure. The integrated multifunction support reduces the FPGA logic requirements by up to 20,000 LEs for PCIe designs that require multiple peripherals.

Figure 8: PCIe Multifunction for Arria V Devices



The Arria V PCIe hard IP operates independently from the core logic. This independent operation allows the PCIe link to wake up and complete link training in less than 100 ms while the Arria V device completes loading the programming file for the rest of the device.

In addition, the PCIe hard IP in the Arria V device provides improved end-to-end datapath protection using ECC.

External Memory Interface

This section provides an overview of the external memory interface in Arria V devices.

Hard and Soft Memory Controllers

Arria V GX,GT, SX, and ST devices support up to four hard memory controllers for DDR3 and DDR2 SDRAM devices. Each controller supports 8 to 32 bit components of up to 4 gigabits (Gb) in density with two chip selects and optional ECC. For the Arria V SoC devices, an additional hard memory controller in the HPS supports DDR3, DDR2, and LPDDR2 SDRAM devices.

All Arria V devices support soft memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices, QDR II+, QDR II, and DDR II+ SRAM devices, and RLDRAM II devices for maximum flexibility.

Note: DDR3 SDRAM leveling is supported only in Arria V GZ devices.

Arria V Device Overview

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Related Information

External Memory Interface Spec Estimator

For the latest information and to estimate the external memory system performance specification, use Altera's External Memory Interface Spec Estimator tool.

Low-Power Serial Transceivers

Arria V devices deliver the industry's lowest power consumption per transceiver channel:

- 12.5 Gbps transceivers at less than 170 mW
- 10 Gbps transceivers at less than 165 mW
- 6 Gbps transceivers at less than 105 mW

Arria V transceivers are designed to be compliant with a wide range of protocols and data rates.

Transceiver Channels

The transceivers are positioned on the left and right outer edges of the device. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks.

The following figures are graphical representations of a top view of the silicon die, which corresponds to a reverse view for flip chip packages. Different Arria V devices may have different floorplans than the ones shown in the figures.

Arria V Device Overview

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Figure 9: Device Chip Overview for Arria V GX and GT Devices

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Arria V Device Overview



PCS Features

PCS Support ⁽¹³⁾	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
PCIe Gen1 (x1, x2, x4, x8) PCIe Gen2 ⁽¹⁴⁾ (x1, x2, x4)	2.5 and 5.0	 Phase compensation FIFO Byte serializer 8B/10B encoder PIPE 2.0 interface to the core logic 	 Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO Rate match FIFO PIPE 2.0 interface to the core logic
GbE	1.25	 Phase compensation FIFO Byte serializer 8B/10B encoder 	 Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO Rate match FIFO
XAUI ⁽¹⁵⁾	3.125	 Phase compensation FIFO Byte serializer 8B/10B encoder XAUI state machine for bonding four channels 	 Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO XAUI state machine for realigning four channels Deskew FIFO circuitry
SDI	0.27 ⁽¹⁶⁾ , 1.485, 2.97	 Phase compensation FIFO Byte serializer 	 Byte deserializer Phase compensation FIFO
GPON ⁽¹⁷⁾	1.25 and 2.5		
CPRI ⁽¹⁸⁾	0.6144 to 6.144	 Phase compensation FIFO Byte serializer 8B/10B encoder TX deterministic latency 	 Word aligner 8B/10B decoder Byte deserializer Phase compensation FIFO RX deterministic latency



⁽¹³⁾ Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through the soft PCS.

⁽¹⁴⁾ PCIe Gen2 is supported only through the PCIe hard IP.

⁽¹⁵⁾ XAUI is supported through the soft PCS.

⁽¹⁶⁾ The 0.27 Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

⁽¹⁷⁾ The GPON standard does not support burst mode.

⁽¹⁸⁾ CPRI data rates above 6.5536 Gbps, such as 9.8304 Gbps, are supported through the soft PCS.

SoC with HPS

Each SoC combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

HPS Features

The HPS consists of a dual-core ARM Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in the following figure.

Figure 12: HPS with Dual-Core ARM Cortex-A9 MPCore Processor





System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals to interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

HPS-FPGA AXI Bridges

The HPS–FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA[®]) Advanced eXtensible Interface (AXI[™]) specifications, consist of the following bridges:

- FPGA-to-HPS AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to slaves in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS–FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS–FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon[®] Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features. The SDRAM controller subsystem supports DDR2, DDR3, or LPDDR2 devices up to 4 Gb in density operating at up to 533 MHz (1066 Mbps data rate).

FPGA Configuration and Processor Booting

The FPGA fabric and HPS in the SoC are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power, or shut down the entire FPGA fabric to reduce total system power.



You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- You can power up both the HPS and the FPGA fabric together, configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

Note: Although the FPGA fabric and HPS are on separate power domains, the HPS must remain powered up during operation while the FPGA fabric can be powered up or down as required.

Related Information

• Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines

Provides detailed information about power supply pin connection guidelines and power regulator sharing.

• Arria V GZ Device Family Pin Connection Guidelines Provides detailed information about power supply pin connection guidelines and power regulator sharing.

Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Qsys system integration tool in the Quartus Prime software.

For software development, the ARM-based SoC devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Altera SoCs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux, VxWorks[®], and other operating systems is available for the SoCs. For more information on the operating systems support availability, contact the Altera sales team.

You can begin device-specific firmware and software development on the Altera SoC Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board that runs on a PC. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

Related Information

Altera Worldwide Sales Support

Dynamic and Partial Reconfiguration

The Arria V devices support dynamic reconfiguration and partial reconfiguration.

Dynamic Reconfiguration

The dynamic reconfiguration feature allows you to dynamically change the transceiver data rates, PMA settings, or protocols of a channel, without affecting data transfer on adjacent channels. This feature is ideal for applications that require on-the-fly multiprotocol or multirate support. You can reconfigure the PMA, PCS, and PCIe hard IP blocks with dynamic reconfiguration.

Arria V Device Overview

Altera Corporation



Partial Reconfiguration

Note: Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

Partial reconfiguration allows you to reconfigure part of the device while other sections of the device remain operational. This capability is important in systems with critical uptime requirements because it allows you to make updates or adjust functionality without disrupting services.

Apart from lowering cost and power consumption, partial reconfiguration increases the effective logic density of the device because placing device functions that do not operate simultaneously is not necessary. Instead, you can store these functions in external memory and load them whenever the functions are required. This capability reduces the size of the device because it allows multiple applications on a single device—saving the board space and reducing the power consumption.

Altera simplifies the time-intensive task of partial reconfiguration by building this capability on top of the proven incremental compile and design flow in the Quartus Prime design software. With the Altera solution, you do not need to know all the intricate device architecture details to perform a partial reconfiguration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable simultaneous partial reconfiguration of both the device core and transceivers.

Enhanced Configuration and Configuration via Protocol

Table 23: Configuration Modes and Features of Arria V Devices

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Mode	Data Width	Max Clock Rate (MHz)	Max Data[Rate (Mbps)	Decompressio	Design Security R	Partial econfiguratio (20)	Remote System Update	
AS through the EPCS and EPCQ serial configura- tion device	1 bit, 4 bits	100		Yes	Yes		Yes	
PS through CPLD or external microcontroller	1 bit	125	125	Yes	Yes	_	_	

Arria V devices support 1.8 V, 2.5 V, 3.0 V, and 3.3 V⁽¹⁹⁾ programming voltages and several configuration modes.

Arria V Device Overview



⁽¹⁹⁾ Arria V GZ does not support 3.3 V.

⁽²⁰⁾ Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

Document Revision History

Date	Version	Changes
December 2015	2015.12.21	 Updated RoHS and optional suffix information in sample ordering code and available options diagrams for Arria V GX and GT devices. Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.
January 2015	2015.01.23	 Updated package dimension for Arria V GZ H780 package from 29 mm to 33 mm. Updated dual-core ARM Cortex-A9 MPCore processor maximum frequency from 800 MHz to 1.05 GHz.
December 2013	2013.12.26	 10-Gbps Ethernet (10GbE) PCS and Interlaken PCS are for Arria V GZ only. Removed "Preliminary" texts from Ordering Code figures, Maximum Resources, Package Plan and I/O Vertical Migration tables. Added link to Altera Product Selector for each device variant. Added leaded package options. Removed the note "The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs." for all PLLs in the Maximum Resource Counts table. Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F896 package from 170 to 250. Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F1512 package from 350 to 385. Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F1517 package from 528 to 540. Corrected LVDS Transmitter for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 devices from 121 to 120. Added links to Altera's External Memory Spec Estimator tool to the topics listing the external memory interface performance. Added x2 for PCIe Gen3, Gen 2, and Gen 1.
August 2013	2013.08.19	 Removed the note about the PCIe hard IP on the right side of the device in the F896 package of the Arria V GX variant. These devices do not have PCIe hard IP on the right side. Added transceiver speed grade 6 to the available options of the Arria V SX variant. Corrected the maximum LVDS transmitter channel counts for the Arria V GX A1 and A3 devices from 68 to 67. Corrected the maximum FPGA GPIO count for Arria V ST D5 devices from 540 to 528.

Arria V Device Overview

