Intel - 5ASXFB3G4F35C6N Datasheet

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	700MHz
Primary Attributes	FPGA - 350K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA, FC (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5asxfb3g4f35c6n

Advantage	Supporting Feature
Lowest system cost	• Requires as few as four power supplies to operate • Available in thermal composite flip chip ball-grid array (BGA) packaging • Includes innovative features such as Configuration via Protocol (CvP), partial reconfiguration, and design security

Summary of Arria V Features

Table 2: Summary of Features for Arria V Devices

Feature	Description

Technology	• TSMC's 28-nm process technology:
	  • Arria V GX, GT, SX, and ST—28-nm low power (28LP) process
	  • Arria V GZ—28-nm high performance (28HP) process
	• Lowest static power in its class (less than 1.2 W for 500K logic elements (LEs) at 85°C junction under typical conditions)
	• 0.85 V, 1.1 V, or 1.15 V core nominal voltage

Packaging	• Thermal composite flip chip BGA packaging • Multiple device densities with identical package footprints for seamless migration between different device densities • Leaded[(1)], lead-free (Pb-free), and RoHS-compliant options
High-performance FPGA fabric	• Enhanced 8-input ALM with four registers • Improved routing architecture to reduce congestion and improve compilation time
Internal memory blocks	• M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC) (Arria V GX, GT, SX, and ST devices only) • M20K—20-Kb memory blocks with hard ECC (Arria V GZ devices only) • Memory logic array block (MLAB)-640-bit distributed LUTRAM where you can use up to 50% of the ALMs as MLAB memory

(1) Contact Altera for availability.

Feature	Description	

Embedded Hard IP blocks	Variable-precision DSP	• Native support for up to four signal processing precision levels:
		  • Three 9 x 9, two 18 x 18, or one 27 x 27 multiplier in the same variable-precision DSP block
		  • One 36 x 36 multiplier using two variable-precision DSP blocks (Arria V GZ devices only)
		• 64-bit accumulator and cascade for systolic finite impulse responses (FIRs)
		• Embedded internal coefficient memory
		• Preadder/subtractor for improved efficiency

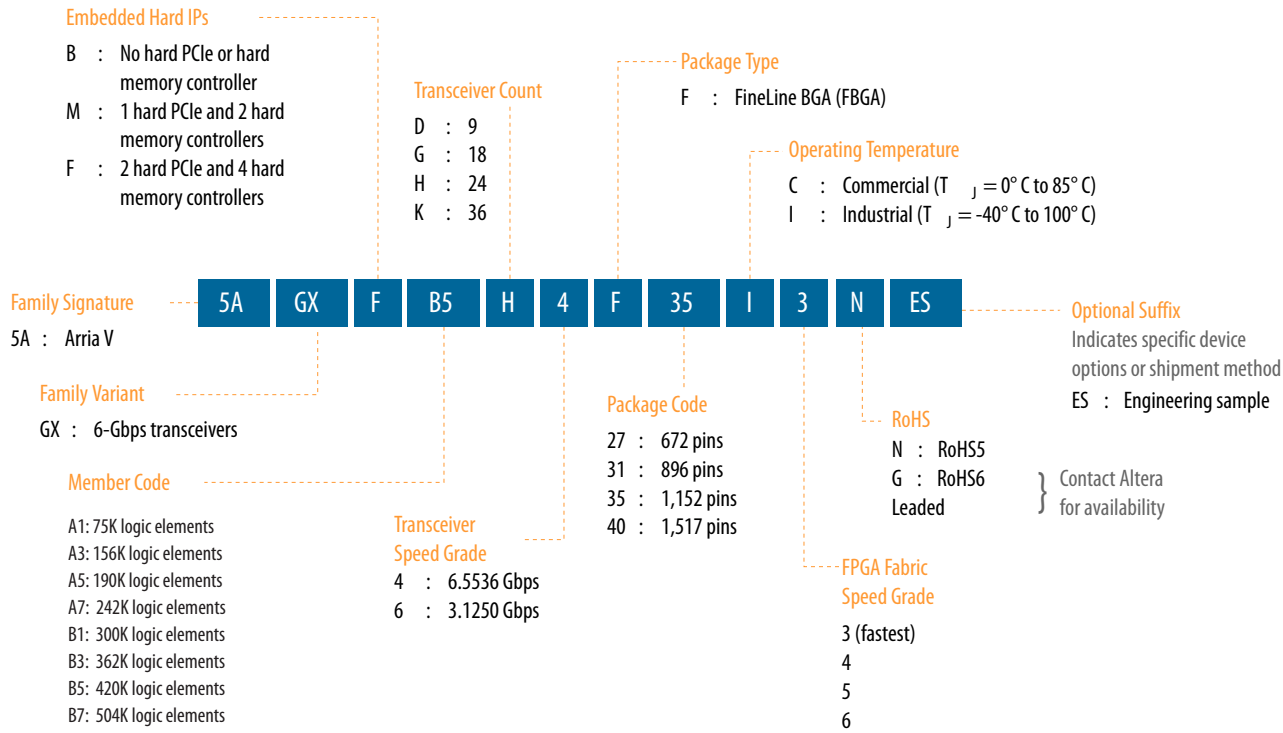
	Memory controller (Arria V GX, GT, SX, and ST only)	DDR3 and DDR2

	Embedded transceiver I/O	• Custom implementation:
		  • Arria V GX and SX devices—up to 6.5536 Gbps
		  • Arria V GT and ST devices—up to 10.3125 Gbps
		  • Arria V GZ devices—up to 12.5 Gbps
		• PCI Express® (PCIe®) Gen2 (x1, x2, or x4) and Gen1 (x1, x2, x4, or x8) hard IP with multifunction support, endpoint, and root port
		• PCIe Gen3 (x1, x2, x4, or x8) support (Arria V GZ only)
		• Gbps Ethernet (GbE) and XAUI physical coding sublayer (PCS)
		• Common Public Radio Interface (CPRI) PCS
		• Gigabit-capable passive optical network (GPON) PCS
		• 10-Gbps Ethernet (10GbE) PCS (Arria V GZ only)
		• Serial RapidIO® (SRIO) PCS
		• Interlaken PCS (Arria V GZ only)

Clock networks	• Up to 650 MHz global clock network • Global, quadrant, and peripheral clock networks • Clock networks that are not used can be powered down to reduce dynamic power	
Phase-locked loops (PLLs)	• High-resolution fractional PLLs • Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB) • Integer mode and fractional mode • LC oscillator ATX transmitter PLLs (Arria V GZ only)	

Available Options

Figure 1: Sample Ordering Code and Available Options for Arria V GX Devices



Maximum Resources

Table 4: Maximum Resource Counts for Arria V GX Devices

Resource		Member Code							
		A1	A3	A5	A7	B1	B3	B5	B7
Logic Elements (LE) (K)		75	156	190	242	300	362	420	504
ALM		28,302	58,900	71,698	91,680	113,208	136,880	158,491	190,240
Register		113,208	235,600	286,792	366,720	452,832	547,520	633,964	760,960
Memory (Kb)	M10K	8,000	10,510	11,800	13,660	15,100	17,260	20,540	24,140
	MLAB	463	961	1,173	1,448	1,852	2,098	2,532	2,906
Variable-precision DSP Block		240	396	600	800	920	1,045	1,092	1,156
18 x 18 Multiplier		480	792	1,200	1,600	1,840	2,090	2,184	2,312
PLL		10	10	12	12	12	12	16	16

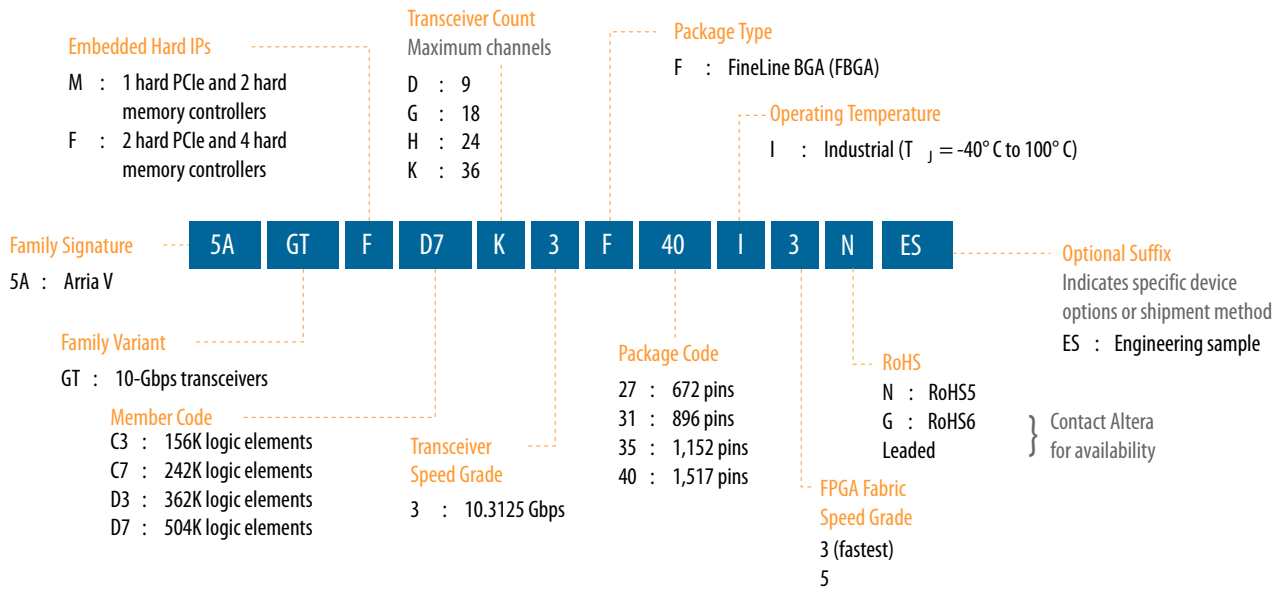
The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

Related Information

Altera Product Selector
Provides the latest information about Altera products.

Available Options

Figure 2: Sample Ordering Code and Available Options for Arria V GT Devices



Maximum Resources

Table 6: Maximum Resource Counts for Arria V GT Devices

Resource		Member Code			
		C3	C7	D3	D7
Logic Elements (LE) (K)		156	242	362	504
ALM		58,900	91,680	136,880	190,240
Register		235,600	366,720	547,520	760,960
Memory (Kb)	M10K	10,510	13,660	17,260	24,140
	MLAB	961	1,448	2,098	2,906
Variable-precision DSP Block		396	800	1,045	1,156
18 x 18 Multiplier		792	1,600	2,090	2,312
PLL		10	12	12	16

Resource		Member Code			
		E1	E3	E5	E7
Memory (Kb)	M20K	11,700	19,140	28,800	34,000
	MLAB	2,594	4,245	4,718	5,306
Variable-precision DSP Block		800	1,044	1,092	1,139
18 x 18 Multiplier		1,600	2,088	2,184	2,278
PLL		20	20	24	24
12.5 Gbps Transceiver		24	24	36	36
GPIO[7]		414	414	674	674
LVDS	Transmitter	99	99	166	166
	Receiver	108	108	168	168
PCIe Hard IP Block		1	1	1	1

Related Information

High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook
Provides the number of LVDS channels in each device package.

Package Plan

Table 9: Package Plan for Arria V GZ Devices

Member Code	H780 (33 mm)		F1152 (35 mm)		F1517 (40 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
E1	342	12	414	24	—	—
E3	342	12	414	24	—	—
E5	—	—	534	24	674	36
E7	—	—	534	24	674	36

Arria V SX

This section provides the available options, maximum resource counts, and package plan for the Arria V SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

(7) The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

Resource		Member Code	
		B3	B5
FPGA PLL		14	14
HPS PLL		3	3
6 Gbps Transceiver		30	30
FPGA GPIO[8]		540	540
HPS I/O		208	208
LVDS	Transmitter	120	120
	Receiver	136	136
PCIe Hard IP Block		2	2
FPGA Hard Memory Controller		3	3
HPS Hard Memory Controller		1	1
ARM Cortex-A9 MPCore Processor		Dual-core	Dual-core

Related Information

High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook

Provides the number of LVDS channels in each device package.

Package Plan

Table 11: Package Plan for Arria V SX Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	F896 (31 mm)			F1152 (35 mm)			F1517 (40 mm)		
	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR
B3	250	208	12	385	208	18	540	208	30
B5	250	208	12	385	208	18	540	208	30

Arria V ST

This section provides the available options, maximum resource counts, and package plan for the Arria V ST devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

(8) The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

Resource		Member Code	
		D3	D5
FPGA GPIO[10]		540	540
HPS I/O		208	208
LVDS	Transmitter	120	120
	Receiver	136	136
PCIe Hard IP Block		2	2
FPGA Hard Memory Controller		3	3
HPS Hard Memory Controller		1	1
ARM Cortex-A9 MPCore Processor		Dual-core	Dual-core

Related Information

- **High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook**
  Provides the number of LVDS channels in each device package.
- **Transceiver Architecture in Arria V Devices**
  Describes 10 Gbps channels usage conditions and SFF-8431 compliance requirements.

Package Plan

Table 13: Package Plan for Arria V ST Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	F896 (31 mm)				F1152 (35 mm)				F1517 (40 mm)			
	FPGA GPIO	HPS I/O	XCVR		FPGA GPIO	HPS I/O	XCVR		FPGA GPIO	HPS I/O	XCVR	
			6 Gbps	10 Gbps			6 Gbps	10 Gbps			6 Gbps	10 Gbps
D3	250	208	12	6	385	208	18	8	540	208	30	16
D5	250	208	12	6	385	208	18	8	540	208	30	16

(9) Chip-to-chip connections only. For 10 Gbps channel usage conditions, refer to the Transceiver Architecture in Arria V Devices chapter.

(10) The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

Variable-Precision DSP Block

Arria V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18, 27 x 27, and 36 x 36 bits natively
- A 64-bit accumulator
- Double accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Dynamic coefficients
- 18-bit internal coefficient register banks
- Enhanced independent multiplier operation
- Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Quartus Prime design software

Table 14: Variable-Precision DSP Block Configurations for Arria V Devices

Usage Example	Multiplier Size (Bit)	DSP Block Resource
Low precision fixed point for video applications	Three 9 x 9	1
Medium precision fixed point in FIR filters	Two 18 x 18	1
FIR filters	Two 18 x 18 with accumulate	1
Single-precision floating-point implementations	One 27 x 27	1
Very high precision fixed point implementations	One 36 x 36	2

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 18, or one 27 x 27 multipliers. Using two DSP block resources, you can also configure a 36 x 36 multiplier for high-precision applications. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

PLL Features

The PLLs in the Arria V devices support the following features:

- Frequency synthesis
- On-chip clock deskew
- Jitter attenuation
- Counter reconfiguration
- Programmable output clock duty cycles
- PLL cascading
- Reference clock switchover
- Programmable bandwidth
- Dynamic phase shift
- Zero delay buffers

Fractional PLL

In addition to integer PLLs, the Arria V devices use a fractional PLL architecture. The devices have up to 16 PLLs, each with 18 output counters. One fractional PLL can use up to 18 output counters and two adjacent fractional PLLs share the 18 output counters. You can use the output counters to reduce PLL usage in two ways:

- Reduce the number of oscillators that are required on your board by using fractional PLLs
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

If you use the fractional PLL mode, you can use the PLLs for precision fractional-N frequency synthesis—removing the need for off-chip reference clock sources in your design.

The transceiver fractional PLLs that are not used by the transceiver I/Os can be used as general purpose fractional PLLs by the FPGA fabric.

FPGA General Purpose I/O

Arria V devices offer highly configurable GPIOs. The following list describes the features of the GPIOs:

- Programmable bus hold and weak pull-up
- LVDS output buffer with programmable differential output voltage (V_{OD}) and programmable pre-emphasis
- On-chip parallel termination (R_T OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Unused voltage reference (`VREF`) pins that can be configured as user I/Os (Arria V GX, GT, SX, and ST only)
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

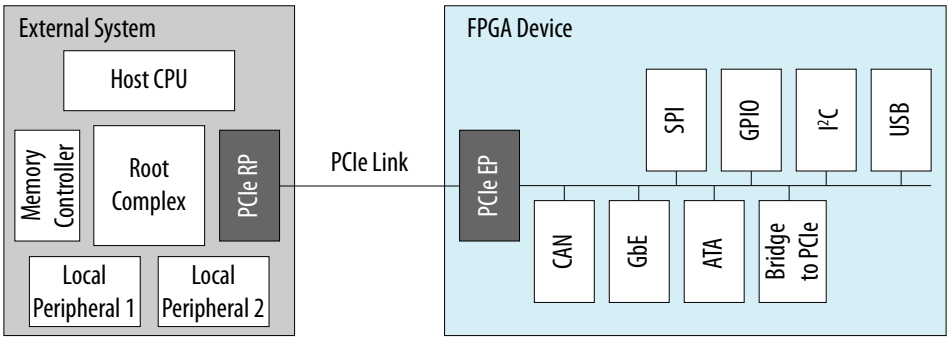
PCIe Gen1, Gen2, and Gen 3 Hard IP

Arria V devices contain PCIe hard IP that is designed for performance and ease-of-use. The PCIe hard IP consists of the MAC, data link, and transaction layers.

The PCIe hard IP supports PCIe Gen3, Gen 2, and Gen 1 end point and root port for up to x8 lane configuration.

The PCIe endpoint support includes multifunction support for up to eight functions, as shown in the following figure. The integrated multifunction support reduces the FPGA logic requirements by up to 20,000 LEs for PCIe designs that require multiple peripherals.

Figure 8: PCIe Multifunction for Arria V Devices



The Arria V PCIe hard IP operates independently from the core logic. This independent operation allows the PCIe link to wake up and complete link training in less than 100 ms while the Arria V device completes loading the programming file for the rest of the device.

In addition, the PCIe hard IP in the Arria V device provides improved end-to-end datapath protection using ECC.

External Memory Interface

This section provides an overview of the external memory interface in Arria V devices.

Hard and Soft Memory Controllers

Arria V GX,GT, SX, and ST devices support up to four hard memory controllers for DDR3 and DDR2 SDRAM devices. Each controller supports 8 to 32 bit components of up to 4 gigabits (Gb) in density with two chip selects and optional ECC. For the Arria V SoC devices, an additional hard memory controller in the HPS supports DDR3, DDR2, and LPDDR2 SDRAM devices.

All Arria V devices support soft memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices, QDR II+, QDR II, and DDR II+ SRAM devices, and RLDRAM II devices for maximum flexibility.

Note: DDR3 SDRAM leveling is supported only in Arria V GZ devices.

External Memory Performance

Table 18: External Memory Interface Performance in Arria V Devices

Interface	Voltage (V)	Hard Controller (MHz)	Soft Controller (MHz)	
		Arria V GX, GT, SX, and ST	Arria V GX, GT, SX, and ST	Arria V GZ
DDR3 SDRAM	1.5	533	667	800
	1.35	533	600	800
DDR2 SDRAM	1.8	400	400	400
LPDDR2 SDRAM	1.2	—	400	—
RLDRAM 3	1.2	—	—	667
RLDRAM II	1.8	—	400	533
	1.5	—	400	533
QDR II+ SRAM	1.8	—	400	500
	1.5	—	400	500
QDR II SRAM	1.8	—	400	333
	1.5	—	400	333
DDR II+ SRAM(12)	1.8	—	400	—
	1.5	—	400	—

Related Information

External Memory Interface Spec Estimator

For the latest information and to estimate the external memory system performance specification, use Altera's External Memory Interface Spec Estimator tool.

HPS External Memory Performance

Table 19: HPS External Memory Interface Performance

The hard processor system (HPS) is available in Arria V SoC devices only.

Interface	Voltage (V)	HPS Hard Controller (MHz)
DDR3 SDRAM	1.5	533
	1.35	533
LPDDR2 SDRAM	1.2	333

(12) Not available as Altera® IP.

Related Information

External Memory Interface Spec Estimator

For the latest information and to estimate the external memory system performance specification, use Altera's External Memory Interface Spec Estimator tool.

Low-Power Serial Transceivers

Arria V devices deliver the industry's lowest power consumption per transceiver channel:

- 12.5 Gbps transceivers at less than 170 mW
- 10 Gbps transceivers at less than 165 mW
- 6 Gbps transceivers at less than 105 mW

Arria V transceivers are designed to be compliant with a wide range of protocols and data rates.

Transceiver Channels

The transceivers are positioned on the left and right outer edges of the device. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks.

The following figures are graphical representations of a top view of the silicon die, which corresponds to a reverse view for flip chip packages. Different Arria V devices may have different floorplans than the ones shown in the figures.

Figure 10: Device Chip Overview for Arria V GZ Devices

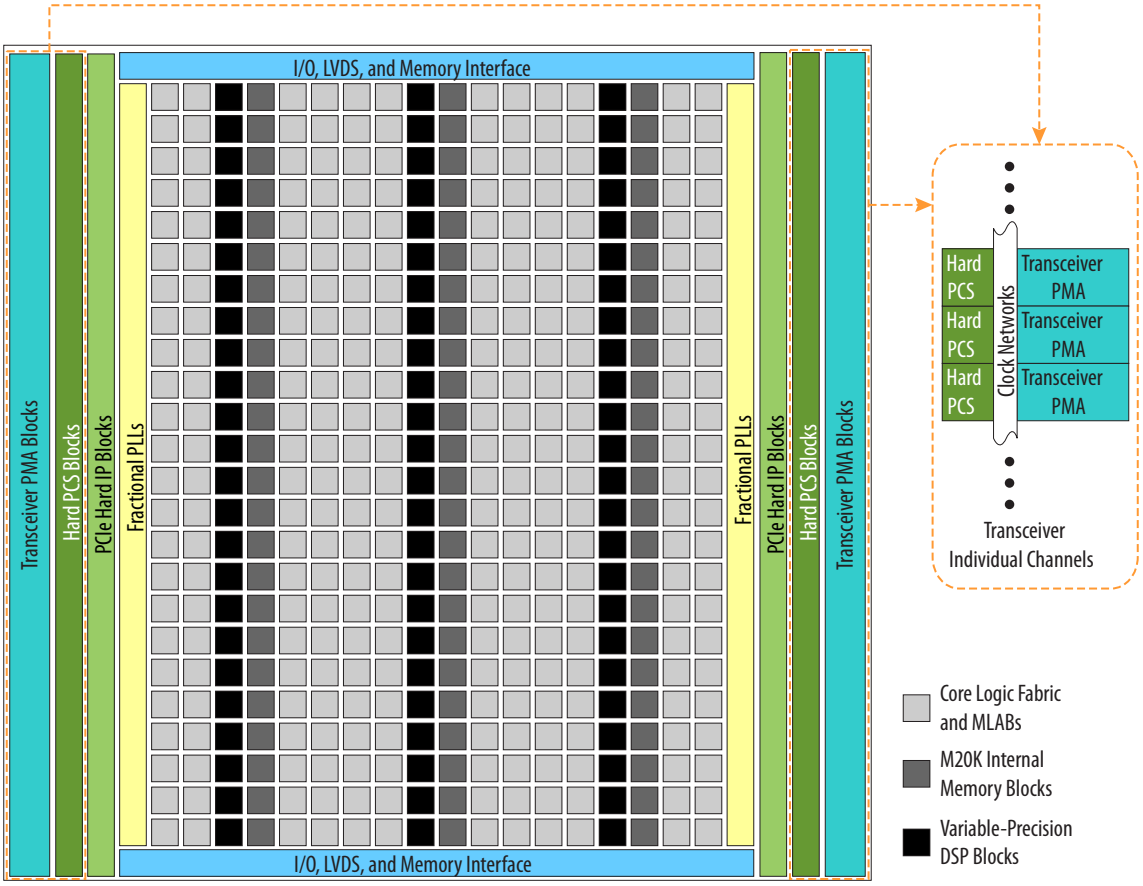
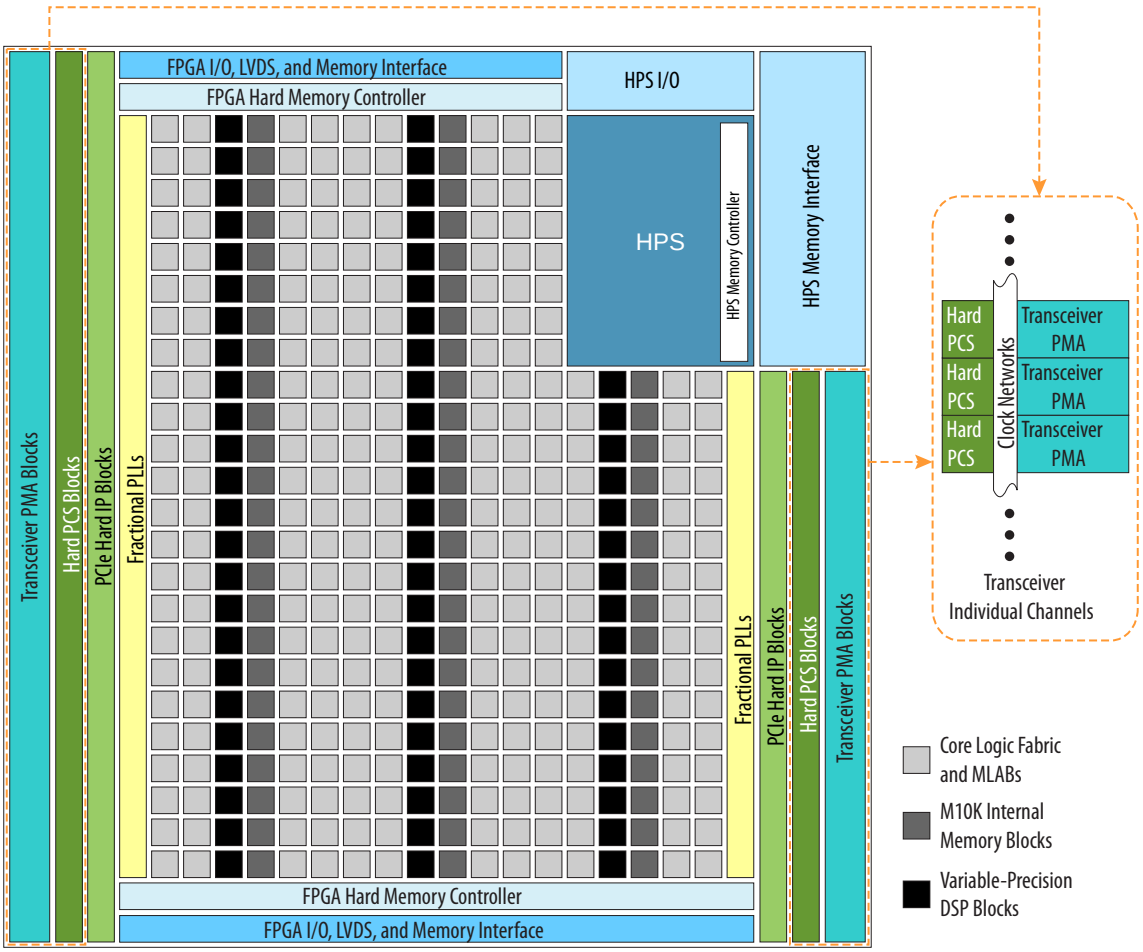


Figure 11: Device Chip Overview for Arria V SX and ST Devices



PMA Features

To prevent core and I/O noise from coupling into the transceivers, the PMA block is isolated from the rest of the chip—ensuring optimal signal integrity. For the transceivers, you can use the channel PLL of an unused receiver PMA as an additional transmit PLL.

Table 20: PMA Features of the Transceivers in Arria V Devices

Features	Capability
Backplane support	• Arria V GX, GT, SX, and ST devices—Driving capability at 6.5536 Gbps with up to 25 dB channel loss • Arria V GZ devices—Driving capability at 12.5 Gbps with up to 16 dB channel loss
Chip-to-chip support	• Arria V GX, GT, SX, and ST devices—Up to 10.3125 Gbps • Arria V GZ devices—Up to 12.5 Gbps

PCS Support[13]	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
PCIe Gen1 (x1, x2, x4, x8)	2.5 and 5.0	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • PIPE 2.0 interface to the core logic	• Word aligner • 8B/10B decoder • Byte deserializer • Phase compensation FIFO • Rate match FIFO • PIPE 2.0 interface to the core logic
PCIe Gen2[14] (x1, x2, x4)			
GbE	1.25	• Phase compensation FIFO • Byte serializer • 8B/10B encoder	• Word aligner • 8B/10B decoder • Byte deserializer • Phase compensation FIFO • Rate match FIFO
XAUI[15]	3.125	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • XAUI state machine for bonding four channels	• Word aligner • 8B/10B decoder • Byte deserializer • Phase compensation FIFO • XAUI state machine for realigning four channels • Deskew FIFO circuitry
SDI	0.27[16], 1.485, 2.97	• Phase compensation FIFO • Byte serializer	• Byte deserializer • Phase compensation FIFO
GPON[17]	1.25 and 2.5		
CPRI[18]	0.6144 to 6.144	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • TX deterministic latency	• Word aligner • 8B/10B decoder • Byte deserializer • Phase compensation FIFO • RX deterministic latency

(13) Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through the soft PCS.
(14) PCIe Gen2 is supported only through the PCIe hard IP.
(15) XAUI is supported through the soft PCS.
(16) The 0.27 Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.
(17) The GPON standard does not support burst mode.
(18) CPRI data rates above 6.5536 Gbps, such as 9.8304 Gbps, are supported through the soft PCS.

Table 22: Transceiver PCS Features for Arria V GZ Devices

Protocol	Data Rates (Gbps)	Transmitter Data Path Features	Receiver Data Path Features
Custom PHY	0.6 to 9.80	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • Bit-slip • Channel bonding	• Word aligner • Deskew FIFO • Rate match FIFO • 8B/10B decoder • Byte deserializer • Byte ordering
GPON	1.25 and 2.5		
Custom 10G PHY	9.98 to 12.5	• TX FIFO • Gear box • Bit-slip	• RX FIFO • Gear box
PCIe Gen1 (x1, x2 x4, x8)	2.5 and 5.0	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • Bit-slip • Channel bonding • PIPE 2.0 interface to core logic	• Word aligner • Deskew FIFO • Rate match FIFO • 8B/10B decoder • Byte deserializer, • Byte ordering • PIPE 2.0 interface to core logic
PCIe Gen2 (x1, x2, x4, x8)			
PCIe Gen3 (x1, x2, x4, x8)	8.0	• Phase compensation FIFO • 128B/130B encoder • Scrambler • Gear box • Bit-slip	• Block synchronization • Rate match FIFO • 128B/130B decoder • Descrambler • Phase compensation FIFO
10GbE	10.3125	• TX FIFO • 64B/66B encoder • Scrambler • Gear box	• RX FIFO • 64B/66B decoder • Descrambler • Block synchronization • Gear box
Interlaken	3.125 to 12.5	• TX FIFO • Frame generator • CRC-32 generator • Scrambler • Disparity generator • Gear box	• RX FIFO • Frame generator • CRC-32 checker • Frame decoder • Descrambler • Disparity checker • Block synchronization • Gear box

Protocol	Data Rates (Gbps)	Transmitter Data Path Features	Receiver Data Path Features
40GBASE-R Ethernet	4 x 10.3125	• TX FIFO • 64B/66B encoder • Scrambler • Alignment marker insertion • Gearbox • Block stripper	• RX FIFO • 64B/66B decoder • Descrambler • Lane reorder • Deskew • Alignment marker lock • Block synchronization • Gear box • Destripper
100GBASE-R Ethernet	10 x 10.3125		
40G and 100G OTN	(4 +1) x 11.3	• TX FIFO • Channel bonding • Byte serializer	• RX FIFO • Lane deskew • Byte deserializer
	(10 +1) x 11.3		
GbE	1.25	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • Bit-slip • Channel bonding • GbE state machine	• Word aligner • Deskew FIFO • Rate match FIFO • 8B/10B decoder • Byte deserializer • Byte ordering • GbE state machine
XAUI	3.125 to 4.25	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • Bit-slip • Channel bonding • XAUI state machine for bonding four channels	• Word aligner • Deskew FIFO • Rate match FIFO • 8B/10B decoder • Byte deserializer • Byte ordering • XAUI state machine for realigning four channels
SRIO	1.25 to 6.25	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • Bit-slip • Channel bonding • SRIO V2.1-compliant x2 and x4 channel bonding	• Word aligner • Deskew FIFO • Rate match FIFO • 8B/10B decoder • Byte deserializer • Byte ordering • SRIO V2.1-compliant x2 and x4 deskew state machine

Document Revision History

Date	Version	Changes
December 2015	2015.12.21	• Updated RoHS and optional suffix information in sample ordering code and available options diagrams for Arria V GX and GT devices. • Changed instances of *Quartus II* to *Quartus Prime*.
January 2015	2015.01.23	• Updated package dimension for Arria V GZ H780 package from 29 mm to 33 mm. • Updated dual-core ARM Cortex-A9 MPCore processor maximum frequency from 800 MHz to 1.05 GHz.
December 2013	2013.12.26	• 10-Gbps Ethernet (10GbE) PCS and Interlaken PCS are for Arria V GZ only. • Removed "Preliminary" texts from Ordering Code figures, Maximum Resources, Package Plan and I/O Vertical Migration tables. • Added link to **Altera Product Selector** for each device variant. • Added leaded package options. • Removed the note "The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs." for all PLLs in the Maximum Resource Counts table. • Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F896 package from 170 to 250. • Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F1152 package from 350 to 385. • Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F1517 package from 528 to 540. • Corrected LVDS Transmitter for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 devices from 121 to 120. • Added links to Altera's **External Memory Spec Estimator** tool to the topics listing the external memory interface performance. • Added x2 for PCIe Gen3, Gen 2, and Gen 1.
August 2013	2013.08.19	• Removed the note about the PCIe hard IP on the right side of the device in the F896 package of the Arria V GX variant. These devices do not have PCIe hard IP on the right side. • Added transceiver speed grade 6 to the available options of the Arria V SX variant. • Corrected the maximum LVDS transmitter channel counts for the Arria V GX A1 and A3 devices from 68 to 67. • Corrected the maximum FPGA GPIO count for Arria V ST D5 devices from 540 to 528.

Date	Version	Changes
June 2013	2013.06.03	• Removed statements about contacting Altera for SFF-8431 compliance requirements. Refer to the **Transceiver Architecture in Arria V Devices** chapter for the requirements.
May 2013	2013.05.06	• Moved all links to the Related Information section of respective topics for easy reference. • Added link to the known document issues in the Knowledge Base. • Updated the available options, maximum resource counts, and per package information for the Arria V SX and ST device variants. • Updated the variable DSP multipliers counts for the Arria V SX and ST device variants. • Clarified that partial reconfiguration is an advanced feature. Contact Altera for support of the feature. • Added footnote to clarify that MLAB 64 bits depth is available only for Arria V GZ devices. • Updated description about power-up sequence requirement for device migration to improve clarity.
January 2013	2013.01.11	• Added the L optional suffix to the Arria V GZ ordering code for the –I3 speed grade. • Added a note about the power-up sequence requirement if you plan to migrate your design from the Arria V GX A5 and A7, and Arria V GT C7 devices to other Arria V devices.
November 2012	2012.11.19	• Updated the summary of features. • Updated Arria V GZ information regarding 3.3 V I/O support. • Removed Arria V GZ engineering sample ordering code. • Updated the maximum resource counts for Arria V GX and GZ. • Updated Arria V ST ordering codes for transceiver count. • Updated transceiver counts for Arria V ST packages. • Added simplified floorplan diagrams for Arria V GZ, SX, and ST. • Added FPP x32 configuration mode for Arria V GZ only. • Updated CvP (PCIe) remote system update support information. • Added HPS external memory performance information. • Updated template.
October 2012	3.0	• Added Arria V GZ information. • Updated Table 1, Table 2, Table 3, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, and Table 21. • Added the “Arria V GZ” section. • Added Table 8, Table 9 and Table 22.

Date	Version	Changes
July 2012	2.1	• Added –I3 speed grade to Figure 1 for Arria V GX devices. • Updated the 6-Gbps transceiver speed from 6.553 Gbps to 6.5536 Gbps in Figure 3 and Figure 1.
June 2012	2.0	• Restructured the document. • Added the “Embedded Memory Capacity” and “Embedded Memory Configurations” sections. • Added Table 1, Table 3, Table 12, Table 15, and Table 16. • Updated Table 2, Table 4, Table 5, Table 6, Table 7, Table 8, Table 9, Table 10, Table 11, Table 13, Table 14, and Table 19. • Updated Figure 1, Figure 2, Figure 3, Figure 4, and Figure 8. • Updated the “FPGA Configuration and Processor Booting” and “Hardware and Software Development” sections. • Text edits throughout the document.
February 2012	1.3	• Updated Table 1–7 and Table 1–8. • Updated Figure 1–9 and Figure 1–10. • Minor text edits.
December 2011	1.2	Minor text edits.
November 2011	1.1	• Updated Table 1–1, Table 1–2, Table 1–3, Table 1–4, Table 1–6, Table 1–7, Table 1–9, and Table 1–10. • Added “SoC FPGA with HPS” section. • Updated “Clock Networks and PLL Clock Sources” and “Ordering Information” sections. • Updated Figure 1–5. • Added Figure 1–6. • Minor text edits.
August 2011	1.0	Initial release.