Welcome to **E-XFL.COM**

Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	1.05GHz
Primary Attributes	FPGA - 462K Logic Elements
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA, FC (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5asxfb5g4f35i3n

Advantage	Supporting Feature
Lowest system cost	• Requires as few as four power supplies to operate • Available in thermal composite flip chip ball-grid array (BGA) packaging • Includes innovative features such as Configuration via Protocol (CvP), partial reconfiguration, and design security

Summary of Arria V Features

Table 2: Summary of Features for Arria V Devices

Feature	Description

Technology	• TSMC's 28-nm process technology:
	  • Arria V GX, GT, SX, and ST—28-nm low power (28LP) process
	  • Arria V GZ—28-nm high performance (28HP) process
	• Lowest static power in its class (less than 1.2 W for 500K logic elements (LEs) at 85°C junction under typical conditions)
	• 0.85 V, 1.1 V, or 1.15 V core nominal voltage

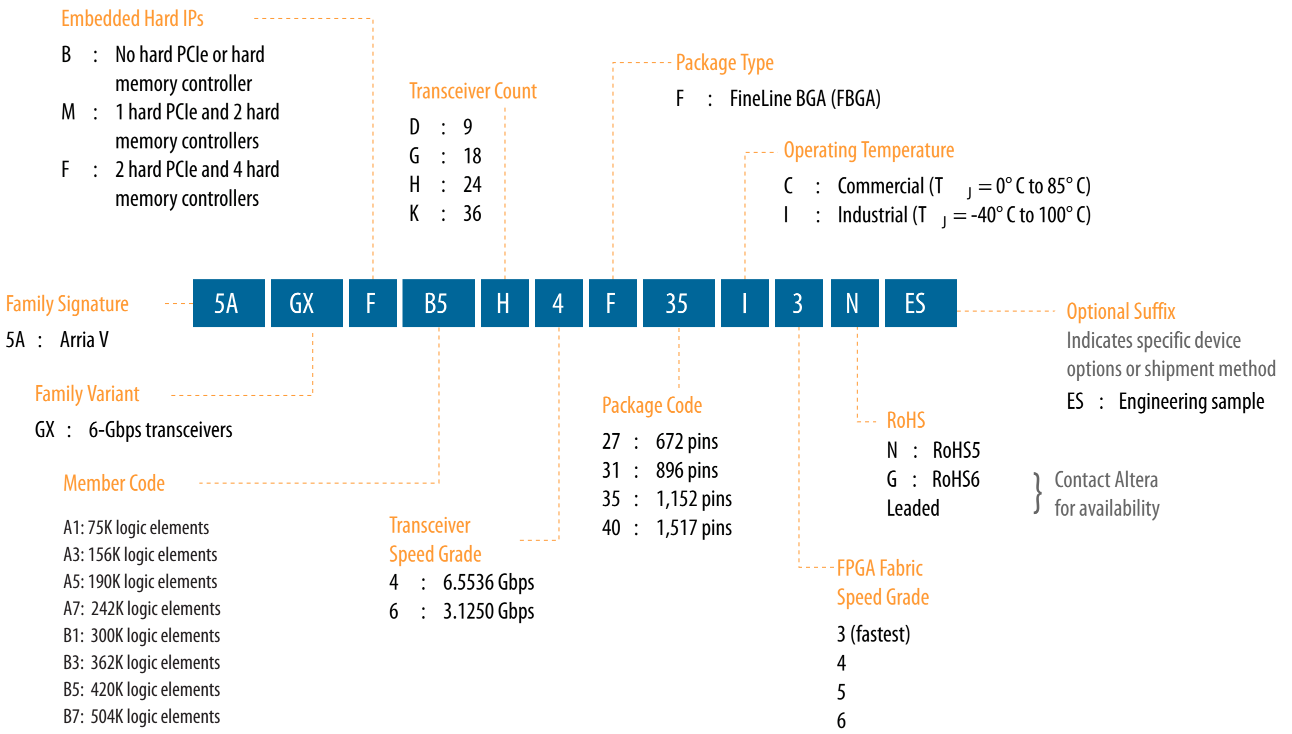
Packaging	• Thermal composite flip chip BGA packaging • Multiple device densities with identical package footprints for seamless migration between different device densities • Leaded(1), lead-free (Pb-free), and RoHS-compliant options
High-performance FPGA fabric	• Enhanced 8-input ALM with four registers • Improved routing architecture to reduce congestion and improve compilation time
Internal memory blocks	• M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC) (Arria V GX, GT, SX, and ST devices only) • M20K—20-Kb memory blocks with hard ECC (Arria V GZ devices only) • Memory logic array block (MLAB)-640-bit distributed LUTRAM where you can use up to 50% of the ALMs as MLAB memory

---

(1) Contact Altera for availability.

Available Options

Figure 1: Sample Ordering Code and Available Options for Arria V GX Devices



Maximum Resources

Table 4: Maximum Resource Counts for Arria V GX Devices

Resource		Member Code							
		A1	A3	A5	A7	B1	B3	B5	B7
Logic Elements (LE) (K)		75	156	190	242	300	362	420	504
ALM		28,302	58,900	71,698	91,680	113,208	136,880	158,491	190,240
Register		113,208	235,600	286,792	366,720	452,832	547,520	633,964	760,960
Memory (Kb)	M10K	8,000	10,510	11,800	13,660	15,100	17,260	20,540	24,140
	MLAB	463	961	1,173	1,448	1,852	2,098	2,532	2,906
Variable-precision DSP Block		240	396	600	800	920	1,045	1,092	1,156
18 x 18 Multiplier		480	792	1,200	1,600	1,840	2,090	2,184	2,312
PLL		10	10	12	12	12	12	16	16

Resource		Member Code							
		A1	A3	A5	A7	B1	B3	B5	B7
6 Gbps Transceiver		9	9	24	24	24	24	36	36
GPIO[3]		416	416	544	544	704	704	704	704
LVDS	Transmitter	67	67	120	120	160	160	160	160
	Receiver	80	80	136	136	176	176	176	176
PCIe Hard IP Block		1	1	2	2	2	2	2	2
Hard Memory Controller		2	2	4	4	4	4	4	4

Related Information

High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook

Provides the number of LVDS channels in each device package.

Package Plan

Table 5: Package Plan for Arria V GX Devices

Member Code	F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)		F1517 (40 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
A1	336	9	416	9	—	—	—	—
A3	336	9	416	9	—	—	—	—
A5	336	9	384	18	544	24	—	—
A7	336	9	384	18	544	24	—	—
B1	—	—	384	18	544	24	704	24
B3	—	—	384	18	544	24	704	24
B5	—	—	—	—	544	24	704	36
B7	—	—	—	—	544	24	704	36

Arria V GT

This section provides the available options, maximum resource counts, and package plan for the Arria V GT devices.

---

(3) The number of GPIOs does not include transceiver I/Os. In the Quartus® Prime software, the number of user I/Os includes transceiver I/Os.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

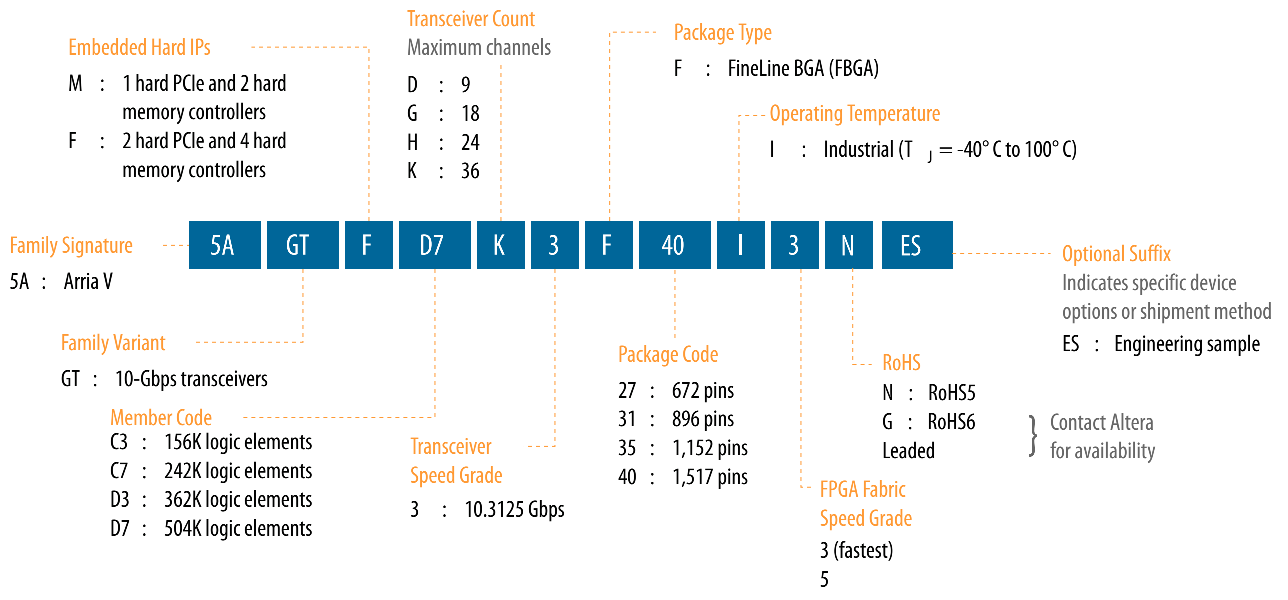
Related Information

Altera Product Selector

Provides the latest information about Altera products.

Available Options

Figure 2: Sample Ordering Code and Available Options for Arria V GT Devices



Maximum Resources

Table 6: Maximum Resource Counts for Arria V GT Devices

Resource		Member Code			
		C3	C7	D3	D7
Logic Elements (LE) (K)		156	242	362	504
ALM		58,900	91,680	136,880	190,240
Register		235,600	366,720	547,520	760,960
Memory (Kb)	M10K	10,510	13,660	17,260	24,140
	MLAB	961	1,448	2,098	2,906
Variable-precision DSP Block		396	800	1,045	1,156
18 x 18 Multiplier		792	1,600	2,090	2,312
PLL		10	12	12	16

Resource		Member Code			
		C3	C7	D3	D7
Transceiver	6 Gbps(4)	3 (9)	6 (24)	6 (24)	6 (36)
	10 Gbps(5)	4	12	12	20
GPIO(6)		416	544	704	704
LVDS	Transmitter	68	120	160	160
	Receiver	80	136	176	176
PCIe Hard IP Block		1	2	2	2
Hard Memory Controller		2	4	4	4

Related Information

- **High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook**
  Provides the number of LVDS channels in each device package.
- **Transceiver Architecture in Arria V Devices**
  Describes 10 Gbps channels usage conditions and SFF-8431 compliance requirements.

Package Plan

Table 7: Package Plan for Arria V GT Devices

Member Code	F672 (27 mm)			F896 (31 mm)			F1152 (35 mm)			F1517 (40 mm)		
	GPIO	XCVR		GPIO	XCVR		GPIO	XCVR		GPIO	XCVR	
		6-Gbps	10-Gbps		6-Gbps	10-Gbps		6-Gbps	10-Gbps		6-Gbps	10-Gbps
C3	336	3 (9)	4	416	3 (9)	4	—	—	—	—	—	—
C7	—	—	—	384	6 (18)	8	544	6 (24)	12	—	—	—
D3	—	—	—	384	6 (18)	8	544	6 (24)	12	704	6 (24)	12
D7	—	—	—	—	—	—	544	6 (24)	12	704	6 (36)	20

The 6-Gbps transceiver counts are for dedicated 6-Gbps channels. You can also configure any pair of 10-Gbps channels as three 6-Gbps channels—the total number of 6-Gbps channels are shown in brackets. For example, you can also configure the Arria V GT D7 device in the F1517 package with nine 6-Gbps

---

(4) The 6 Gbps transceiver counts are for dedicated 6-Gbps channels. You can also configure any pair of 10 Gbps channels as three 6 Gbps channels-the total number of 6 Gbps channels are shown in brackets.

(5) Chip-to-chip connections only. For 10 Gbps channel usage conditions, refer to the Transceiver Architecture in Arria V Devices chapter.

(6) The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

Resource		Member Code			
		E1	E3	E5	E7
Memory (Kb)	M20K	11,700	19,140	28,800	34,000
	MLAB	2,594	4,245	4,718	5,306
Variable-precision DSP Block		800	1,044	1,092	1,139
18 x 18 Multiplier		1,600	2,088	2,184	2,278
PLL		20	20	24	24
12.5 Gbps Transceiver		24	24	36	36
GPIO(7)		414	414	674	674
LVDS	Transmitter	99	99	166	166
	Receiver	108	108	168	168
PCIe Hard IP Block		1	1	1	1

Related Information

High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook

Provides the number of LVDS channels in each device package.

Package Plan

Table 9: Package Plan for Arria V GZ Devices

Member Code	H780 (33 mm)		F1152 (35 mm)		F1517 (40 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
E1	342	12	414	24	—	—
E3	342	12	414	24	—	—
E5	—	—	534	24	674	36
E7	—	—	534	24	674	36

Arria V SX

This section provides the available options, maximum resource counts, and package plan for the Arria V SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

---

(7) The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

Related Information

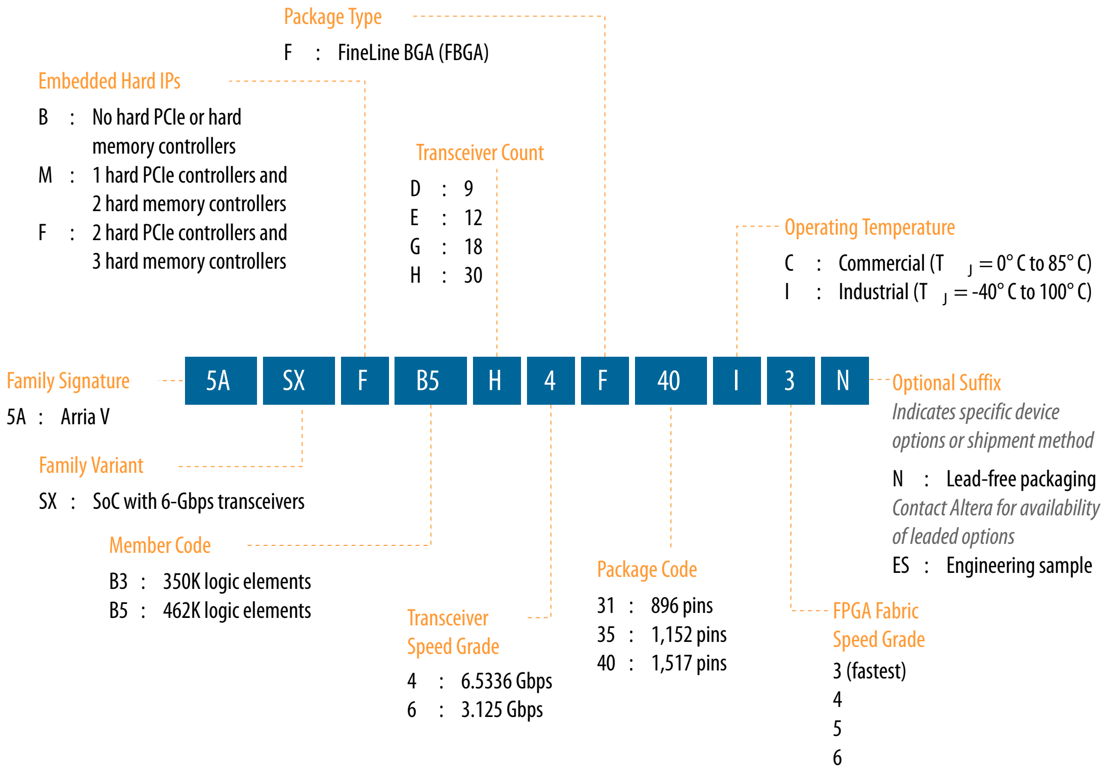
Altera Product Selector

Provides the latest information about Altera products.

Available Options

Figure 4: Sample Ordering Code and Available Options for Arria V SX Devices

The –3 FPGA fabric speed grade is available only for industrial temperature devices.



Maximum Resources

Table 10: Maximum Resource Counts for Arria V SX Devices

Resource		Member Code	
		B3	B5
Logic Elements (LE) (K)		350	462
ALM		132,075	174,340
Register		528,300	697,360
Memory (Kb)	M10K	17,290	22,820
	MLAB	2,014	2,658
Variable-precision DSP Block		809	1,090
18 x 18 Multiplier		1,618	2,180

Resource		Member Code	
		B3	B5
FPGA PLL		14	14
HPS PLL		3	3
6 Gbps Transceiver		30	30
FPGA GPIO[8]		540	540
HPS I/O		208	208
LVDS	Transmitter	120	120
	Receiver	136	136
PCIe Hard IP Block		2	2
FPGA Hard Memory Controller		3	3
HPS Hard Memory Controller		1	1
ARM Cortex-A9 MPCore Processor		Dual-core	Dual-core

Related Information

High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook

Provides the number of LVDS channels in each device package.

Package Plan

Table 11: Package Plan for Arria V SX Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	F896 (31 mm)			F1152 (35 mm)			F1517 (40 mm)		
	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR
B3	250	208	12	385	208	18	540	208	30
B5	250	208	12	385	208	18	540	208	30

Arria V ST

This section provides the available options, maximum resource counts, and package plan for the Arria V ST devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

---

[8] The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

Resource		Member Code	
		D3	D5
FPGA GPIO[10]		540	540
HPS I/O		208	208
LVDS	Transmitter	120	120
	Receiver	136	136
PCIe Hard IP Block		2	2
FPGA Hard Memory Controller		3	3
HPS Hard Memory Controller		1	1
ARM Cortex-A9 MPCore Processor		Dual-core	Dual-core

Related Information

- **High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook**
  Provides the number of LVDS channels in each device package.
- **Transceiver Architecture in Arria V Devices**
  Describes 10 Gbps channels usage conditions and SFF-8431 compliance requirements.

Package Plan

Table 13: Package Plan for Arria V ST Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	F896 (31 mm)				F1152 (35 mm)				F1517 (40 mm)			
	FPGA GPIO	HPS I/O	XCVR		FPGA GPIO	HPS I/O	XCVR		FPGA GPIO	HPS I/O	XCVR	
			6 Gbps	10 Gbps			6 Gbps	10 Gbps			6 Gbps	10 Gbps
D3	250	208	12	6	385	208	18	8	540	208	30	16
D5	250	208	12	6	385	208	18	8	540	208	30	16

---

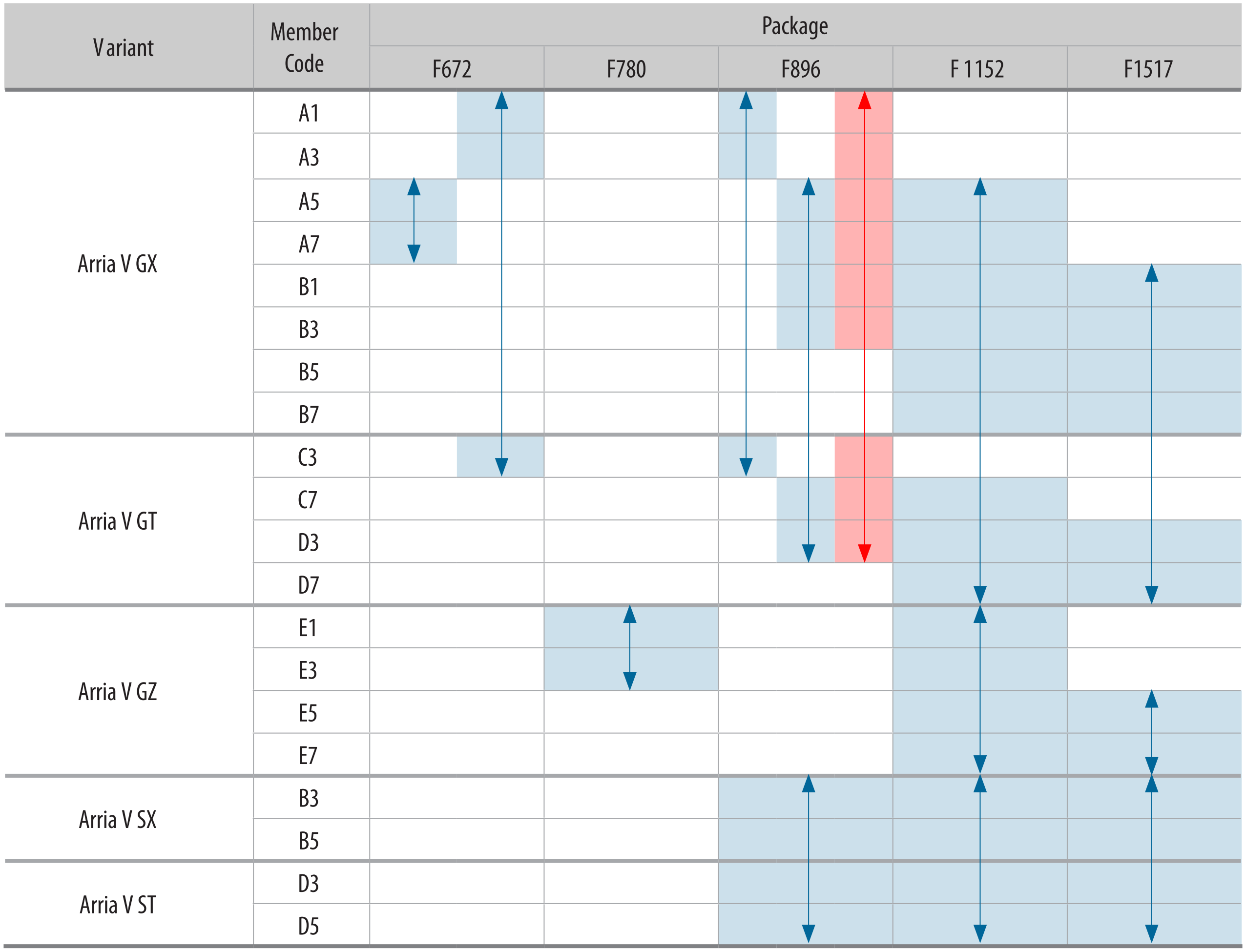
[9] Chip-to-chip connections only. For 10 Gbps channel usage conditions, refer to the Transceiver Architecture in Arria V Devices chapter.

[10] The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

I/O Vertical Migration for Arria V Devices

Figure 6: Vertical Migration Capability Across Arria V Device Packages and Densities

The arrows indicate the vertical migration paths. Some packages have several migration paths. The devices included in each vertical migration path are shaded. You can also migrate your design across device densities in the same package option if the devices have the same dedicated pins, configuration pins, and power pins.



You can achieve the vertical migration shaded in red if you use only up to 320 GPIOs, up to nine 6 Gbps transceiver channels, and up to four 10 Gbps transceiver (for Arria V GT devices). This migration path is not shown in the Quartus Prime software Pin Migration View.

Note: To verify the pin migration compatibility, use the Pin Migration View window in the Quartus Prime software Pin Planner.

Note: Except for Arria V GX A5 and A7, and Arria V GT C7 devices, all other Arria V GX and GT devices require a specific power-up sequence. If you plan to migrate your design from Arria V GX A5 and A7, and Arria V GT C7 devices to other Arria V devices, your design must adhere to the same required power-up sequence.

Related Information

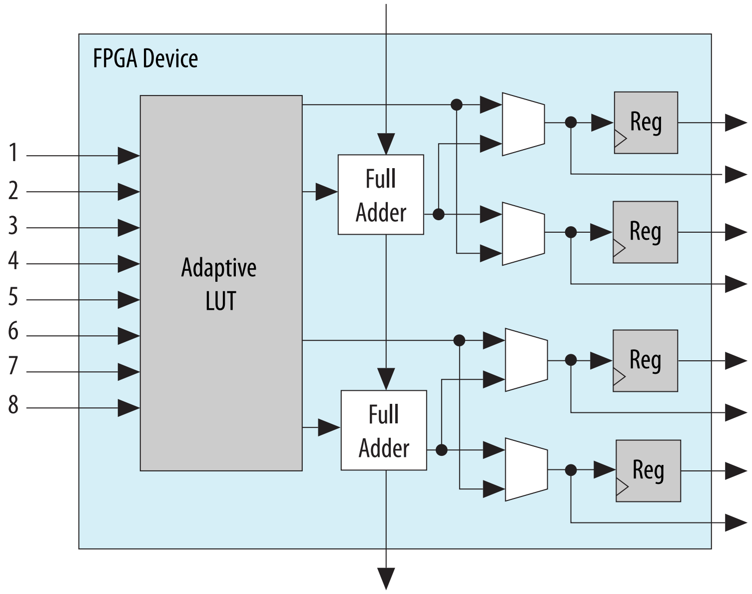
- **Managing Device I/O Pins chapter, Quartus Prime Handbook**
  Provides more information about vertical I/O migrations.
- **Power Management in Arria V Devices**
  Describes the power-up sequence required for Arria V GX and GT devices.

Adaptive Logic Module

Arria V devices use a 28 nm ALM as the basic building block of the logic fabric.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than previous generations.

Figure 7: ALM for Arria V Devices



You can configure up to 50% of the ALMs in the Arria V devices as distributed memory using MLABs.

Related Information

Embedded Memory Capacity in Arria V Devices on page 20
Lists the embedded memory capacity for each device.

External Memory Performance

Table 18: External Memory Interface Performance in Arria V Devices

Interface	Voltage (V)	Hard Controller (MHz)	Soft Controller (MHz)	
		Arria V GX, GT, SX, and ST	Arria V GX, GT, SX, and ST	Arria V GZ
DDR3 SDRAM	1.5	533	667	800
	1.35	533	600	800
DDR2 SDRAM	1.8	400	400	400
LPDDR2 SDRAM	1.2	—	400	—
RLDRAM 3	1.2	—	—	667
RLDRAM II	1.8	—	400	533
	1.5	—	400	533
QDR II+ SRAM	1.8	—	400	500
	1.5	—	400	500
QDR II SRAM	1.8	—	400	333
	1.5	—	400	333
DDR II+ SRAM(12)	1.8	—	400	—
	1.5	—	400	—

Related Information

External Memory Interface Spec Estimator

For the latest information and to estimate the external memory system performance specification, use Altera's External Memory Interface Spec Estimator tool.

HPS External Memory Performance

Table 19: HPS External Memory Interface Performance

The hard processor system (HPS) is available in Arria V SoC devices only.

Interface	Voltage (V)	HPS Hard Controller (MHz)
DDR3 SDRAM	1.5	533
	1.35	533
LPDDR2 SDRAM	1.2	333

---

(12) Not available as Altera® IP.

Features	Capability
PLL-based clock recovery	Superior jitter tolerance
Programmable serializer and deserializer (SERDES)	Flexible SERDES width
Equalization and pre-emphasis	• Arria V GX, GT, SX, and ST devices—Up to 14.37 dB of pre-emphasis and up to 4.7 dB of equalization • Arria V GZ devices—4-tap pre-emphasis and de-emphasis
Ring oscillator transmit PLLs	611 Mbps to 10.3125 Gbps
LC oscillator ATX transmit PLLs (Arria V GZ devices only)	600 Mbps to 12.5 Gbps
Input reference clock range	27 MHz to 710 MHz
Transceiver dynamic reconfiguration	Allows the reconfiguration of a single channel without affecting the operation of other channels

PCS Features

The Arria V core logic connects to the PCS through an 8, 10, 16, 20, 32, 40, 64, 66, or 67 bit interface, depending on the transceiver data rate and protocol. Arria V devices contain PCS hard IP to support PCIe Gen1, Gen2, and Gen3, GbE, Serial RapidIO (SRIO), GPON, and CPRI.

All other standard and proprietary protocols within the following speed ranges are also supported:

- 611 Mbps to 6.5536 Gbps—supported through the custom double-width mode (up to 6.5536 Gbps) and custom single-width mode (up to 3.75 Gbps) of the transceiver PCS hard IP.
- 6.5536 Gbps to 10.3125 Gbps—supported through dedicated 80 or 64 bit interface that bypass the PCS hard IP and connects the PMA directly to the core logic. In Arria V GZ, this is supported in the transceiver PCS hard IP.

Table 21: Transceiver PCS Features for Arria V GX, GT, ST, and SX Devices

PCS Support[13]	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
Custom single- and double-width modes	0.611 to ~6.5536	• Phase compensation FIFO • Byte serializer • 8B/10B encoder	• Word aligner • 8B/10B decoder • Byte deserializer • Phase compensation FIFO
SRIO	1.25 to 6.25		
Serial ATA	1.5, 3.0, 6.0		

---

[13] Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through the soft PCS.

PCS Support(13)	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
PCIe Gen1 (x1, x2, x4, x8)	2.5 and 5.0	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • PIPE 2.0 interface to the core logic	• Word aligner • 8B/10B decoder • Byte deserializer • Phase compensation FIFO • Rate match FIFO • PIPE 2.0 interface to the core logic
PCIe Gen2(14) (x1, x2, x4)			
GbE	1.25	• Phase compensation FIFO • Byte serializer • 8B/10B encoder	• Word aligner • 8B/10B decoder • Byte deserializer • Phase compensation FIFO • Rate match FIFO
XAUI(15)	3.125	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • XAUI state machine for bonding four channels	• Word aligner • 8B/10B decoder • Byte deserializer • Phase compensation FIFO • XAUI state machine for realigning four channels • Deskew FIFO circuitry
SDI	0.27(16), 1.485, 2.97	• Phase compensation FIFO • Byte serializer	• Byte deserializer • Phase compensation FIFO
GPON(17)	1.25 and 2.5		
CPRI(18)	0.6144 to 6.144	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • TX deterministic latency	• Word aligner • 8B/10B decoder • Byte deserializer • Phase compensation FIFO • RX deterministic latency

---

(13) Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through the soft PCS.

(14) PCIe Gen2 is supported only through the PCIe hard IP.

(15) XAUI is supported through the soft PCS.

(16) The 0.27 Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

(17) The GPON standard does not support burst mode.

(18) CPRI data rates above 6.5536 Gbps, such as 9.8304 Gbps, are supported through the soft PCS.

System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals to interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

HPS–FPGA AXI Bridges

The HPS–FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA®) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to slaves in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS–FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS–FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features. The SDRAM controller subsystem supports DDR2, DDR3, or LPDDR2 devices up to 4 Gb in density operating at up to 533 MHz (1066 Mbps data rate).

FPGA Configuration and Processor Booting

The FPGA fabric and HPS in the SoC are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power, or shut down the entire FPGA fabric to reduce total system power.

You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- You can power up both the HPS and the FPGA fabric together, configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

Note: Although the FPGA fabric and HPS are on separate power domains, the HPS must remain powered up during operation while the FPGA fabric can be powered up or down as required.

Related Information

- **Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines**
  Provides detailed information about power supply pin connection guidelines and power regulator sharing.
- **Arria V GZ Device Family Pin Connection Guidelines**
  Provides detailed information about power supply pin connection guidelines and power regulator sharing.

Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Qsys system integration tool in the Quartus Prime software.

For software development, the ARM-based SoC devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Altera SoCs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux, VxWorks®, and other operating systems is available for the SoCs. For more information on the operating systems support availability, contact the Altera sales team.

You can begin device-specific firmware and software development on the Altera SoC Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board that runs on a PC. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

Related Information

Altera Worldwide Sales Support

Dynamic and Partial Reconfiguration

The Arria V devices support dynamic reconfiguration and partial reconfiguration.

Dynamic Reconfiguration

The dynamic reconfiguration feature allows you to dynamically change the transceiver data rates, PMA settings, or protocols of a channel, without affecting data transfer on adjacent channels. This feature is ideal for applications that require on-the-fly multiprotocol or multirate support. You can reconfigure the PMA, PCS, and PCIe hard IP blocks with dynamic reconfiguration.

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompressio	Design Security	Partial Reconfiguratio (20)	Remote System Update
FPP	8 bits	125	—	Yes	Yes	—	Parallel flash loader
	16 bits	125	—	Yes	Yes	Yes(21)	
	32 bits(22)	100	—	Yes	Yes	—	
CvP (PCIe)	x1, x2, x4, and x8 lanes	—	—	Yes	Yes	Yes	—
JTAG	1 bit	33	33	—	—	—	—
Configuration via HPS	16 bits	125	—	Yes	Yes	Yes (21)	Parallel flash loader
	32 bits	100	—	Yes	Yes	—	

Instead of using an external flash or ROM, you can configure the Arria V devices through PCIe using CvP. The CvP mode offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. The Arria V CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

Note: Although Arria V GZ devices support PCIe Gen3, you can use only PCIe Gen1 and PCIe Gen2 for CvP configuration scheme.

Related Information

Configuration via Protocol (CvP) Implementation in Altera FPGAs User Guide
Provides more information about CvP.

Power Management

Leveraging the FPGA architectural features, process technology advancements, and transceivers that are designed for power efficiency, the Arria V devices consume less power than previous generation Arria V FPGAs:

- Total device core power consumption—less by up to 50%.
- Transceiver channel power consumption—less by up to 50%.

Additionally, Arria V devices contain several hard IP blocks, including PCIe Gen1, Gen2, and Gen3, GbE, SRIO, GPON, and CPRI protocols, that reduce logic resources and deliver substantial power savings of up to 25% less power than equivalent soft implementations.

---

(20) Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

(21) Supported at a maximum clock rate of 62.5 MHz.

(22) Arria V GZ only

Document Revision History

Date	Version	Changes
December 2015	2015.12.21	• Updated RoHS and optional suffix information in sample ordering code and available options diagrams for Arria V GX and GT devices. • Changed instances of *Quartus II* to *Quartus Prime*.
January 2015	2015.01.23	• Updated package dimension for Arria V GZ H780 package from 29 mm to 33 mm. • Updated dual-core ARM Cortex-A9 MPCore processor maximum frequency from 800 MHz to 1.05 GHz.
December 2013	2013.12.26	• 10-Gbps Ethernet (10GbE) PCS and Interlaken PCS are for Arria V GZ only. • Removed "Preliminary" texts from Ordering Code figures, Maximum Resources, Package Plan and I/O Vertical Migration tables. • Added link to **Altera Product Selector** for each device variant. • Added leaded package options. • Removed the note "The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs." for all PLLs in the Maximum Resource Counts table. • Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F896 package from 170 to 250. • Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F1152 package from 350 to 385. • Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F1517 package from 528 to 540. • Corrected LVDS Transmitter for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 devices from 121 to 120. • Added links to Altera's **External Memory Spec Estimator** tool to the topics listing the external memory interface performance. • Added x2 for PCIe Gen3, Gen 2, and Gen 1.
August 2013	2013.08.19	• Removed the note about the PCIe hard IP on the right side of the device in the F896 package of the Arria V GX variant. These devices do not have PCIe hard IP on the right side. • Added transceiver speed grade 6 to the available options of the Arria V SX variant. • Corrected the maximum LVDS transmitter channel counts for the Arria V GX A1 and A3 devices from 68 to 67. • Corrected the maximum FPGA GPIO count for Arria V ST D5 devices from 540 to 528.

Date	Version	Changes
June 2013	2013.06.03	- Removed statements about contacting Altera for SFF-8431 compliance requirements. Refer to the **Transceiver Architecture in Arria V Devices** chapter for the requirements.
May 2013	2013.05.06	- Moved all links to the Related Information section of respective topics for easy reference. - Added link to the known document issues in the Knowledge Base. - Updated the available options, maximum resource counts, and per package information for the Arria V SX and ST device variants. - Updated the variable DSP multipliers counts for the Arria V SX and ST device variants. - Clarified that partial reconfiguration is an advanced feature. Contact Altera for support of the feature. - Added footnote to clarify that MLAB 64 bits depth is available only for Arria V GZ devices. - Updated description about power-up sequence requirement for device migration to improve clarity.
January 2013	2013.01.11	- Added the L optional suffix to the Arria V GZ ordering code for the –I3 speed grade. - Added a note about the power-up sequence requirement if you plan to migrate your design from the Arria V GX A5 and A7, and Arria V GT C7 devices to other Arria V devices.
November 2012	2012.11.19	- Updated the summary of features. - Updated Arria V GZ information regarding 3.3 V I/O support. - Removed Arria V GZ engineering sample ordering code. - Updated the maximum resource counts for Arria V GX and GZ. - Updated Arria V ST ordering codes for transceiver count. - Updated transceiver counts for Arria V ST packages. - Added simplified floorplan diagrams for Arria V GZ, SX, and ST. - Added FPP x32 configuration mode for Arria V GZ only. - Updated CvP (PCIe) remote system update support information. - Added HPS external memory performance information. - Updated template.
October 2012	3.0	- Added Arria V GZ information. - Updated Table 1, Table 2, Table 3, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, and Table 21. - Added the “Arria V GZ” section. - Added Table 8, Table 9 and Table 22.

Date	Version	Changes
July 2012	2.1	• Added –I3 speed grade to Figure 1 for Arria V GX devices. • Updated the 6-Gbps transceiver speed from 6.553 Gbps to 6.5536 Gbps in Figure 3 and Figure 1.
June 2012	2.0	• Restructured the document. • Added the “Embedded Memory Capacity” and “Embedded Memory Configurations” sections. • Added Table 1, Table 3, Table 12, Table 15, and Table 16. • Updated Table 2, Table 4, Table 5, Table 6, Table 7, Table 8, Table 9, Table 10, Table 11, Table 13, Table 14, and Table 19. • Updated Figure 1, Figure 2, Figure 3, Figure 4, and Figure 8. • Updated the “FPGA Configuration and Processor Booting” and “Hardware and Software Development” sections. • Text edits throughout the document.
February 2012	1.3	• Updated Table 1–7 and Table 1–8. • Updated Figure 1–9 and Figure 1–10. • Minor text edits.
December 2011	1.2	Minor text edits.
November 2011	1.1	• Updated Table 1–1, Table 1–2, Table 1–3, Table 1–4, Table 1–6, Table 1–7, Table 1–9, and Table 1–10. • Added “SoC FPGA with HPS” section. • Updated “Clock Networks and PLL Clock Sources” and “Ordering Information” sections. • Updated Figure 1–5. • Added Figure 1–6. • Minor text edits.
August 2011	1.0	Initial release.