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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	925MHz
Primary Attributes	FPGA - 462K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA, FC (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5asxfb5h4f40c4n

Advantage	Supporting Feature
Lowest system cost	• Requires as few as four power supplies to operate • Available in thermal composite flip chip ball-grid array (BGA) packaging • Includes innovative features such as Configuration via Protocol (CvP), partial reconfiguration, and design security

Summary of Arria V Features

Table 2: Summary of Features for Arria V Devices

Feature	Description

Technology	• TSMC's 28-nm process technology:
	  • Arria V GX, GT, SX, and ST—28-nm low power (28LP) process
	  • Arria V GZ—28-nm high performance (28HP) process
	• Lowest static power in its class (less than 1.2 W for 500K logic elements (LEs) at 85°C junction under typical conditions)
	• 0.85 V, 1.1 V, or 1.15 V core nominal voltage

Packaging	• Thermal composite flip chip BGA packaging • Multiple device densities with identical package footprints for seamless migration between different device densities • Leaded(1), lead-free (Pb-free), and RoHS-compliant options
High-performance FPGA fabric	• Enhanced 8-input ALM with four registers • Improved routing architecture to reduce congestion and improve compilation time
Internal memory blocks	• M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC) (Arria V GX, GT, SX, and ST devices only) • M20K—20-Kb memory blocks with hard ECC (Arria V GZ devices only) • Memory logic array block (MLAB)-640-bit distributed LUTRAM where you can use up to 50% of the ALMs as MLAB memory

(1) Contact Altera for availability.

Feature	Description	

Embedded Hard IP blocks	Variable-precision DSP	• Native support for up to four signal processing precision levels:
		  • Three 9 x 9, two 18 x 18, or one 27 x 27 multiplier in the same variable-precision DSP block
		  • One 36 x 36 multiplier using two variable-precision DSP blocks (Arria V GZ devices only)
		• 64-bit accumulator and cascade for systolic finite impulse responses (FIRs)
		• Embedded internal coefficient memory
		• Preadder/subtractor for improved efficiency

	Memory controller (Arria V GX, GT, SX, and ST only)	DDR3 and DDR2

	Embedded transceiver I/O	• Custom implementation:
		  • Arria V GX and SX devices—up to 6.5536 Gbps
		  • Arria V GT and ST devices—up to 10.3125 Gbps
		  • Arria V GZ devices—up to 12.5 Gbps
		• PCI Express® (PCIe®) Gen2 (x1, x2, or x4) and Gen1 (x1, x2, x4, or x8) hard IP with multifunction support, endpoint, and root port
		• PCIe Gen3 (x1, x2, x4, or x8) support (Arria V GZ only)
		• Gbps Ethernet (GbE) and XAUI physical coding sublayer (PCS)
		• Common Public Radio Interface (CPRI) PCS
		• Gigabit-capable passive optical network (GPON) PCS
		• 10-Gbps Ethernet (10GbE) PCS (Arria V GZ only)
		• Serial RapidIO® (SRIO) PCS
		• Interlaken PCS (Arria V GZ only)

Clock networks	• Up to 650 MHz global clock network • Global, quadrant, and peripheral clock networks • Clock networks that are not used can be powered down to reduce dynamic power	
Phase-locked loops (PLLs)	• High-resolution fractional PLLs • Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB) • Integer mode and fractional mode • LC oscillator ATX transmitter PLLs (Arria V GZ only)	

Feature	Description
FPGA General-purpose I/Os (GPIOs)	• 1.6 Gbps LVDS receiver and transmitter • 800 MHz/1.6 Gbps external memory interface • On-chip termination (OCT) • 3.3 V support (2)
External Memory Interface	Memory interfaces with low latency: • Hard memory controller-up to 1.066 Gbps • Soft memory controller-up to 1.6 Gbps
Low-power high-speed serial interface	• 600 Mbps to 12.5 Gbps integrated transceiver speed • Less than 105 mW per channel at 6 Gbps, less than 165 mW per channel at 10 Gbps, and less than 170 mW per channel at 12.5 Gbps • Transmit pre-emphasis and receiver equalization • Dynamic partial reconfiguration of individual channels • Physical medium attachment (PMA) with soft PCS that supports 9.8304 Gbps CPRI (Arria V GT and ST only) • PMA with hard PCS that supports up to 9.8 Gbps CPRI (Arria V GZ only) • Hard PCS that supports 10GBASE-R and 10GBASE-KR (Arria V GZ only)
HPS (Arria V SX and ST devices only)	• Dual-core ARM Cortex-A9 MPCore processor—up to 1.05 GHz maximum frequency with support for symmetric and asymmetric multiprocessing • Interface peripherals—10/100/1000 Ethernet media access control (EMAC), USB 2.0 On-The-GO (OTG) controller, quad serial peripheral interface (QSPI) flash controller, NAND flash controller, Secure Digital/MultiMediaCard (SD/MMC) controller, UART, serial peripheral interface (SPI), I2C interface, and up to 85 HPS GPIO interfaces • System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers • On-chip RAM and boot ROM • HPS–FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa • FPGA-to-HPS SDRAM controller subsystem—provides a configurable interface to the multiport front end (MPFE) of the HPS SDRAM controller • ARM CoreSight™ JTAG debug access port, trace port, and on-chip trace storage

(2) Arria V GZ devices support 3.3 V with a 3.0 V V_{CCIO}.

Feature	Description
Configuration	• Tamper protection-comprehensive design protection to protect your valuable IP investments • Enhanced advanced encryption standard (AES) design security features • CvP • Partial and dynamic reconfiguration of the FPGA • Active serial (AS) x1 and x4, passive serial (PS), JTAG, and fast passive parallel (FPP) x8, x16, and x32 (Arria V GZ) configuration options • Remote system upgrade

Arria V Device Variants and Packages

Table 3: Device Variants for the Arria V Device Family

Variant	Description
Arria V GX	FPGA with integrated 6.5536 Gbps transceivers that provides bandwidth, cost, and power levels that are optimized for high-volume data and signal-processing applications
Arria V GT	FPGA with integrated 10.3125 Gbps transceivers that provides enhanced high-speed serial I/O bandwidth for cost-sensitive data and signal processing applications
Arria V GZ	FPGA with integrated 12.5 Gbps transceivers that provides enhanced high-speed serial I/O bandwidth for high-performance and cost-sensitive data and signal processing applications
Arria V SX	SoC with integrated ARM-based HPS and 6.5536 Gbps transceivers
Arria V ST	SoC with integrated ARM-based HPS and 10.3125 Gbps transceivers

Arria V GX

This section provides the available options, maximum resource counts, and package plan for the Arria V GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

Related Information

Altera Product Selector
Provides the latest information about Altera products.

Resource		Member Code							
		A1	A3	A5	A7	B1	B3	B5	B7
6 Gbps Transceiver		9	9	24	24	24	24	36	36
GPIO(3)		416	416	544	544	704	704	704	704
LVDS	Transmitter	67	67	120	120	160	160	160	160
	Receiver	80	80	136	136	176	176	176	176
PCIe Hard IP Block		1	1	2	2	2	2	2	2
Hard Memory Controller		2	2	4	4	4	4	4	4

Related Information

High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook
Provides the number of LVDS channels in each device package.

Package Plan

Table 5: Package Plan for Arria V GX Devices

Member Code	F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)		F1517 (40 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
A1	336	9	416	9	—	—	—	—
A3	336	9	416	9	—	—	—	—
A5	336	9	384	18	544	24	—	—
A7	336	9	384	18	544	24	—	—
B1	—	—	384	18	544	24	704	24
B3	—	—	384	18	544	24	704	24
B5	—	—	—	—	544	24	704	36
B7	—	—	—	—	544	24	704	36

Arria V GT

This section provides the available options, maximum resource counts, and package plan for the Arria V GT devices.

(3) The number of GPIOs does not include transceiver I/Os. In the Quartus® Prime software, the number of user I/Os includes transceiver I/Os.

and eighteen 10-Gbps, twelve 6-Gbps and sixteen 10-Gbps, fifteen 6-Gbps and fourteen 10-Gbps, or up to thirty-six 6-Gbps with no 10-Gbps channels.

Arria V GZ

This section provides the available options, maximum resource counts, and package plan for the Arria V GZ devices.

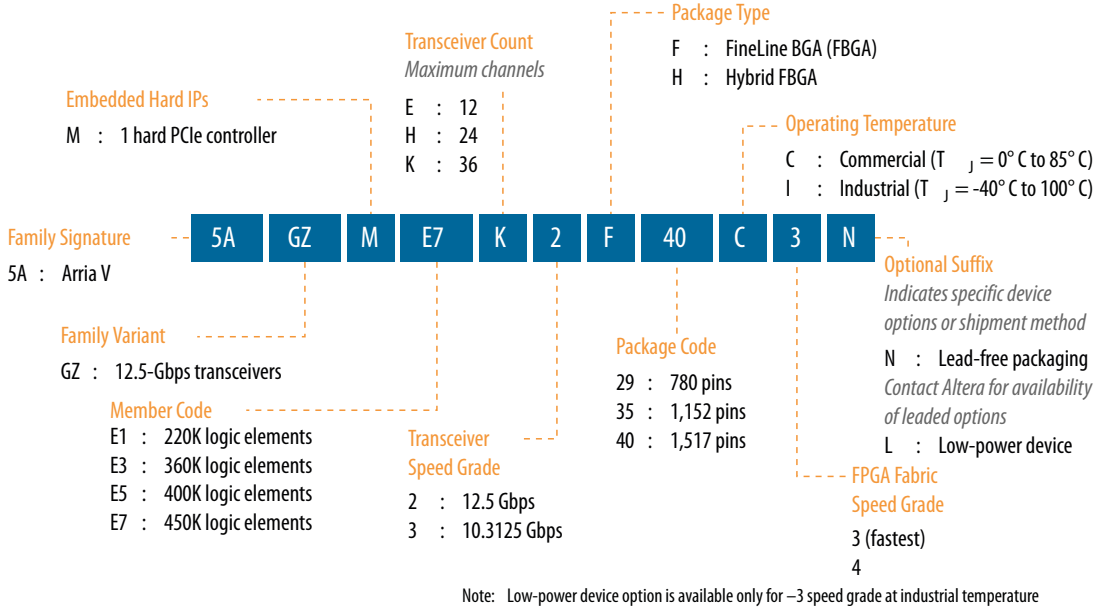
The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

Related Information

Altera Product Selector
Provides the latest information about Altera products.

Available Options

Figure 3: Sample Ordering Code and Available Options for Arria V GZ Devices



Note: Low-power device option is available only for –3 speed grade at industrial temperature

Maximum Resources

Table 8: Maximum Resource Counts for Arria V GZ Devices

Resource	Member Code			
	E1	E3	E5	E7
Logic Elements (LE) (K)	220	360	400	450
ALM	83,020	135,840	150,960	169,800
Register	332,080	543,360	603,840	679,200

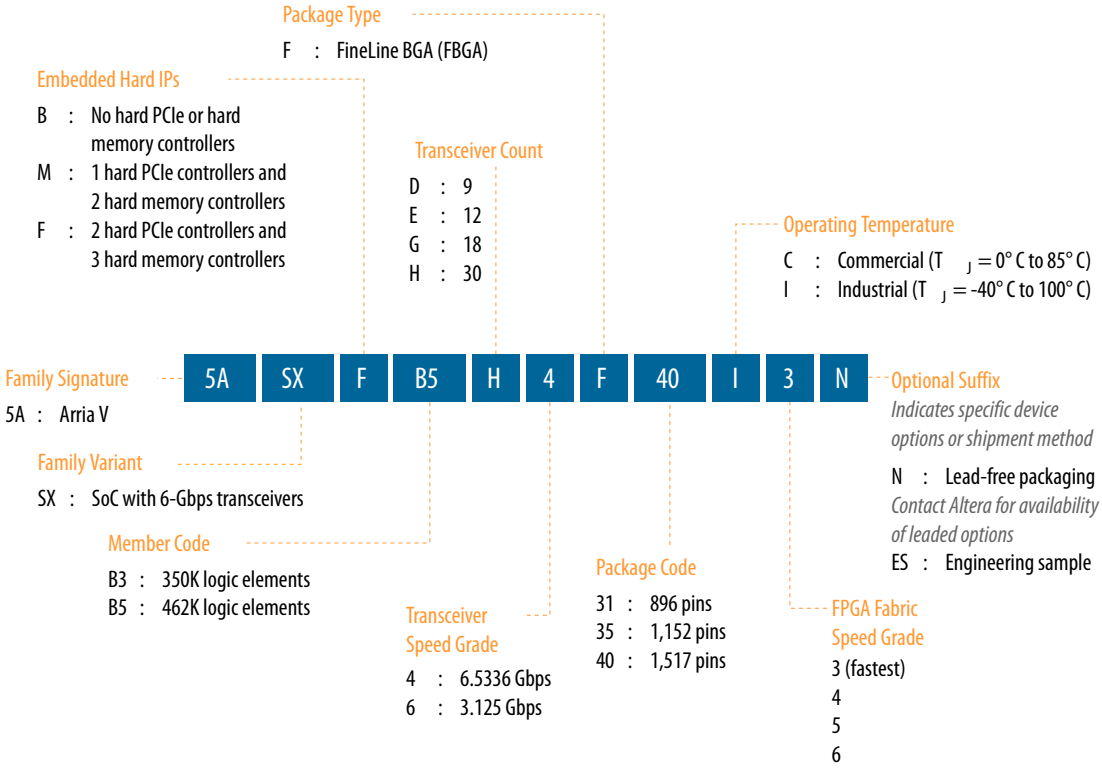
Related Information

Altera Product Selector
Provides the latest information about Altera products.

Available Options

Figure 4: Sample Ordering Code and Available Options for Arria V SX Devices

The –3 FPGA fabric speed grade is available only for industrial temperature devices.



Maximum Resources

Table 10: Maximum Resource Counts for Arria V SX Devices

Resource		Member Code	
		B3	B5
Logic Elements (LE) (K)		350	462
ALM		132,075	174,340
Register		528,300	697,360
Memory (Kb)	M10K	17,290	22,820
	MLAB	2,014	2,658
Variable-precision DSP Block		809	1,090
18 x 18 Multiplier		1,618	2,180

Resource		Member Code	
		B3	B5
FPGA PLL		14	14
HPS PLL		3	3
6 Gbps Transceiver		30	30
FPGA GPIO[8]		540	540
HPS I/O		208	208
LVDS	Transmitter	120	120
	Receiver	136	136
PCIe Hard IP Block		2	2
FPGA Hard Memory Controller		3	3
HPS Hard Memory Controller		1	1
ARM Cortex-A9 MPCore Processor		Dual-core	Dual-core

Related Information

High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook

Provides the number of LVDS channels in each device package.

Package Plan

Table 11: Package Plan for Arria V SX Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	F896 (31 mm)			F1152 (35 mm)			F1517 (40 mm)		
	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR
B3	250	208	12	385	208	18	540	208	30
B5	250	208	12	385	208	18	540	208	30

Arria V ST

This section provides the available options, maximum resource counts, and package plan for the Arria V ST devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

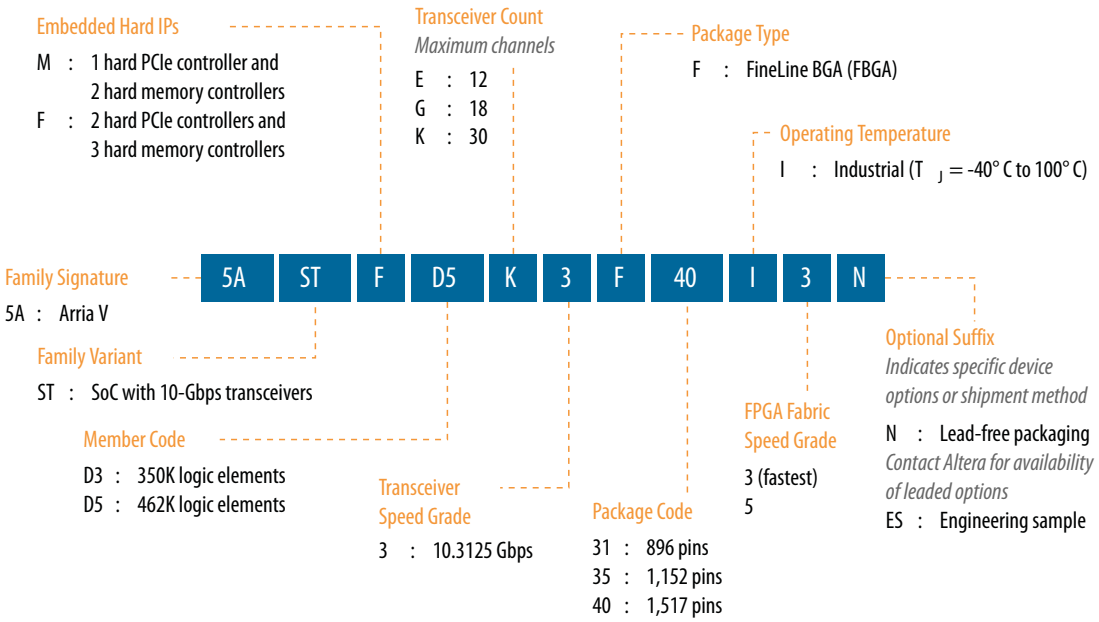
[8] The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

Related Information

Altera Product Selector
Provides the latest information about Altera products.

Available Options

Figure 5: Sample Ordering Code and Available Options for Arria V ST Devices



Maximum Resources

Table 12: Maximum Resource Counts for Arria V ST Devices

Resource		Member Code	
		D3	D5
Logic Elements (LE) (K)		350	462
ALM		132,075	174,340
Register		528,300	697,360
Memory (Kb)	M10K	17,290	22,820
	MLAB	2,014	2,658
Variable-precision DSP Block		809	1,090
18 x 18 Multiplier		1,618	2,180
FPGA PLL		14	14
HPS PLL		3	3
Transceiver	6-Gbps	30	30
	10-Gbps[9]	16	16

Variable-Precision DSP Block

Arria V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18, 27 x 27, and 36 x 36 bits natively
- A 64-bit accumulator
- Double accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Dynamic coefficients
- 18-bit internal coefficient register banks
- Enhanced independent multiplier operation
- Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Quartus Prime design software

Table 14: Variable-Precision DSP Block Configurations for Arria V Devices

Usage Example	Multiplier Size (Bit)	DSP Block Resource
Low precision fixed point for video applications	Three 9 x 9	1
Medium precision fixed point in FIR filters	Two 18 x 18	1
FIR filters	Two 18 x 18 with accumulate	1
Single-precision floating-point implementations	One 27 x 27	1
Very high precision fixed point implementations	One 36 x 36	2

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 18, or one 27 x 27 multipliers. Using two DSP block resources, you can also configure a 36 x 36 multiplier for high-precision applications. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

Types of Embedded Memory

The Arria V devices contain two types of memory blocks:

- 20 Kb M20K or 10 Kb M10K blocks—blocks of dedicated memory resources. The M20K and M10K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Arria V devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB. You can also configure these ALMs, in Arria V GZ devices, as ten 64 x 1 blocks, giving you one 64 x 10 simple dual-port SRAM block per MLAB.

Embedded Memory Capacity in Arria V Devices

Table 16: Embedded Memory Capacity and Distribution in Arria V Devices

Variant	Member Code	M20K		M10K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Arria V GX	A1	—	—	800	8,000	741	463	8,463
	A3	—	—	1,051	10,510	1538	961	11,471
	A5	—	—	1,180	11,800	1877	1,173	12,973
	A7	—	—	1,366	13,660	2317	1,448	15,108
	B1	—	—	1,510	15,100	2964	1,852	16,952
	B3	—	—	1,726	17,260	3357	2,098	19,358
	B5	—	—	2,054	20,540	4052	2,532	23,072
	B7	—	—	2,414	24,140	4650	2,906	27,046
Arria V GT	C3	—	—	1,051	10,510	1538	961	11,471
	C7	—	—	1,366	13,660	2317	1,448	15,108
	D3	—	—	1,726	17,260	3357	2,098	19,358
	D7	—	—	2,414	24,140	4650	2,906	27,046
Arria V GZ	E1	585	11,700	—	—	4,151	2,594	14,294
	E3	957	19,140	—	—	6,792	4,245	23,385
	E5	1,440	28,800	—	—	7,548	4,718	33,518
	E7	1,700	34,000	—	—	8,490	5,306	39,306
Arria V SX	B3	—	—	1,729	17,290	3223	2,014	19,304
	B5	—	—	2,282	22,820	4253	2,658	25,478

Figure 9: Device Chip Overview for Arria V GX and GT Devices

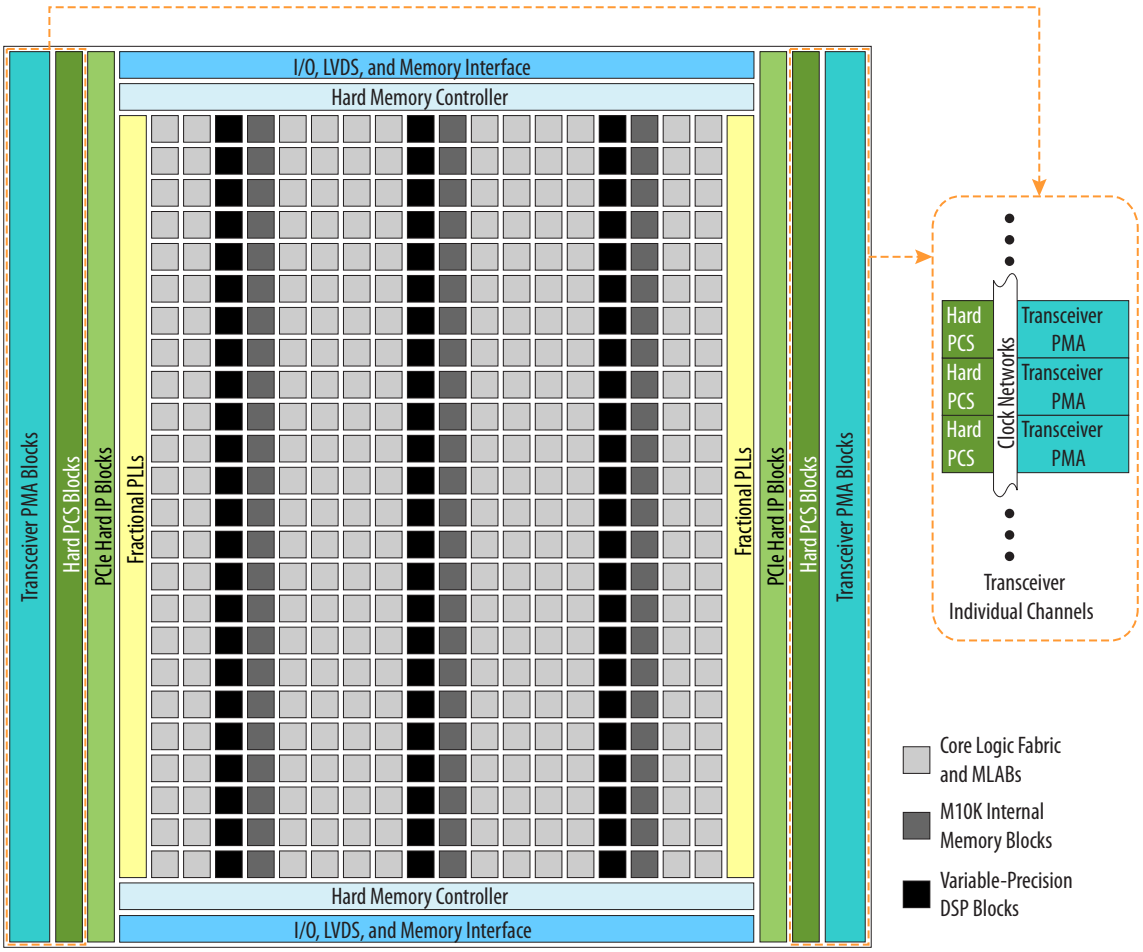


Figure 10: Device Chip Overview for Arria V GZ Devices

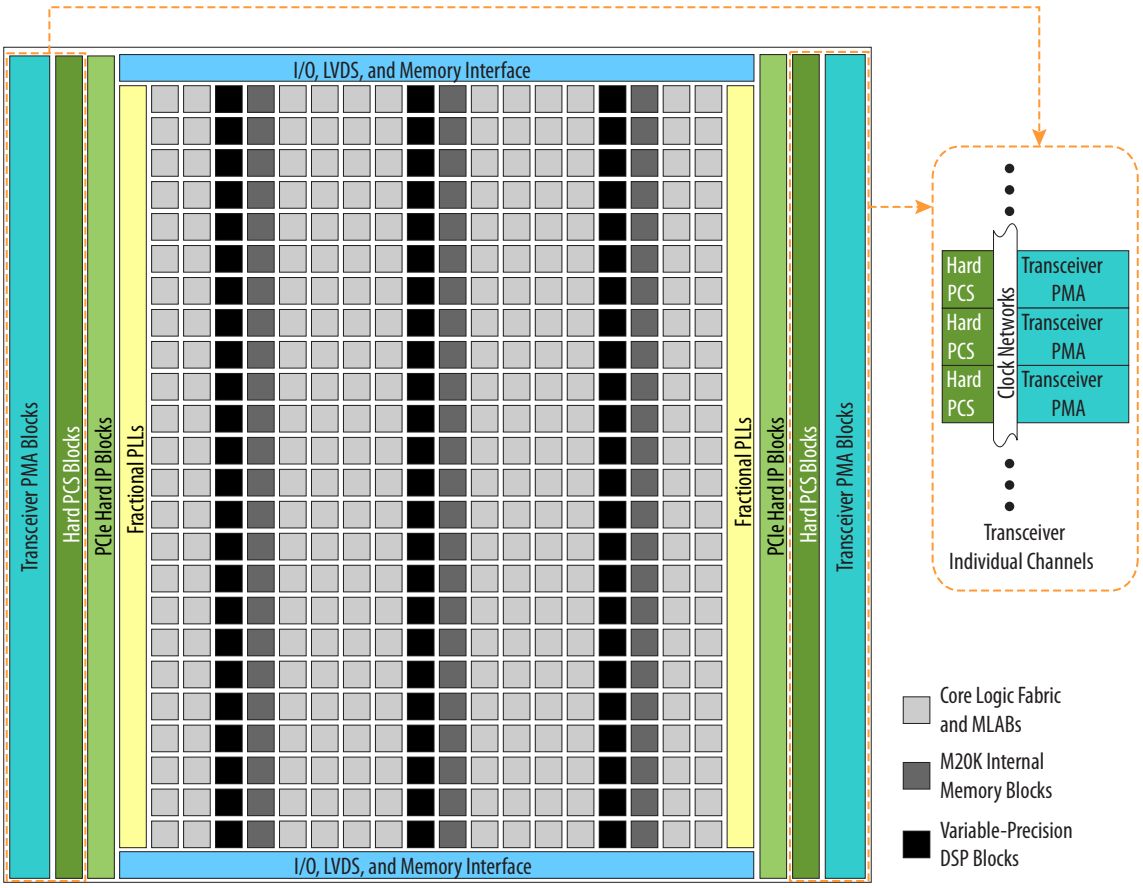
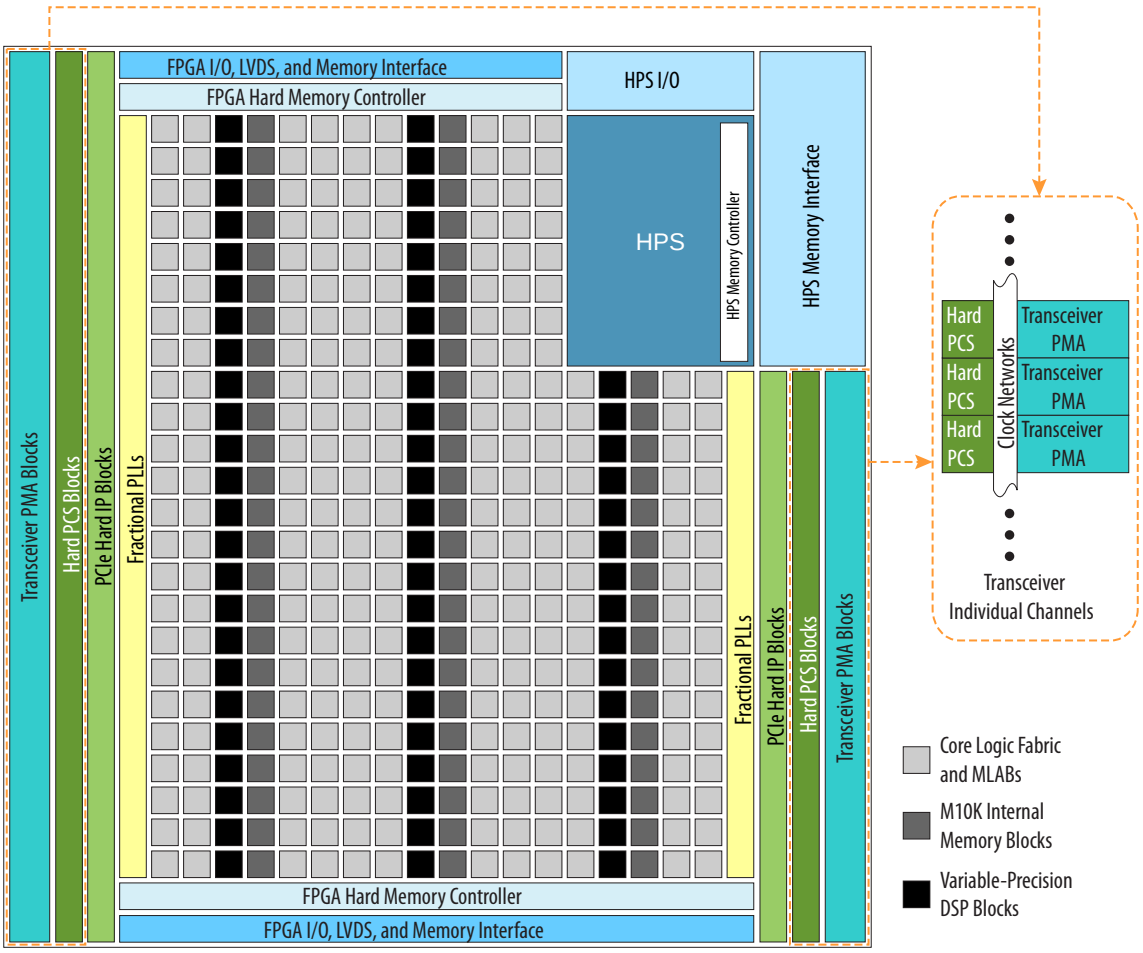


Figure 11: Device Chip Overview for Arria V SX and ST Devices



PMA Features

To prevent core and I/O noise from coupling into the transceivers, the PMA block is isolated from the rest of the chip—ensuring optimal signal integrity. For the transceivers, you can use the channel PLL of an unused receiver PMA as an additional transmit PLL.

Table 20: PMA Features of the Transceivers in Arria V Devices

Features	Capability
Backplane support	• Arria V GX, GT, SX, and ST devices—Driving capability at 6.5536 Gbps with up to 25 dB channel loss • Arria V GZ devices—Driving capability at 12.5 Gbps with up to 16 dB channel loss
Chip-to-chip support	• Arria V GX, GT, SX, and ST devices—Up to 10.3125 Gbps • Arria V GZ devices—Up to 12.5 Gbps

Table 22: Transceiver PCS Features for Arria V GZ Devices

Protocol	Data Rates (Gbps)	Transmitter Data Path Features	Receiver Data Path Features
Custom PHY	0.6 to 9.80	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • Bit-slip • Channel bonding	• Word aligner • Deskew FIFO • Rate match FIFO • 8B/10B decoder • Byte deserializer • Byte ordering
GPON	1.25 and 2.5		
Custom 10G PHY	9.98 to 12.5	• TX FIFO • Gear box • Bit-slip	• RX FIFO • Gear box
PCIe Gen1 (x1, x2 x4, x8)	2.5 and 5.0	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • Bit-slip • Channel bonding • PIPE 2.0 interface to core logic	• Word aligner • Deskew FIFO • Rate match FIFO • 8B/10B decoder • Byte deserializer, • Byte ordering • PIPE 2.0 interface to core logic
PCIe Gen2 (x1, x2, x4, x8)			
PCIe Gen3 (x1, x2, x4, x8)	8.0	• Phase compensation FIFO • 128B/130B encoder • Scrambler • Gear box • Bit-slip	• Block synchronization • Rate match FIFO • 128B/130B decoder • Descrambler • Phase compensation FIFO
10GbE	10.3125	• TX FIFO • 64B/66B encoder • Scrambler • Gear box	• RX FIFO • 64B/66B decoder • Descrambler • Block synchronization • Gear box
Interlaken	3.125 to 12.5	• TX FIFO • Frame generator • CRC-32 generator • Scrambler • Disparity generator • Gear box	• RX FIFO • Frame generator • CRC-32 checker • Frame decoder • Descrambler • Disparity checker • Block synchronization • Gear box

Protocol	Data Rates (Gbps)	Transmitter Data Path Features	Receiver Data Path Features
40GBASE-R Ethernet	4 x 10.3125	• TX FIFO • 64B/66B encoder • Scrambler • Alignment marker insertion • Gearbox • Block stripper	• RX FIFO • 64B/66B decoder • Descrambler • Lane reorder • Deskew • Alignment marker lock • Block synchronization • Gear box • Destripper
100GBASE-R Ethernet	10 x 10.3125		
40G and 100G OTN	(4 +1) x 11.3 (10 +1) x 11.3	• TX FIFO • Channel bonding • Byte serializer	• RX FIFO • Lane deskew • Byte deserializer
GbE	1.25	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • Bit-slip • Channel bonding • GbE state machine	• Word aligner • Deskew FIFO • Rate match FIFO • 8B/10B decoder • Byte deserializer • Byte ordering • GbE state machine
XAUI	3.125 to 4.25	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • Bit-slip • Channel bonding • XAUI state machine for bonding four channels	• Word aligner • Deskew FIFO • Rate match FIFO • 8B/10B decoder • Byte deserializer • Byte ordering • XAUI state machine for realigning four channels
SRIO	1.25 to 6.25	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • Bit-slip • Channel bonding • SRIO V2.1-compliant x2 and x4 channel bonding	• Word aligner • Deskew FIFO • Rate match FIFO • 8B/10B decoder • Byte deserializer • Byte ordering • SRIO V2.1-compliant x2 and x4 deskew state machine

SoC with HPS

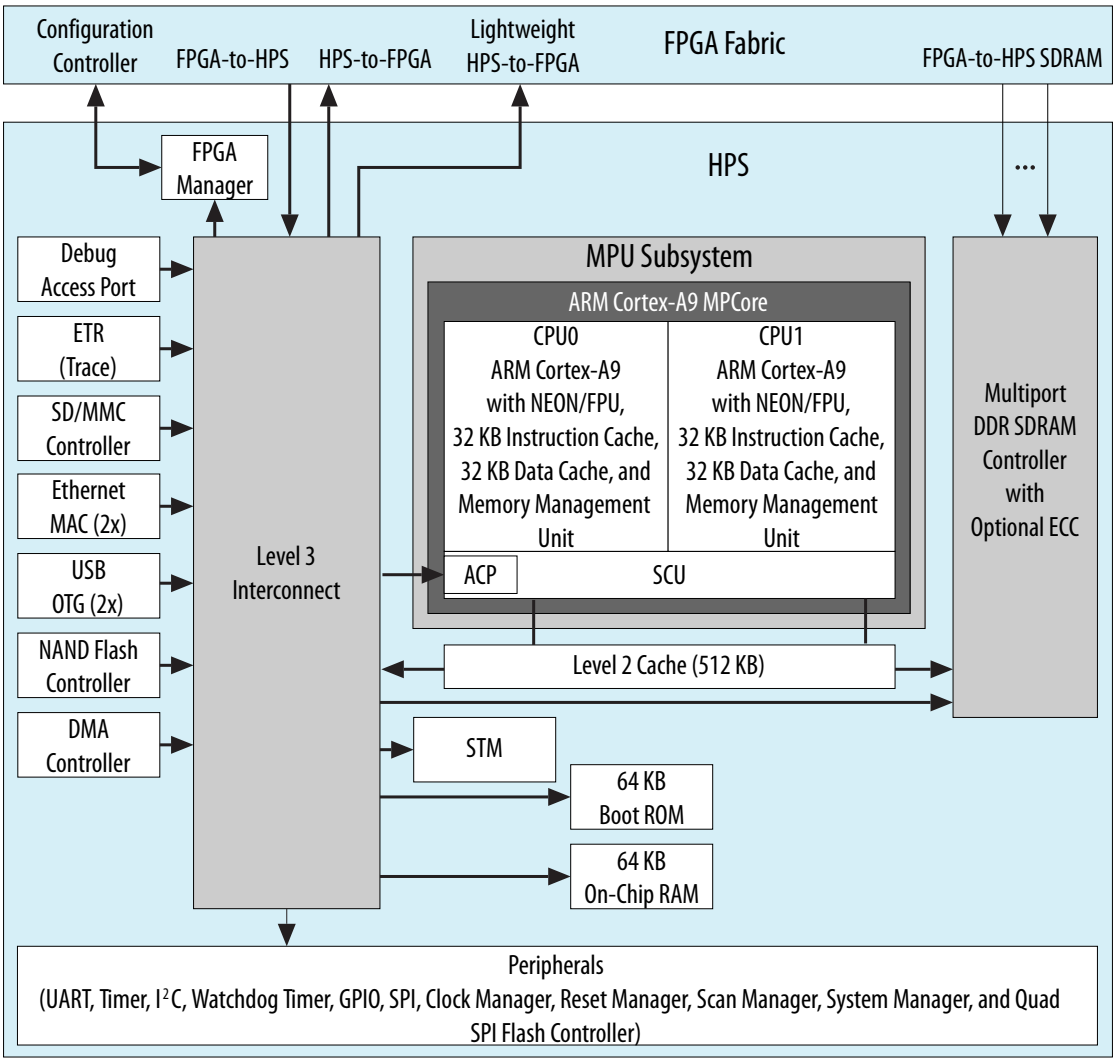
Each SoC combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

HPS Features

The HPS consists of a dual-core ARM Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in the following figure.

Figure 12: HPS with Dual-Core ARM Cortex-A9 MPCore Processor



System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals to interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

HPS–FPGA AXI Bridges

The HPS–FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA®) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to slaves in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS–FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS–FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features. The SDRAM controller subsystem supports DDR2, DDR3, or LPDDR2 devices up to 4 Gb in density operating at up to 533 MHz (1066 Mbps data rate).

FPGA Configuration and Processor Booting

The FPGA fabric and HPS in the SoC are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power, or shut down the entire FPGA fabric to reduce total system power.

Date	Version	Changes
June 2013	2013.06.03	• Removed statements about contacting Altera for SFF-8431 compliance requirements. Refer to the **Transceiver Architecture in Arria V Devices** chapter for the requirements.
May 2013	2013.05.06	• Moved all links to the Related Information section of respective topics for easy reference. • Added link to the known document issues in the Knowledge Base. • Updated the available options, maximum resource counts, and per package information for the Arria V SX and ST device variants. • Updated the variable DSP multipliers counts for the Arria V SX and ST device variants. • Clarified that partial reconfiguration is an advanced feature. Contact Altera for support of the feature. • Added footnote to clarify that MLAB 64 bits depth is available only for Arria V GZ devices. • Updated description about power-up sequence requirement for device migration to improve clarity.
January 2013	2013.01.11	• Added the L optional suffix to the Arria V GZ ordering code for the –I3 speed grade. • Added a note about the power-up sequence requirement if you plan to migrate your design from the Arria V GX A5 and A7, and Arria V GT C7 devices to other Arria V devices.
November 2012	2012.11.19	• Updated the summary of features. • Updated Arria V GZ information regarding 3.3 V I/O support. • Removed Arria V GZ engineering sample ordering code. • Updated the maximum resource counts for Arria V GX and GZ. • Updated Arria V ST ordering codes for transceiver count. • Updated transceiver counts for Arria V ST packages. • Added simplified floorplan diagrams for Arria V GZ, SX, and ST. • Added FPP x32 configuration mode for Arria V GZ only. • Updated CvP (PCIe) remote system update support information. • Added HPS external memory performance information. • Updated template.
October 2012	3.0	• Added Arria V GZ information. • Updated Table 1, Table 2, Table 3, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, and Table 21. • Added the “Arria V GZ” section. • Added Table 8, Table 9 and Table 22.

Date	Version	Changes
July 2012	2.1	• Added –I3 speed grade to Figure 1 for Arria V GX devices. • Updated the 6-Gbps transceiver speed from 6.553 Gbps to 6.5536 Gbps in Figure 3 and Figure 1.
June 2012	2.0	• Restructured the document. • Added the "Embedded Memory Capacity" and "Embedded Memory Configurations" sections. • Added Table 1, Table 3, Table 12, Table 15, and Table 16. • Updated Table 2, Table 4, Table 5, Table 6, Table 7, Table 8, Table 9, Table 10, Table 11, Table 13, Table 14, and Table 19. • Updated Figure 1, Figure 2, Figure 3, Figure 4, and Figure 8. • Updated the "FPGA Configuration and Processor Booting" and "Hardware and Software Development" sections. • Text edits throughout the document.
February 2012	1.3	• Updated Table 1–7 and Table 1–8. • Updated Figure 1–9 and Figure 1–10. • Minor text edits.
December 2011	1.2	Minor text edits.
November 2011	1.1	• Updated Table 1–1, Table 1–2, Table 1–3, Table 1–4, Table 1–6, Table 1–7, Table 1–9, and Table 1–10. • Added "SoC FPGA with HPS" section. • Updated "Clock Networks and PLL Clock Sources" and "Ordering Information" sections. • Updated Figure 1–5. • Added Figure 1–6. • Minor text edits.
August 2011	1.0	Initial release.