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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	700MHz
Primary Attributes	FPGA - 462K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA, FC (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5asxfb5h6f40c6nes

Advantage	Supporting Feature
Lowest system cost	• Requires as few as four power supplies to operate • Available in thermal composite flip chip ball-grid array (BGA) packaging • Includes innovative features such as Configuration via Protocol (CvP), partial reconfiguration, and design security

Summary of Arria V Features

Table 2: Summary of Features for Arria V Devices

Feature	Description

Technology	• TSMC's 28-nm process technology:
	  • Arria V GX, GT, SX, and ST—28-nm low power (28LP) process
	  • Arria V GZ—28-nm high performance (28HP) process
	• Lowest static power in its class (less than 1.2 W for 500K logic elements (LEs) at 85°C junction under typical conditions)
	• 0.85 V, 1.1 V, or 1.15 V core nominal voltage

Packaging	• Thermal composite flip chip BGA packaging • Multiple device densities with identical package footprints for seamless migration between different device densities • Leaded(1), lead-free (Pb-free), and RoHS-compliant options
High-performance FPGA fabric	• Enhanced 8-input ALM with four registers • Improved routing architecture to reduce congestion and improve compilation time
Internal memory blocks	• M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC) (Arria V GX, GT, SX, and ST devices only) • M20K—20-Kb memory blocks with hard ECC (Arria V GZ devices only) • Memory logic array block (MLAB)-640-bit distributed LUTRAM where you can use up to 50% of the ALMs as MLAB memory

(1) Contact Altera for availability.

Feature	Description
FPGA General-purpose I/Os (GPIOs)	• 1.6 Gbps LVDS receiver and transmitter • 800 MHz/1.6 Gbps external memory interface • On-chip termination (OCT) • 3.3 V support (2)
External Memory Interface	Memory interfaces with low latency: • Hard memory controller-up to 1.066 Gbps • Soft memory controller-up to 1.6 Gbps
Low-power high-speed serial interface	• 600 Mbps to 12.5 Gbps integrated transceiver speed • Less than 105 mW per channel at 6 Gbps, less than 165 mW per channel at 10 Gbps, and less than 170 mW per channel at 12.5 Gbps • Transmit pre-emphasis and receiver equalization • Dynamic partial reconfiguration of individual channels • Physical medium attachment (PMA) with soft PCS that supports 9.8304 Gbps CPRI (Arria V GT and ST only) • PMA with hard PCS that supports up to 9.8 Gbps CPRI (Arria V GZ only) • Hard PCS that supports 10GBASE-R and 10GBASE-KR (Arria V GZ only)
HPS (Arria V SX and ST devices only)	• Dual-core ARM Cortex-A9 MPCore processor—up to 1.05 GHz maximum frequency with support for symmetric and asymmetric multiprocessing • Interface peripherals—10/100/1000 Ethernet media access control (EMAC), USB 2.0 On-The-GO (OTG) controller, quad serial peripheral interface (QSPI) flash controller, NAND flash controller, Secure Digital/MultiMediaCard (SD/MMC) controller, UART, serial peripheral interface (SPI), I2C interface, and up to 85 HPS GPIO interfaces • System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers • On-chip RAM and boot ROM • HPS–FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa • FPGA-to-HPS SDRAM controller subsystem—provides a configurable interface to the multiport front end (MPFE) of the HPS SDRAM controller • ARM CoreSight™ JTAG debug access port, trace port, and on-chip trace storage

(2) Arria V GZ devices support 3.3 V with a 3.0 V V_{CCIO}.

Feature	Description
Configuration	• Tamper protection-comprehensive design protection to protect your valuable IP investments • Enhanced advanced encryption standard (AES) design security features • CvP • Partial and dynamic reconfiguration of the FPGA • Active serial (AS) x1 and x4, passive serial (PS), JTAG, and fast passive parallel (FPP) x8, x16, and x32 (Arria V GZ) configuration options • Remote system upgrade

Arria V Device Variants and Packages

Table 3: Device Variants for the Arria V Device Family

Variant	Description
Arria V GX	FPGA with integrated 6.5536 Gbps transceivers that provides bandwidth, cost, and power levels that are optimized for high-volume data and signal-processing applications
Arria V GT	FPGA with integrated 10.3125 Gbps transceivers that provides enhanced high-speed serial I/O bandwidth for cost-sensitive data and signal processing applications
Arria V GZ	FPGA with integrated 12.5 Gbps transceivers that provides enhanced high-speed serial I/O bandwidth for high-performance and cost-sensitive data and signal processing applications
Arria V SX	SoC with integrated ARM-based HPS and 6.5536 Gbps transceivers
Arria V ST	SoC with integrated ARM-based HPS and 10.3125 Gbps transceivers

Arria V GX

This section provides the available options, maximum resource counts, and package plan for the Arria V GX devices.

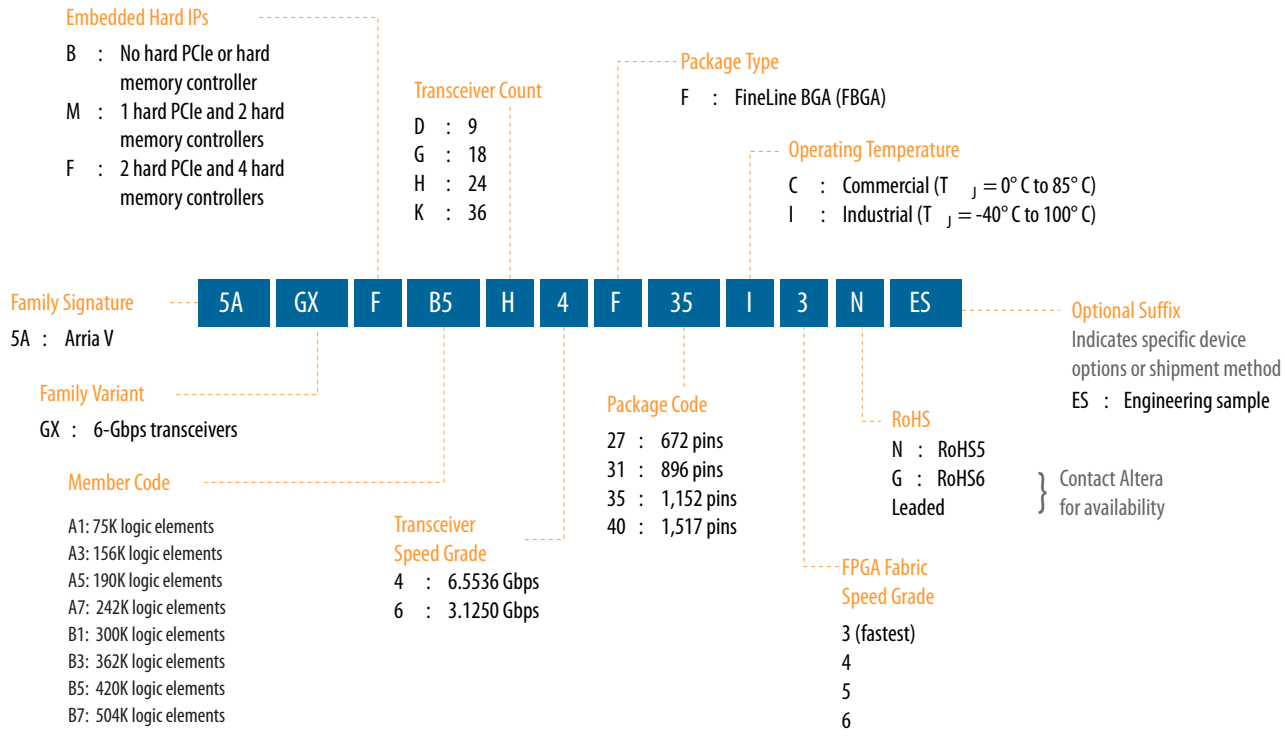
The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

Related Information

Altera Product Selector
Provides the latest information about Altera products.

Available Options

Figure 1: Sample Ordering Code and Available Options for Arria V GX Devices



Maximum Resources

Table 4: Maximum Resource Counts for Arria V GX Devices

Resource		Member Code							
		A1	A3	A5	A7	B1	B3	B5	B7
Logic Elements (LE) (K)		75	156	190	242	300	362	420	504
ALM		28,302	58,900	71,698	91,680	113,208	136,880	158,491	190,240
Register		113,208	235,600	286,792	366,720	452,832	547,520	633,964	760,960
Memory (Kb)	M10K	8,000	10,510	11,800	13,660	15,100	17,260	20,540	24,140
	MLAB	463	961	1,173	1,448	1,852	2,098	2,532	2,906
Variable-precision DSP Block		240	396	600	800	920	1,045	1,092	1,156
18 x 18 Multiplier		480	792	1,200	1,600	1,840	2,090	2,184	2,312
PLL		10	10	12	12	12	12	16	16

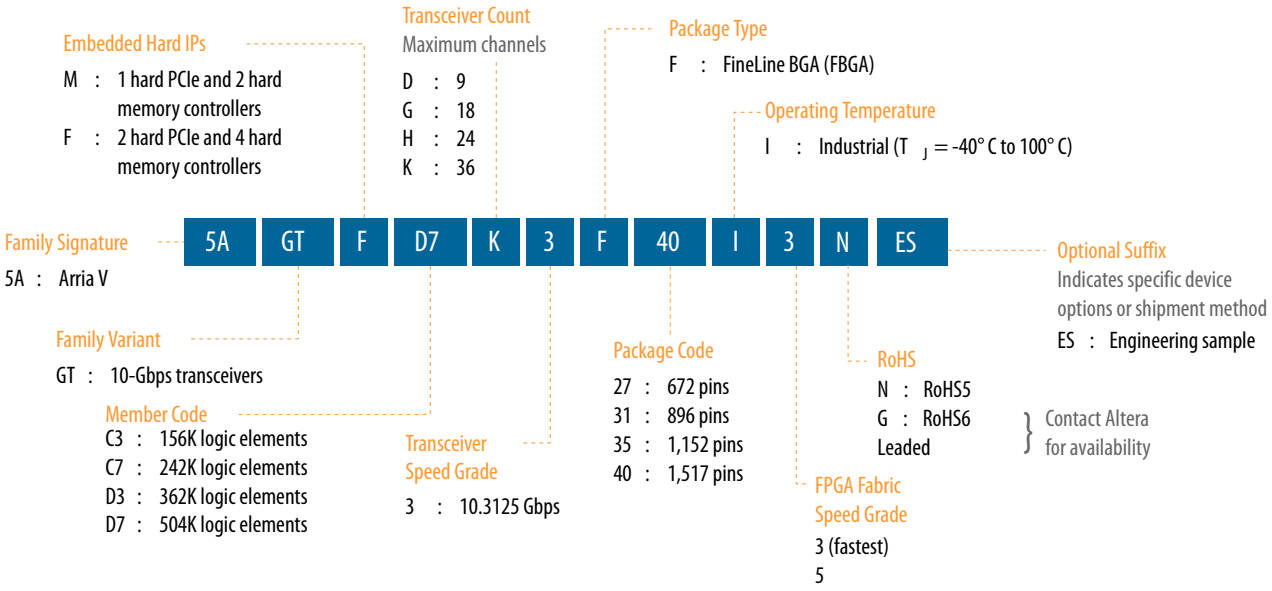
The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

Related Information

Altera Product Selector
Provides the latest information about Altera products.

Available Options

Figure 2: Sample Ordering Code and Available Options for Arria V GT Devices



Maximum Resources

Table 6: Maximum Resource Counts for Arria V GT Devices

Resource		Member Code			
		C3	C7	D3	D7
Logic Elements (LE) (K)		156	242	362	504
ALM		58,900	91,680	136,880	190,240
Register		235,600	366,720	547,520	760,960
Memory (Kb)	M10K	10,510	13,660	17,260	24,140
	MLAB	961	1,448	2,098	2,906
Variable-precision DSP Block		396	800	1,045	1,156
18 x 18 Multiplier		792	1,600	2,090	2,312
PLL		10	12	12	16

and eighteen 10-Gbps, twelve 6-Gbps and sixteen 10-Gbps, fifteen 6-Gbps and fourteen 10-Gbps, or up to thirty-six 6-Gbps with no 10-Gbps channels.

Arria V GZ

This section provides the available options, maximum resource counts, and package plan for the Arria V GZ devices.

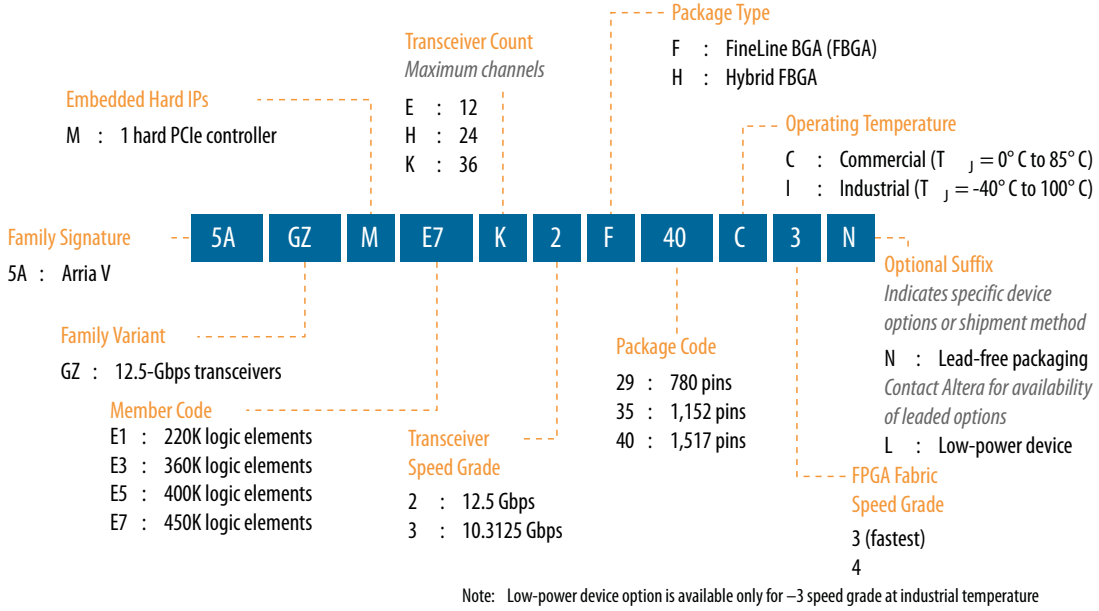
The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

Related Information

Altera Product Selector
Provides the latest information about Altera products.

Available Options

Figure 3: Sample Ordering Code and Available Options for Arria V GZ Devices



Note: Low-power device option is available only for –3 speed grade at industrial temperature

Maximum Resources

Table 8: Maximum Resource Counts for Arria V GZ Devices

Resource	Member Code			
	E1	E3	E5	E7
Logic Elements (LE) (K)	220	360	400	450
ALM	83,020	135,840	150,960	169,800
Register	332,080	543,360	603,840	679,200

Resource		Member Code			
		E1	E3	E5	E7
Memory (Kb)	M20K	11,700	19,140	28,800	34,000
	MLAB	2,594	4,245	4,718	5,306
Variable-precision DSP Block		800	1,044	1,092	1,139
18 x 18 Multiplier		1,600	2,088	2,184	2,278
PLL		20	20	24	24
12.5 Gbps Transceiver		24	24	36	36
GPIO[7]		414	414	674	674
LVDS	Transmitter	99	99	166	166
	Receiver	108	108	168	168
PCIe Hard IP Block		1	1	1	1

Related Information

High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook
Provides the number of LVDS channels in each device package.

Package Plan

Table 9: Package Plan for Arria V GZ Devices

Member Code	H780 (33 mm)		F1152 (35 mm)		F1517 (40 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
E1	342	12	414	24	—	—
E3	342	12	414	24	—	—
E5	—	—	534	24	674	36
E7	—	—	534	24	674	36

Arria V SX

This section provides the available options, maximum resource counts, and package plan for the Arria V SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

(7) The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

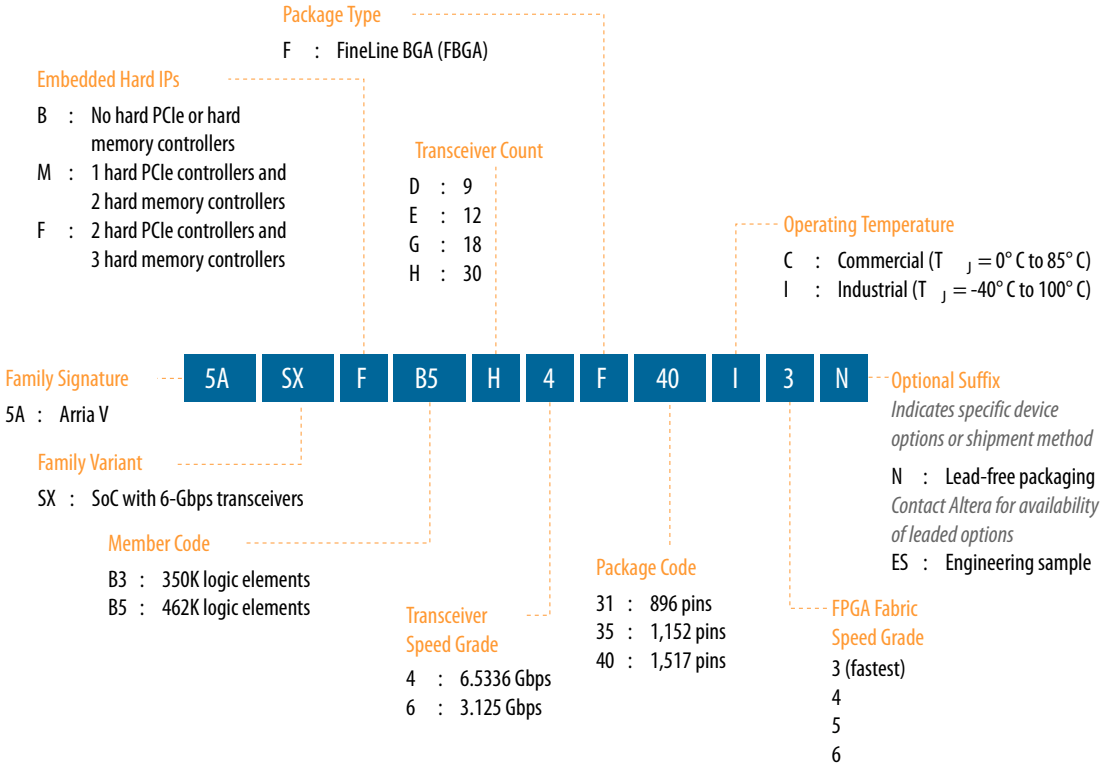
Related Information

Altera Product Selector
Provides the latest information about Altera products.

Available Options

Figure 4: Sample Ordering Code and Available Options for Arria V SX Devices

The –3 FPGA fabric speed grade is available only for industrial temperature devices.



Maximum Resources

Table 10: Maximum Resource Counts for Arria V SX Devices

Resource		Member Code	
		B3	B5
Logic Elements (LE) (K)		350	462
ALM		132,075	174,340
Register		528,300	697,360
Memory (Kb)	M10K	17,290	22,820
	MLAB	2,014	2,658
Variable-precision DSP Block		809	1,090
18 x 18 Multiplier		1,618	2,180

Resource		Member Code	
		B3	B5
FPGA PLL		14	14
HPS PLL		3	3
6 Gbps Transceiver		30	30
FPGA GPIO[8]		540	540
HPS I/O		208	208
LVDS	Transmitter	120	120
	Receiver	136	136
PCIe Hard IP Block		2	2
FPGA Hard Memory Controller		3	3
HPS Hard Memory Controller		1	1
ARM Cortex-A9 MPCore Processor		Dual-core	Dual-core

Related Information

High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook

Provides the number of LVDS channels in each device package.

Package Plan

Table 11: Package Plan for Arria V SX Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	F896 (31 mm)			F1152 (35 mm)			F1517 (40 mm)		
	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR
B3	250	208	12	385	208	18	540	208	30
B5	250	208	12	385	208	18	540	208	30

Arria V ST

This section provides the available options, maximum resource counts, and package plan for the Arria V ST devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

[8] The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

Variable-Precision DSP Block

Arria V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18, 27 x 27, and 36 x 36 bits natively
- A 64-bit accumulator
- Double accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Dynamic coefficients
- 18-bit internal coefficient register banks
- Enhanced independent multiplier operation
- Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Quartus Prime design software

Table 14: Variable-Precision DSP Block Configurations for Arria V Devices

Usage Example	Multiplier Size (Bit)	DSP Block Resource
Low precision fixed point for video applications	Three 9 x 9	1
Medium precision fixed point in FIR filters	Two 18 x 18	1
FIR filters	Two 18 x 18 with accumulate	1
Single-precision floating-point implementations	One 27 x 27	1
Very high precision fixed point implementations	One 36 x 36	2

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 18, or one 27 x 27 multipliers. Using two DSP block resources, you can also configure a 36 x 36 multiplier for high-precision applications. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

Variant	Member Code	M20K		M10K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Arria V ST	D3	—	—	1,729	17,290	3223	2,014	19,304
	D5	—	—	2,282	22,820	4253	2,658	25,478

Embedded Memory Configurations

Table 17: Supported Embedded Memory Block Configurations for Arria V Devices

This table lists the maximum configurations supported for the embedded memory blocks. The information is applicable only to the single-port RAM and ROM modes.

Memory Block	Depth (bits)	Programmable Width
MLAB	32	x16, x18, or x20
	64(11)	x10
M20K	512	x40
	1K	x20
	2K	x10
	4K	x5
	8K	x2
	16K	x1
M10K	256	x40 or x32
	512	x20 or x16
	1K	x10 or x8
	2K	x5 or x4
	4K	x2
	8K	x1

Clock Networks and PLL Clock Sources

650 MHz Arria V devices have 16 global clock networks capable of up to operation. The clock network architecture is based on Altera's global, quadrant, and peripheral clock structure. This clock structure is supported by dedicated clock input pins and fractional PLLs.

Note: To reduce power consumption, the Quartus Prime software identifies all unused sections of the clock network and powers them down.

(11) Available for Arria V GZ devices only.

Related Information

External Memory Interface Spec Estimator
For the latest information and to estimate the external memory system performance specification, use Altera's External Memory Interface Spec Estimator tool.

Low-Power Serial Transceivers

Arria V devices deliver the industry's lowest power consumption per transceiver channel:

- 12.5 Gbps transceivers at less than 170 mW
- 10 Gbps transceivers at less than 165 mW
- 6 Gbps transceivers at less than 105 mW

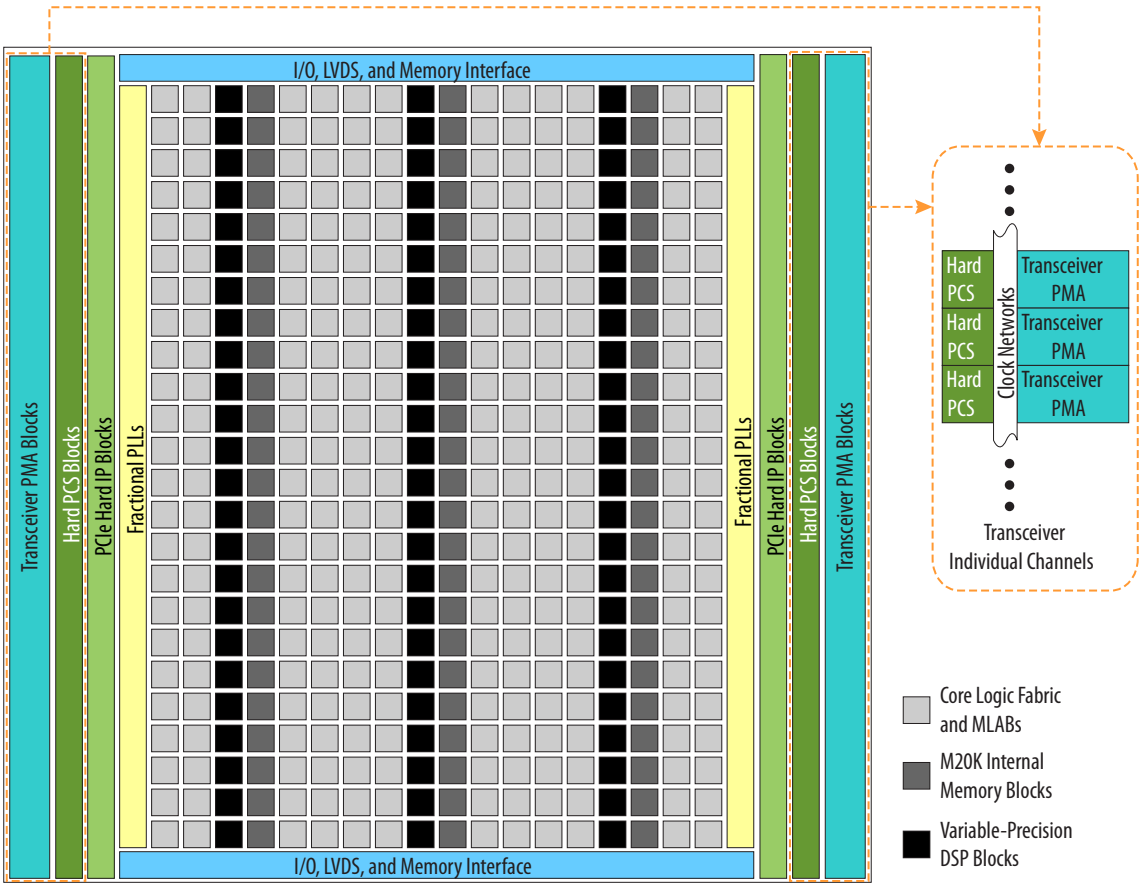
Arria V transceivers are designed to be compliant with a wide range of protocols and data rates.

Transceiver Channels

The transceivers are positioned on the left and right outer edges of the device. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks.

The following figures are graphical representations of a top view of the silicon die, which corresponds to a reverse view for flip chip packages. Different Arria V devices may have different floorplans than the ones shown in the figures.

Figure 10: Device Chip Overview for Arria V GZ Devices



Features	Capability
PLL-based clock recovery	Superior jitter tolerance
Programmable serializer and deserializer (SERDES)	Flexible SERDES width
Equalization and pre-emphasis	• Arria V GX, GT, SX, and ST devices—Up to 14.37 dB of pre-emphasis and up to 4.7 dB of equalization • Arria V GZ devices—4-tap pre-emphasis and de-emphasis
Ring oscillator transmit PLLs	611 Mbps to 10.3125 Gbps
LC oscillator ATX transmit PLLs (Arria V GZ devices only)	600 Mbps to 12.5 Gbps
Input reference clock range	27 MHz to 710 MHz
Transceiver dynamic reconfiguration	Allows the reconfiguration of a single channel without affecting the operation of other channels

PCS Features

The Arria V core logic connects to the PCS through an 8, 10, 16, 20, 32, 40, 64, 66, or 67 bit interface, depending on the transceiver data rate and protocol. Arria V devices contain PCS hard IP to support PCIe Gen1, Gen2, and Gen3, GbE, Serial RapidIO (SRIO), GPON, and CPRI.

All other standard and proprietary protocols within the following speed ranges are also supported:

- 611 Mbps to 6.5536 Gbps—supported through the custom double-width mode (up to 6.5536 Gbps) and custom single-width mode (up to 3.75 Gbps) of the transceiver PCS hard IP.
- 6.5536 Gbps to 10.3125 Gbps—supported through dedicated 80 or 64 bit interface that bypass the PCS hard IP and connects the PMA directly to the core logic. In Arria V GZ, this is supported in the transceiver PCS hard IP.

Table 21: Transceiver PCS Features for Arria V GX, GT, ST, and SX Devices

PCS Support[13]	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
Custom single- and double-width modes	0.611 to ~6.5536	• Phase compensation FIFO • Byte serializer • 8B/10B encoder	• Word aligner • 8B/10B decoder • Byte deserializer • Phase compensation FIFO
SRIO	1.25 to 6.25		
Serial ATA	1.5, 3.0, 6.0		

[13] Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through the soft PCS.

PCS Support[13]	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
PCIe Gen1 (x1, x2, x4, x8)	2.5 and 5.0	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • PIPE 2.0 interface to the core logic	• Word aligner • 8B/10B decoder • Byte deserializer • Phase compensation FIFO • Rate match FIFO • PIPE 2.0 interface to the core logic
PCIe Gen2[14] (x1, x2, x4)			
GbE	1.25	• Phase compensation FIFO • Byte serializer • 8B/10B encoder	• Word aligner • 8B/10B decoder • Byte deserializer • Phase compensation FIFO • Rate match FIFO
XAUI[15]	3.125	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • XAUI state machine for bonding four channels	• Word aligner • 8B/10B decoder • Byte deserializer • Phase compensation FIFO • XAUI state machine for realigning four channels • Deskew FIFO circuitry
SDI	0.27[16], 1.485, 2.97	• Phase compensation FIFO • Byte serializer	• Byte deserializer • Phase compensation FIFO
GPON[17]	1.25 and 2.5		
CPRI[18]	0.6144 to 6.144	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • TX deterministic latency	• Word aligner • 8B/10B decoder • Byte deserializer • Phase compensation FIFO • RX deterministic latency

(13) Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through the soft PCS.
(14) PCIe Gen2 is supported only through the PCIe hard IP.
(15) XAUI is supported through the soft PCS.
(16) The 0.27 Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.
(17) The GPON standard does not support burst mode.
(18) CPRI data rates above 6.5536 Gbps, such as 9.8304 Gbps, are supported through the soft PCS.

Table 22: Transceiver PCS Features for Arria V GZ Devices

Protocol	Data Rates (Gbps)	Transmitter Data Path Features	Receiver Data Path Features
Custom PHY	0.6 to 9.80	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • Bit-slip • Channel bonding	• Word aligner • Deskew FIFO • Rate match FIFO • 8B/10B decoder • Byte deserializer • Byte ordering
GPON	1.25 and 2.5		
Custom 10G PHY	9.98 to 12.5	• TX FIFO • Gear box • Bit-slip	• RX FIFO • Gear box
PCIe Gen1 (x1, x2 x4, x8)	2.5 and 5.0	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • Bit-slip • Channel bonding • PIPE 2.0 interface to core logic	• Word aligner • Deskew FIFO • Rate match FIFO • 8B/10B decoder • Byte deserializer, • Byte ordering • PIPE 2.0 interface to core logic
PCIe Gen2 (x1, x2, x4, x8)			
PCIe Gen3 (x1, x2, x4, x8)	8.0	• Phase compensation FIFO • 128B/130B encoder • Scrambler • Gear box • Bit-slip	• Block synchronization • Rate match FIFO • 128B/130B decoder • Descrambler • Phase compensation FIFO
10GbE	10.3125	• TX FIFO • 64B/66B encoder • Scrambler • Gear box	• RX FIFO • 64B/66B decoder • Descrambler • Block synchronization • Gear box
Interlaken	3.125 to 12.5	• TX FIFO • Frame generator • CRC-32 generator • Scrambler • Disparity generator • Gear box	• RX FIFO • Frame generator • CRC-32 checker • Frame decoder • Descrambler • Disparity checker • Block synchronization • Gear box

Protocol	Data Rates (Gbps)	Transmitter Data Path Features	Receiver Data Path Features
40GBASE-R Ethernet	4 x 10.3125	• TX FIFO • 64B/66B encoder • Scrambler • Alignment marker insertion • Gearbox • Block stripper	• RX FIFO • 64B/66B decoder • Descrambler • Lane reorder • Deskew • Alignment marker lock • Block synchronization • Gear box • Destripper
100GBASE-R Ethernet	10 x 10.3125		
40G and 100G OTN	(4 +1) x 11.3 (10 +1) x 11.3	• TX FIFO • Channel bonding • Byte serializer	• RX FIFO • Lane deskew • Byte deserializer
GbE	1.25	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • Bit-slip • Channel bonding • GbE state machine	• Word aligner • Deskew FIFO • Rate match FIFO • 8B/10B decoder • Byte deserializer • Byte ordering • GbE state machine
XAUI	3.125 to 4.25	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • Bit-slip • Channel bonding • XAUI state machine for bonding four channels	• Word aligner • Deskew FIFO • Rate match FIFO • 8B/10B decoder • Byte deserializer • Byte ordering • XAUI state machine for realigning four channels
SRIO	1.25 to 6.25	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • Bit-slip • Channel bonding • SRIO V2.1-compliant x2 and x4 channel bonding	• Word aligner • Deskew FIFO • Rate match FIFO • 8B/10B decoder • Byte deserializer • Byte ordering • SRIO V2.1-compliant x2 and x4 deskew state machine

System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals to interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

HPS–FPGA AXI Bridges

The HPS–FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA®) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to slaves in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS–FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS–FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features. The SDRAM controller subsystem supports DDR2, DDR3, or LPDDR2 devices up to 4 Gb in density operating at up to 533 MHz (1066 Mbps data rate).

FPGA Configuration and Processor Booting

The FPGA fabric and HPS in the SoC are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power, or shut down the entire FPGA fabric to reduce total system power.

You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- You can power up both the HPS and the FPGA fabric together, configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

Note: Although the FPGA fabric and HPS are on separate power domains, the HPS must remain powered up during operation while the FPGA fabric can be powered up or down as required.

Related Information

- **Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines**
  Provides detailed information about power supply pin connection guidelines and power regulator sharing.
- **Arria V GZ Device Family Pin Connection Guidelines**
  Provides detailed information about power supply pin connection guidelines and power regulator sharing.

Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Qsys system integration tool in the Quartus Prime software.

For software development, the ARM-based SoC devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Altera SoCs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux, VxWorks®, and other operating systems is available for the SoCs. For more information on the operating systems support availability, contact the Altera sales team.

You can begin device-specific firmware and software development on the Altera SoC Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board that runs on a PC. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

Related Information

Altera Worldwide Sales Support

Dynamic and Partial Reconfiguration

The Arria V devices support dynamic reconfiguration and partial reconfiguration.

Dynamic Reconfiguration

The dynamic reconfiguration feature allows you to dynamically change the transceiver data rates, PMA settings, or protocols of a channel, without affecting data transfer on adjacent channels. This feature is ideal for applications that require on-the-fly multiprotocol or multirate support. You can reconfigure the PMA, PCS, and PCIe hard IP blocks with dynamic reconfiguration.

Partial Reconfiguration

Note: Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

Partial reconfiguration allows you to reconfigure part of the device while other sections of the device remain operational. This capability is important in systems with critical uptime requirements because it allows you to make updates or adjust functionality without disrupting services.

Apart from lowering cost and power consumption, partial reconfiguration increases the effective logic density of the device because placing device functions that do not operate simultaneously is not necessary. Instead, you can store these functions in external memory and load them whenever the functions are required. This capability reduces the size of the device because it allows multiple applications on a single device—saving the board space and reducing the power consumption.

Altera simplifies the time-intensive task of partial reconfiguration by building this capability on top of the proven incremental compile and design flow in the Quartus Prime design software. With the Altera solution, you do not need to know all the intricate device architecture details to perform a partial reconfiguration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable simultaneous partial reconfiguration of both the device core and transceivers.

Enhanced Configuration and Configuration via Protocol

Table 23: Configuration Modes and Features of Arria V Devices

Arria V devices support 1.8 V, 2.5 V, 3.0 V, and 3.3 V[19] programming voltages and several configuration modes.

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompressio	Design Security	Partial Reconfiguratio[20]	Remote System Update
AS through the EPCS and EPCQ serial configuration device	1 bit, 4 bits	100	—	Yes	Yes	—	Yes
PS through CPLD or external microcontroller	1 bit	125	125	Yes	Yes	—	—

[19] Arria V GZ does not support 3.3 V.
[20] Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.