Intel - 5ASXMB3G6F40C6N Datasheet

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System On Chip (SoC)

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Resource		Member Code			
		C3	C7	D3	D7
Transceiver	6 Gbps[4]	3 (9)	6 (24)	6 (24)	6 (36)
	10 Gbps[5]	4	12	12	20
GPIO[6]		416	544	704	704
LVDS	Transmitter	68	120	160	160
	Receiver	80	136	176	176
PCIe Hard IP Block		1	2	2	2
Hard Memory Controller		2	4	4	4

Resource		Member Code			
		E1	E3	E5	E7
Memory (Kb)	M20K	11,700	19,140	28,800	34,000
	MLAB	2,594	4,245	4,718	5,306
Variable-precision DSP Block		800	1,044	1,092	1,139
18 x 18 Multiplier		1,600	2,088	2,184	2,278
PLL		20	20	24	24
12.5 Gbps Transceiver		24	24	36	36
GPIO(7)		414	414	674	674
LVDS	Transmitter	99	99	166	166
	Receiver	108	108	168	168
PCIe Hard IP Block		1	1	1	1

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Provides the number of LVDS channels in each device package.

Package Plan

Table 9: Package Plan for Arria V GZ Devices

Member Code	H780 (33 mm)		F1152 (35 mm)		F1517 (40 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
E1	342	12	414	24	*f*	*f*
E3	342	12	414	24	*f*	*f*
E5	*f*	*f*	534	24	674	36
E7	*f*	*f*	534	24	674	36

Arria V SX

This section provides the available options, maximum resource counts, and package plan for the Arria V SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

(7) The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

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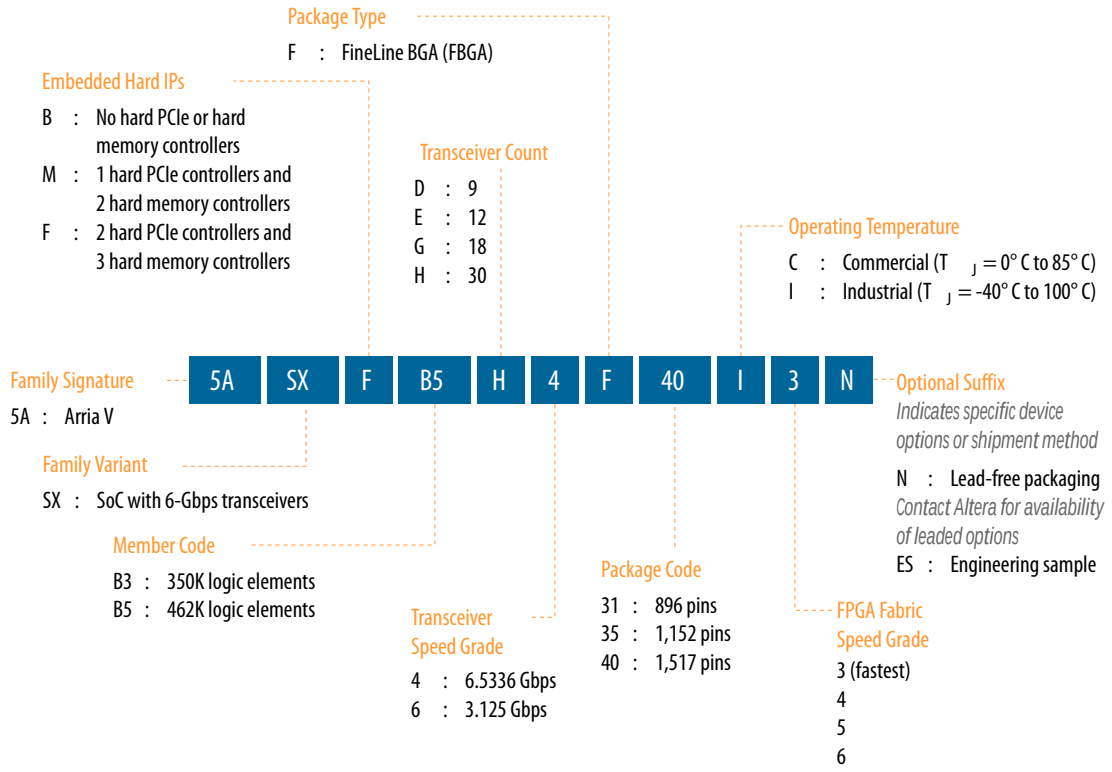
Provides the latest information about Altera products.

Available Options

Figure 4: Sample Ordering Code and Available Options for Arria V SX Devices

The …3 FPGA fabric speed grade is available only for industrial temperature devices.



Maximum Resources

Table 10: Maximum Resource Counts for Arria V SX Devices

Resource		Member Code	
		B3	B5
Logic Elements (LE) (K)		350	462
ALM		132,075	174,340
Register		528,300	697,360
Memory (Kb)	M10K	17,290	22,820
	MLAB	2,014	2,658
Variable-precision DSP Block		809	1,090
18 x 18 Multiplier		1,618	2,180

PLL Features

The PLLs in the Arria V devices support the following features:

- Frequency synthesis
- On-chip clock deskew
- Jitter attenuation
- Counter reconfiguration
- Programmable output clock duty cycles
- PLL cascading
- Reference clock switchover
- Programmable bandwidth
- Dynamic phase shift
- Zero delay buffers

Fractional PLL

In addition to integer PLLs, the Arria V devices use a fractional PLL architecture. The devices have up to 16 PLLs, each with 18 output counters. One fractional PLL can use up to 18 output counters and two adjacent fractional PLLs share the 18 output counters. You can use the output counters to reduce PLL usage in two ways:

- Reduce the number of oscillators that are required on your board by using fractional PLLs
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

If you use the fractional PLL mode, you can use the PLLs for precision fractional-N frequency synthesis, removing the need for off-chip reference clock sources in your design.

The transceiver fractional PLLs that are not used by the transceiver I/Os can be used as general purpose fractional PLLs by the FPGA fabric.

FPGA General Purpose I/O

Arria V devices offer highly configurable GPIOs. The following list describes the features of the GPIOs:

- Programmable bus hold and weak pull-up
- LVDS output buffer with programmable differential output voltage (V_{OD}) and programmable pre-emphasis
- On-chip parallel termination (R OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Unused voltage reference (V_{REF}) pins that can be configured as user I/Os (Arria V GX, GT, SX, and ST only)
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

External Memory Performance

Table 18: External Memory Interface Performance in Arria V Devices

Interface	Voltage (V)	Hard Controller (MHz)	Soft Controller (MHz)	
		Arria V GX, GT, SX, and ST	Arria V GX, GT, SX, and ST	Arria V GZ
DDR3 SDRAM	1.5	533	667	800
	1.35	533	600	800
DDR2 SDRAM	1.8	400	400	400
LPDDR2 SDRAM	1.2	*f*	400	*f*
RLDRAM 3	1.2	*f*	*f*	667
RLDRAM II	1.8	*f*	400	533
	1.5	*f*	400	533
QDR II+ SRAM	1.8	*f*	400	500
	1.5	*f*	400	500
QDR II SRAM	1.8	*f*	400	333
	1.5	*f*	400	333
DDR II+ SRAM[12]	1.8	*f*	400	*f*
	1.5	*f*	400	*f*

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For the latest information and to estimate the external memory system performance specification, use Altera•s External Memory Interface Spec Estimator tool.

HPS External Memory Performance

Table 19: HPS External Memory Interface Performance

The hard processor system (HPS) is available in Arria V SoC devices only.

Interface	Voltage (V)	HPS Hard Controller (MHz)
DDR3 SDRAM	1.5	533
	1.35	533
LPDDR2 SDRAM	1.2	333

(12) Not available as Altera IP.

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For the latest information and to estimate the external memory system performance specification, use Altera•s External Memory Interface Spec Estimator tool.

Low-Power Serial Transceivers

Arria V devices deliver the industry•s lowest power consumption per transceiver channel:

- 12.5 Gbps transceivers at less than 170 mW
- 10 Gbps transceivers at less than 165 mW
- 6 Gbps transceivers at less than 105 mW

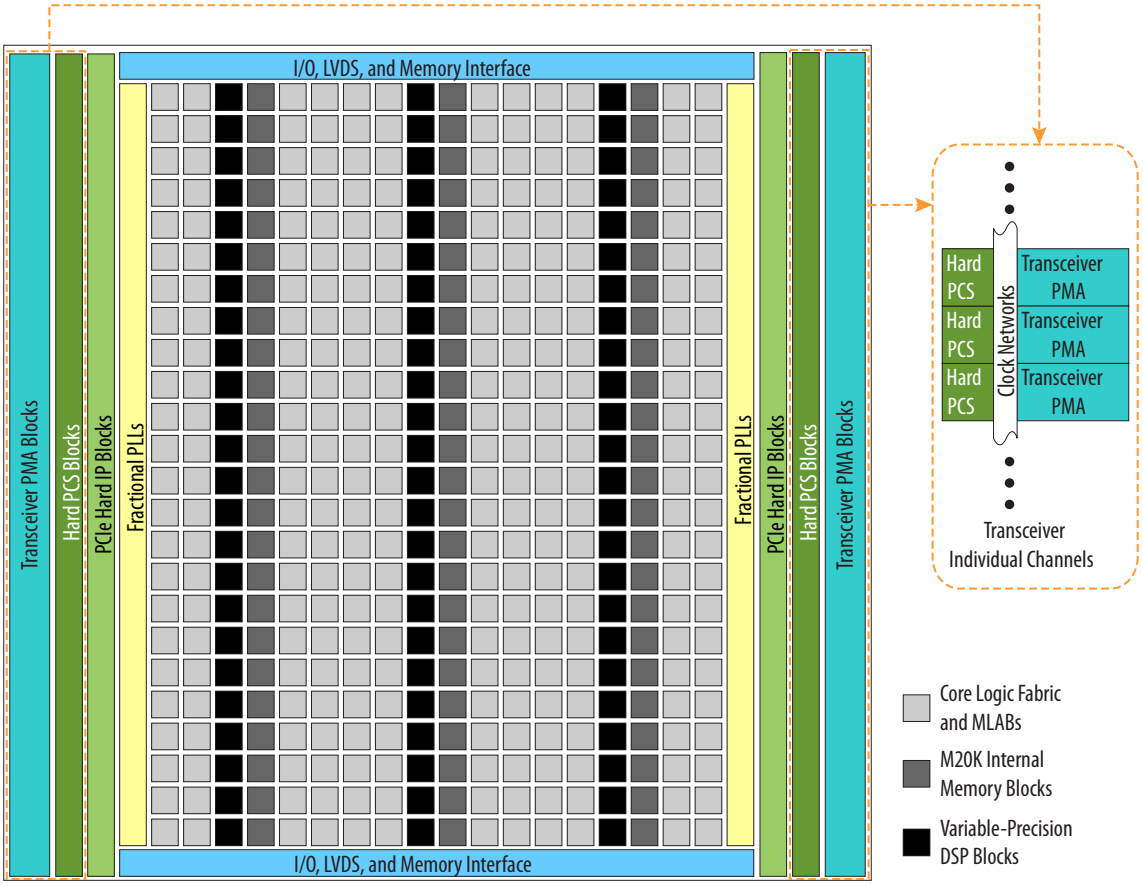
Arria V transceivers are designed to be compliant with a wide range of protocols and data rates.

Transceiver Channels

The transceivers are positioned on the left and right outer edges of the device. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks.

The following figures are graphical representations of a top view of the silicon die, which corresponds to a reverse view for flip chip packages. Different Arria V devices may have different floorplans than the ones shown in the figures.

Figure 10: Device Chip Overview for Arria V GZ Devices



Features	Capability
PLL-based clock recovery	Superior jitter tolerance
Programmable serializer and deserializer (SERDES)	Flexible SERDES width
Equalization and pre-emphasis	€ Arria V GX, GT, SX, and ST devices ƒ Up to 14.37 dB of pre-emphasis and up to 4.7 dB of equalization € Arria V GZ devices ƒ 4-tap pre-emphasis and de-emphasis
Ring oscillator transmit PLLs	611 Mbps to 10.3125 Gbps
LC oscillator ATX transmit PLLs (Arria V GZ devices only)	600 Mbps to 12.5 Gbps
Input reference clock range	27 MHz to 710 MHz
Transceiver dynamic reconfiguration	Allows the reconfiguration of a single channel without affecting the operation of other channels

PCS Features

The Arria V core logic connects to the PCS through an 8, 10, 16, 20, 32, 40, 64, 66, or 67 bit interface, depending on the transceiver data rate and protocol. Arria V devices contain PCS hard IP to support PCIe Gen1, Gen2, and Gen3, GbE, Serial RapidIO (SRIO), GPON, and CPRI.

All other standard and proprietary protocols within the following speed ranges are also supported:

€ 611 Mbps to 6.5536 Gbps ƒ supported through the custom double-width mode (up to 6.5536 Gbps) and custom single-width mode (up to 3.75 Gbps) of the transceiver PCS hard IP.

€ 6.5536 Gbps to 10.3125 Gbps ƒ supported through dedicated 80 or 64 bit interface that bypass the PCS hard IP and connects the PMA directly to the core logic. In Arria V GZ, this is supported in the transceiver PCS hard IP.

Table 21: Transceiver PCS Features for Arria V GX, GT, ST, and SX Devices

PCS Support[13]	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
Custom single- and double-width modes	0.611 to ~6.5536	€ Phase compensation FIFO € Byte serializer € 8B/10B encoder	€ Word aligner € 8B/10B decoder € Byte deserializer € Phase compensation FIFO
SRIO	1.25 to 6.25		
Serial ATA	1.5, 3.0, 6.0		

(13) Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through the soft PCS

PCS Support[13]	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
PCIe Gen1 (x1, x2, x4, x8) PCIe Gen2[14] (x1, x2, x4)	2.5 and 5.0	€ Phase compensation FIFO € Byte serializer € 8B/10B encoder € PIPE 2.0 interface to the core logic	€ Word aligner € 8B/10B decoder € Byte deserializer € Phase compensation FIFO € Rate match FIFO € PIPE 2.0 interface to the core logic
GbE	1.25	€ Phase compensation FIFO € Byte serializer € 8B/10B encoder	€ Word aligner € 8B/10B decoder € Byte deserializer € Phase compensation FIFO € Rate match FIFO
XAUI[15]	3.125	€ Phase compensation FIFO € Byte serializer € 8B/10B encoder € XAUI state machine for bonding four channels	€ Word aligner € 8B/10B decoder € Byte deserializer € Phase compensation FIFO € XAUI state machine for realigning four channels € Deskew FIFO circuitry
SDI	0.27[16], 1.485, 2.97	€ Phase compensation FIFO € Byte serializer	€ Byte deserializer € Phase compensation FIFO
GPON[17]	1.25 and 2.5		
CPRI[18]	0.6144 to 6.144	€ Phase compensation FIFO € Byte serializer € 8B/10B encoder € TX deterministic latency	€ Word aligner € 8B/10B decoder € Byte deserializer € Phase compensation FIFO € RX deterministic latency

(13) Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through the soft PCS
(14) PCIe Gen2 is supported only through the PCIe hard IP.
(15) XAUI is supported through the soft PCS.
(16) The 0.27 Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.
(17) The GPON standard does not support burst mode.
(18) CPRI data rates above 6.5536 Gbps, such as 9.8304 Gbps, are supported through the soft PCS.

Table 22: Transceiver PCS Features for Arria V GZ Devices

Protocol	Data Rates (Gbps)	Transmitter Data Path Features	Receiver Data Path Features
Custom PHY	0.6 to 9.80	€ Phase compensation FIFO € Byte serializer € 8B/10B encoder € Bit-slip € Channel bonding	€ Word aligner € Deskew FIFO € Rate match FIFO € 8B/10B decoder € Byte deserializer € Byte ordering
GPON	1.25 and 2.5		
Custom 10G PHY	9.98 to 12.5	€ TX FIFO € Gear box € Bit-slip	€ RX FIFO € Gear box
PCIe Gen1 (x1, x2 x4, x8)	2.5 and 5.0	€ Phase compensation FIFO € Byte serializer € 8B/10B encoder € Bit-slip € Channel bonding € PIPE 2.0 interface to core logic	€ Word aligner € Deskew FIFO € Rate match FIFO € 8B/10B decoder € Byte deserializer, € Byte ordering € PIPE 2.0 interface to core logic
PCIe Gen2 (x1, x2, x4, x8)			
PCIe Gen3 (x1, x2, x4, x8)	8.0	€ Phase compensation FIFO € 128B/130B encoder € Scrambler € Gear box € Bit-slip	€ Block synchronization € Rate match FIFO € 128B/130B decoder € Descrambler € Phase compensation FIFO
10GbE	10.3125	€ TX FIFO € 64B/66B encoder € Scrambler € Gear box	€ RX FIFO € 64B/66B decoder € Descrambler € Block synchronization € Gear box
Interlaken	3.125 to 12.5	€ TX FIFO € Frame generator € CRC-32 generator € Scrambler € Disparity generator € Gear box	€ RX FIFO € Frame generator € CRC-32 checker € Frame decoder € Descrambler € Disparity checker € Block synchronization € Gear box

You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- You can power up both the HPS and the FPGA fabric together, configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

Not Although the FPGA fabric and HPS are on separate power domains, the HPS must remain powered up during operation while the FPGA fabric can be powered up or down as required.

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  Provides detailed information about power supply pin connection guidelines and power regulator sharing.
- **rr ▪ V GZ D v c F▪m Ăy ▪ Co▪▪ ct o▪ G Ă▪ s**
  Provides detailed information about power supply pin connection guidelines and power regulator sharing.

Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Qsys system integration tool in the Quartus Prime software.

For software development, the ARM-based SoC devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Altera SoCs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux, VxWorks®, and other operating systems is available for the SoCs. For more information on the operating systems support availability, contact the Altera sales team.

You can begin device-specific firmware and software development on the Altera SoC Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board that runs on a PC. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

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Dynamic and Partial Reconfiguration

The Arria V devices support dynamic reconfiguration and partial reconfiguration.

Dynamic Reconfiguration

The dynamic reconfiguration feature allows you to dynamically change the transceiver data rates, PMA settings, or protocols of a channel, without affecting data transfer on adjacent channels. This feature is ideal for applications that require on-the-fly multiprotocol or multirate support. You can reconfigure the PMA, PCS, and PCIe hard IP blocks with dynamic reconfiguration.

Partial Reconfiguration

Not Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

Partial reconfiguration allows you to reconfigure part of the device while other sections of the device remain operational. This capability is important in systems with critical uptime requirements because it allows you to make updates or adjust functionality without disrupting services.

Apart from lowering cost and power consumption, partial reconfiguration increases the effective logic density of the device because placing device functions that do not operate simultaneously is not necessary. Instead, you can store these functions in external memory and load them whenever the functions are required. This capability reduces the size of the device because it allows multiple applications on a single device *f* saving the board space and reducing the power consumption.

Altera simplifies the time-intensive task of partial reconfiguration by building this capability on top of the proven incremental compile and design flow in the Quartus Prime design software. With the Altera solution, you do not need to know all the intricate device architecture details to perform a partial reconfi, guration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable simultaneous partial reconfigu, ration of both the device core and transceivers.

Enhanced Configuration and Configuration via Protocol

Table 23: Configuration Modes and Features of Arria V Devices

Arria V devices support 1.8 V, 2.5 V, 3.0 V, and 3.3 V[19] programming voltages and several configuration modes.

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompressio	Design Security	Partial Reconfiguratio [20]	Remote System Update
AS through the EPCS and EPCQ serial configura, tion device	1 bit, 4 bits	100	*f*	Yes	Yes	*f*	Yes
PS through CPLD or external microcontroller	1 bit	125	125	Yes	Yes	*f*	*f*

(19) Arria V GZ does not support 3.3 V.
(20) Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

Document Revision History

Date	Version	Changes
December 2015	2015.12.21	€ Updated RoHS and optional suffix information in sample ordering code and available options diagrams for Arria V GX and GT devices. € Changed instances of *Quartus II* to *Quartus Prime*.
January 2015	2015.01.23	€ Updated package dimension for Arria V GZ H780 package from 29 mm to 33 mm. € Updated dual-core ARM Cortex-A9 MPCore processor maximum frequency from 800 MHz to 1.05 GHz.
December 2013	2013.12.26	€ 10-Gbps Ethernet (10GbE) PCS and Interlaken PCS are for Arria V GZ only. € Removed "Preliminary" texts from Ordering Code figures, Maximum Resources, Package Plan and I/O Vertical Migration tables. € Added link to Ă r• ro ct S Ăctor for each device variant. € Added leaded package options. € Removed the note "The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs." for all PLLs in the Maximum Resource Counts table. € Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F896 package from 170 to 250. € Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F1152 package from 350 to 385. € Corrected FPGA GPIO for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 F1517 package from 528 to 540. € Corrected LVDS Transmitter for Arria V SX B3 and B5 as well as Arria V ST D3 and D5 devices from 121 to 120. € Added links to Altera•Ŧt r•Ă mory Sp c Ŧt m•tor tool to the topics listing the external memory interface performance. € Added x2 for PCIe Gen3, Gen 2, and Gen 1.
August 2013	2013.08.19	€ Removed the note about the PCIe hard IP on the right side of the device in the F896 package of the Arria V GX variant. These devices do not have PCIe hard IP on the right side. € Added transceiver speed grade 6 to the available options of the Arria V SX variant. € Corrected the maximum LVDS transmitter channel counts for the Arria V GX A1 and A3 devices from 68 to 67. € Corrected the maximum FPGA GPIO count for Arria V ST D5 devices from 540 to 528.