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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Obsolete
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I <sup>2</sup> C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	700MHz
Primary Attributes	FPGA - 462K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FBGA, FC (31x31)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5asxmb5e6f31c6n">https://www.e-xfl.com/product-detail/intel/5asxmb5e6f31c6n</a>

Feature	Description
Configuration	<ul style="list-style-type: none"> <li>• Tamper protection-comprehensive design protection to protect your valuable IP investments</li> <li>• Enhanced advanced encryption standard (AES) design security features</li> <li>• CvP</li> <li>• Partial and dynamic reconfiguration of the FPGA</li> <li>• Active serial (AS) x1 and x4, passive serial (PS), JTAG, and fast passive parallel (FPP) x8, x16, and x32 ( Arria V GZ) configuration options</li> <li>• Remote system upgrade</li> </ul>

## Arria V Device Variants and Packages

**Table 3: Device Variants for the Arria V Device Family**

Variant	Description
Arria V GX	FPGA with integrated 6.5536 Gbps transceivers that provides bandwidth, cost, and power levels that are optimized for high-volume data and signal-processing applications
Arria V GT	FPGA with integrated 10.3125 Gbps transceivers that provides enhanced high-speed serial I/O bandwidth for cost-sensitive data and signal processing applications
Arria V GZ	FPGA with integrated 12.5 Gbps transceivers that provides enhanced high-speed serial I/O bandwidth for high-performance and cost-sensitive data and signal processing applications
Arria V SX	SoC with integrated ARM-based HPS and 6.5536 Gbps transceivers
Arria V ST	SoC with integrated ARM-based HPS and 10.3125 Gbps transceivers

### Arria V GX

This section provides the available options, maximum resource counts, and package plan for the Arria V GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

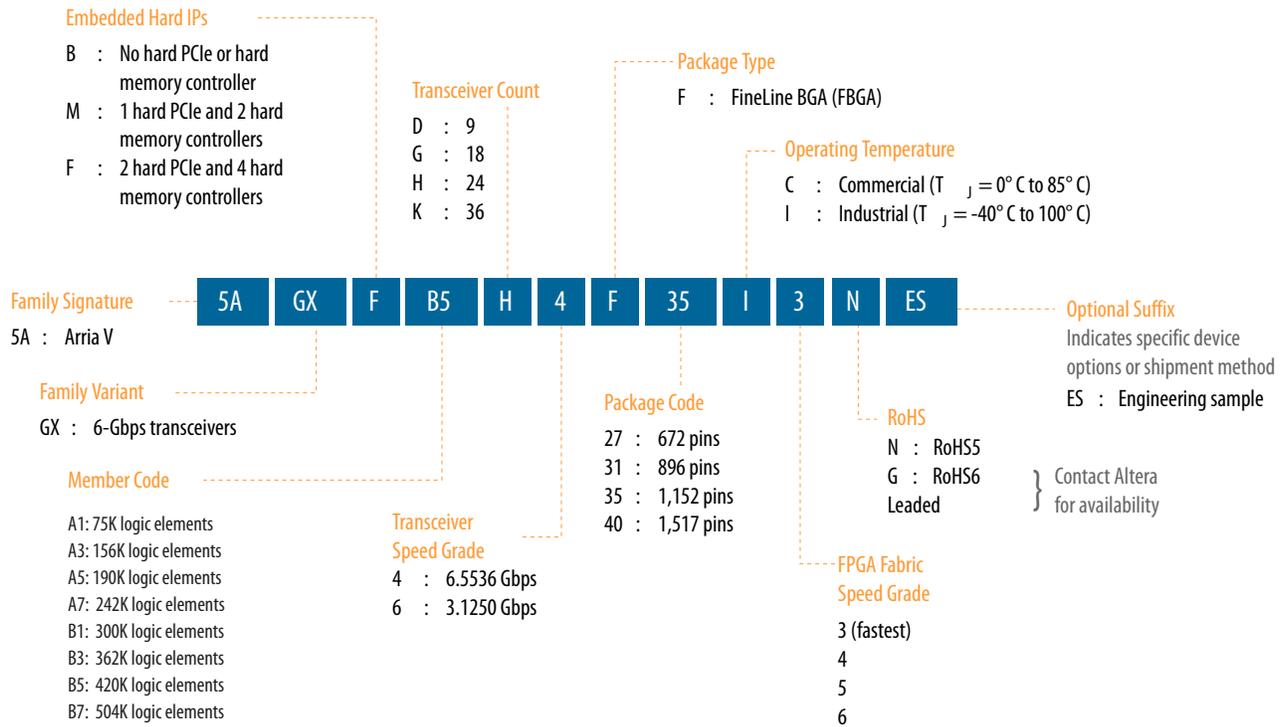
#### Related Information

##### [Altera Product Selector](#)

Provides the latest information about Altera products.

## Available Options

Figure 1: Sample Ordering Code and Available Options for Arria V GX Devices



## Maximum Resources

Table 4: Maximum Resource Counts for Arria V GX Devices

Resource	Member Code								
	A1	A3	A5	A7	B1	B3	B5	B7	
Logic Elements (LE) (K)	75	156	190	242	300	362	420	504	
ALM	28,302	58,900	71,698	91,680	113,208	136,880	158,491	190,240	
Register	113,208	235,600	286,792	366,720	452,832	547,520	633,964	760,960	
Memory (Kb)	M10K	8,000	10,510	11,800	13,660	15,100	17,260	20,540	24,140
	MLAB	463	961	1,173	1,448	1,852	2,098	2,532	2,906
Variable-precision DSP Block	240	396	600	800	920	1,045	1,092	1,156	
18 x 18 Multiplier	480	792	1,200	1,600	1,840	2,090	2,184	2,312	
PLL	10	10	12	12	12	12	16	16	

Resource		Member Code			
		C3	C7	D3	D7
Transceiver	6 Gbps <sup>(4)</sup>	3 (9)	6 (24)	6 (24)	6 (36)
	10 Gbps <sup>(5)</sup>	4	12	12	20
GPIO <sup>(6)</sup>		416	544	704	704
LVDS	Transmitter	68	120	160	160
	Receiver	80	136	176	176
PCIe Hard IP Block		1	2	2	2
Hard Memory Controller		2	4	4	4

**Related Information**

- [High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook](#)  
Provides the number of LVDS channels in each device package.
- [Transceiver Architecture in Arria V Devices](#)  
Describes 10 Gbps channels usage conditions and SFF-8431 compliance requirements.

**Package Plan**

**Table 7: Package Plan for Arria V GT Devices**

Member Code	F672 (27 mm)			F896 (31 mm)			F1152 (35 mm)			F1517 (40 mm)		
	GPIO	XCVR		GPIO	XCVR		GPIO	XCVR		GPIO	XCVR	
		6-Gbps	10-Gbps		6-Gbps	10-Gbps		6-Gbps	10-Gbps		6-Gbps	10-Gbps
C3	336	3 (9)	4	416	3 (9)	4	—	—	—	—	—	—
C7	—	—	—	384	6 (18)	8	544	6 (24)	12	—	—	—
D3	—	—	—	384	6 (18)	8	544	6 (24)	12	704	6 (24)	12
D7	—	—	—	—	—	—	544	6 (24)	12	704	6 (36)	20

The 6-Gbps transceiver counts are for dedicated 6-Gbps channels. You can also configure any pair of 10-Gbps channels as three 6-Gbps channels—the total number of 6-Gbps channels are shown in brackets. For example, you can also configure the Arria V GT D7 device in the F1517 package with nine 6-Gbps

<sup>(4)</sup> The 6 Gbps transceiver counts are for dedicated 6-Gbps channels. You can also configure any pair of 10 Gbps channels as three 6 Gbps channels—the total number of 6 Gbps channels are shown in brackets.  
<sup>(5)</sup> Chip-to-chip connections only. For 10 Gbps channel usage conditions, refer to the Transceiver Architecture in Arria V Devices chapter.  
<sup>(6)</sup> The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

and eighteen 10-Gbps, twelve 6-Gbps and sixteen 10-Gbps, fifteen 6-Gbps and fourteen 10-Gbps, or up to thirty-six 6-Gbps with no 10-Gbps channels.

## Arria V GZ

This section provides the available options, maximum resource counts, and package plan for the Arria V GZ devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

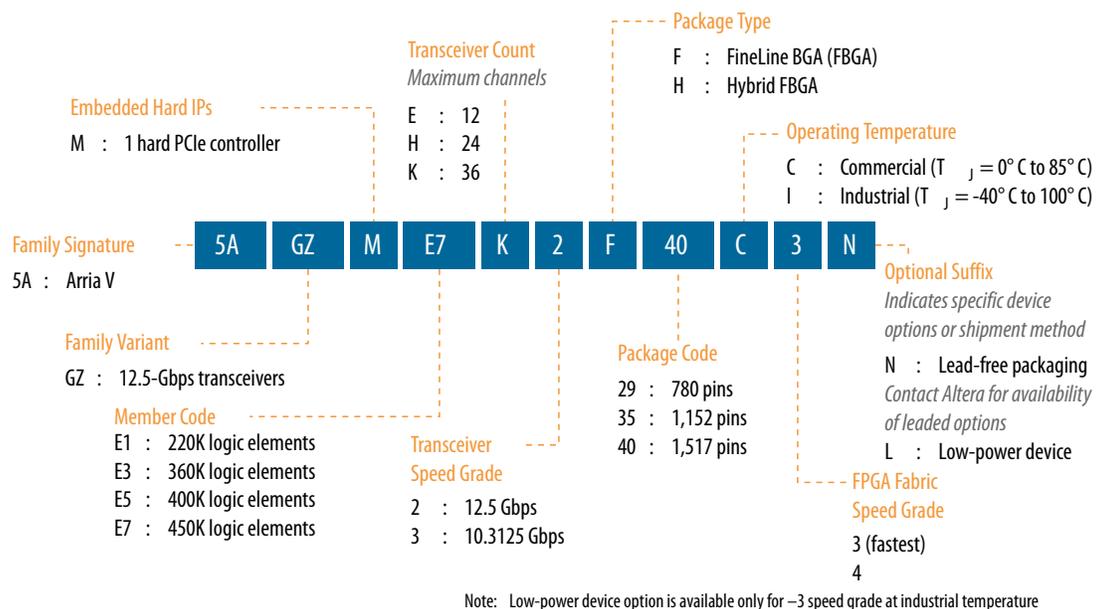
### Related Information

#### Altera Product Selector

Provides the latest information about Altera products.

## Available Options

Figure 3: Sample Ordering Code and Available Options for Arria V GZ Devices



## Maximum Resources

Table 8: Maximum Resource Counts for Arria V GZ Devices

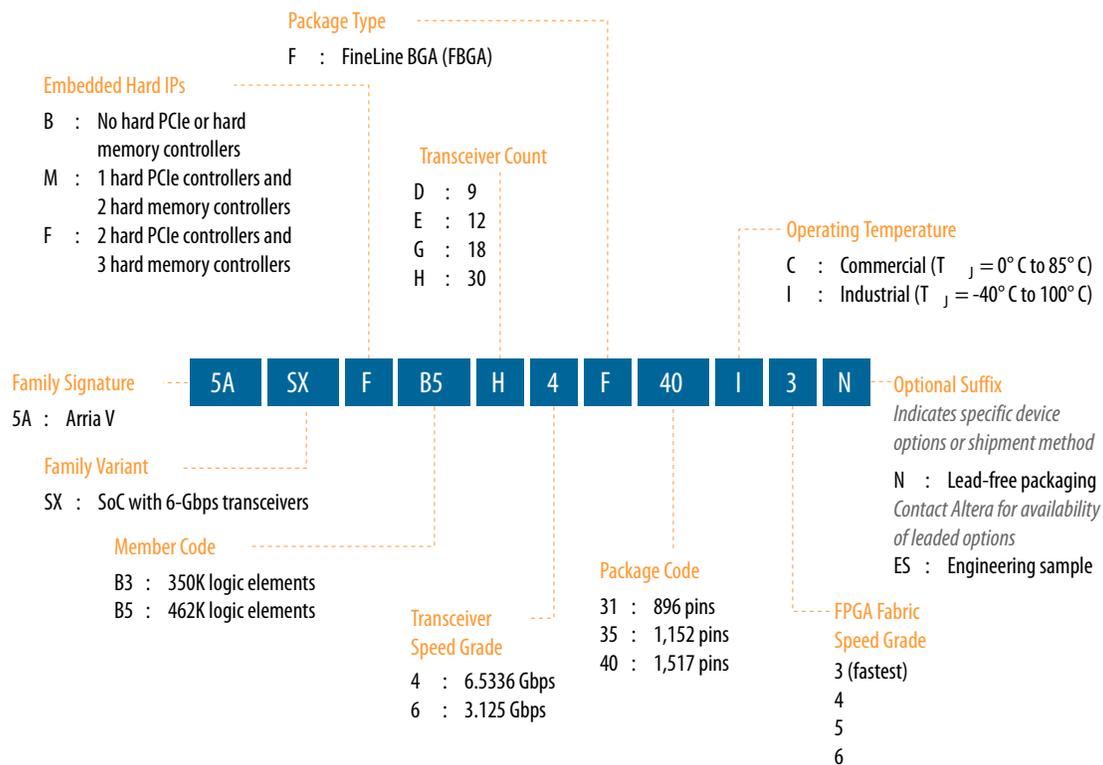
Resource	Member Code			
	E1	E3	E5	E7
Logic Elements (LE) (K)	220	360	400	450
ALM	83,020	135,840	150,960	169,800
Register	332,080	543,360	603,840	679,200

**Related Information****Altera Product Selector**

Provides the latest information about Altera products.

**Available Options****Figure 4: Sample Ordering Code and Available Options for Arria V SX Devices**

The –3 FPGA fabric speed grade is available only for industrial temperature devices.

**Maximum Resources****Table 10: Maximum Resource Counts for Arria V SX Devices**

Resource	Member Code	
	B3	B5
Logic Elements (LE) (K)	350	462
ALM	132,075	174,340
Register	528,300	697,360
Memory (Kb)	M10K	22,820
	MLAB	2,658
Variable-precision DSP Block	809	1,090
18 x 18 Multiplier	1,618	2,180

Resource	Member Code	
	B3	B5
FPGA PLL	14	14
HPS PLL	3	3
6 Gbps Transceiver	30	30
FPGA GPIO <sup>(8)</sup>	540	540
HPS I/O	208	208
LVDS	Transmitter	120
	Receiver	136
PCIe Hard IP Block	2	2
FPGA Hard Memory Controller	3	3
HPS Hard Memory Controller	1	1
ARM Cortex-A9 MPCore Processor	Dual-core	Dual-core

**Related Information**

[High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook](#)

Provides the number of LVDS channels in each device package.

**Package Plan**

**Table 11: Package Plan for Arria V SX Devices**

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	F896 (31 mm)			F1152 (35 mm)			F1517 (40 mm)		
	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR
B3	250	208	12	385	208	18	540	208	30
B5	250	208	12	385	208	18	540	208	30

**Arria V ST**

This section provides the available options, maximum resource counts, and package plan for the Arria V ST devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

<sup>(8)</sup> The number of GPIOs does not include transceiver I/Os. In the Quartus Prime software, the number of user I/Os includes transceiver I/Os.

## I/O Vertical Migration for Arria V Devices

**Figure 6: Vertical Migration Capability Across Arria V Device Packages and Densities**

The arrows indicate the vertical migration paths. Some packages have several migration paths. The devices included in each vertical migration path are shaded. You can also migrate your design across device densities in the same package option if the devices have the same dedicated pins, configuration pins, and power pins.

Variant	Member Code	Package				
		F672	F780	F896	F 1152	F1517
Arria V GX	A1					
	A3					
	A5					
	A7					
	B1					
	B3					
	B5					
	B7					
Arria V GT	C3					
	C7					
	D3					
	D7					
Arria V GZ	E1					
	E3					
	E5					
	E7					
Arria V SX	B3					
	B5					
Arria V ST	D3					
	D5					

You can achieve the vertical migration shaded in red if you use only up to 320 GPIOs, up to nine 6 Gbps transceiver channels, and up to four 10 Gbps transceiver (for Arria V GT devices). This migration path is not shown in the Quartus Prime software Pin Migration View.

**Note:** To verify the pin migration compatibility, use the Pin Migration View window in the Quartus Prime software Pin Planner.

**Note:** Except for Arria V GX A5 and A7, and Arria V GT C7 devices, all other Arria V GX and GT devices require a specific power-up sequence. If you plan to migrate your design from Arria V GX A5 and A7, and Arria V GT C7 devices to other Arria V devices, your design must adhere to the same required power-up sequence.

**Related Information**

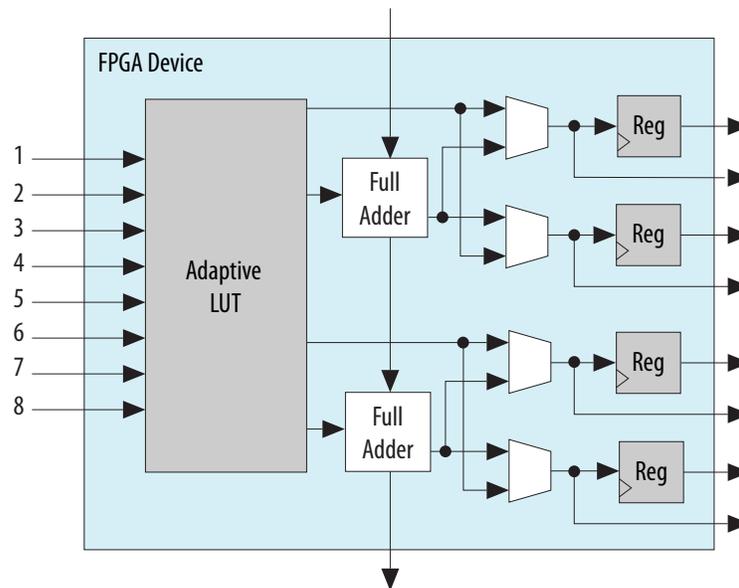
- [Managing Device I/O Pins chapter, Quartus Prime Handbook](#)  
Provides more information about vertical I/O migrations.
- [Power Management in Arria V Devices](#)  
Describes the power-up sequence required for Arria V GX and GT devices.

## Adaptive Logic Module

Arria V devices use a 28 nm ALM as the basic building block of the logic fabric.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than previous generations.

**Figure 7: ALM for Arria V Devices**



You can configure up to 50% of the ALMs in the Arria V devices as distributed memory using MLABs.

**Related Information**

[Embedded Memory Capacity in Arria V Devices](#) on page 20

Lists the embedded memory capacity for each device.

## Variable-Precision DSP Block

Arria V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18, 27 x 27, and 36 x 36 bits natively
- A 64-bit accumulator
- Double accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Dynamic coefficients
- 18-bit internal coefficient register banks
- Enhanced independent multiplier operation
- Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Quartus Prime design software

**Table 14: Variable-Precision DSP Block Configurations for Arria V Devices**

Usage Example	Multiplier Size (Bit)	DSP Block Resource
Low precision fixed point for video applications	Three 9 x 9	1
Medium precision fixed point in FIR filters	Two 18 x 18	1
FIR filters	Two 18 x 18 with accumulate	1
Single-precision floating-point implementations	One 27 x 27	1
Very high precision fixed point implementations	One 36 x 36	2

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 18, or one 27 x 27 multipliers. Using two DSP block resources, you can also configure a 36 x 36 multiplier for high-precision applications. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

Variant	Member Code	M20K		M10K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Arria V ST	D3	—	—	1,729	17,290	3223	2,014	19,304
	D5	—	—	2,282	22,820	4253	2,658	25,478

## Embedded Memory Configurations

**Table 17: Supported Embedded Memory Block Configurations for Arria V Devices**

This table lists the maximum configurations supported for the embedded memory blocks. The information is applicable only to the single-port RAM and ROM modes.

Memory Block	Depth (bits)	Programmable Width
MLAB	32	x16, x18, or x20
	64 <sup>(11)</sup>	x10
M20K	512	x40
	1K	x20
	2K	x10
	4K	x5
	8K	x2
	16K	x1
M10K	256	x40 or x32
	512	x20 or x16
	1K	x10 or x8
	2K	x5 or x4
	4K	x2
	8K	x1

## Clock Networks and PLL Clock Sources

650 MHz Arria V devices have 16 global clock networks capable of up to operation. The clock network architecture is based on Altera's global, quadrant, and peripheral clock structure. This clock structure is supported by dedicated clock input pins and fractional PLLs.

**Note:** To reduce power consumption, the Quartus Prime software identifies all unused sections of the clock network and powers them down.

<sup>(11)</sup> Available for Arria V GZ devices only.

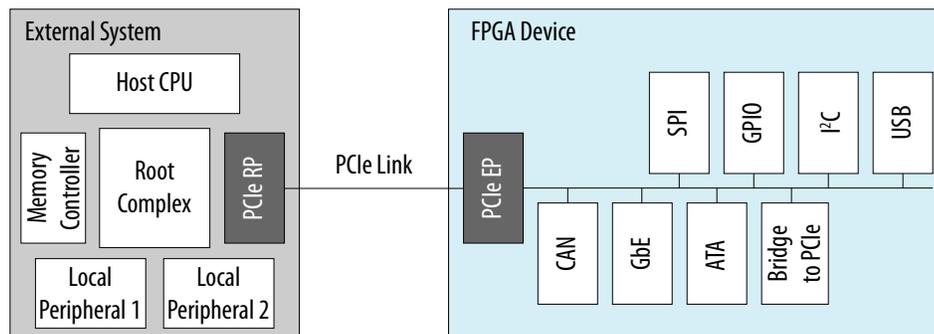
## PCIe Gen1, Gen2, and Gen 3 Hard IP

Arria V devices contain PCIe hard IP that is designed for performance and ease-of-use. The PCIe hard IP consists of the MAC, data link, and transaction layers.

The PCIe hard IP supports PCIe Gen3, Gen 2, and Gen 1 end point and root port for up to x8 lane configuration.

The PCIe endpoint support includes multifunction support for up to eight functions, as shown in the following figure. The integrated multifunction support reduces the FPGA logic requirements by up to 20,000 LEs for PCIe designs that require multiple peripherals.

**Figure 8: PCIe Multifunction for Arria V Devices**



The Arria V PCIe hard IP operates independently from the core logic. This independent operation allows the PCIe link to wake up and complete link training in less than 100 ms while the Arria V device completes loading the programming file for the rest of the device.

In addition, the PCIe hard IP in the Arria V device provides improved end-to-end datapath protection using ECC.

## External Memory Interface

This section provides an overview of the external memory interface in Arria V devices.

### Hard and Soft Memory Controllers

Arria V GX,GT, SX, and ST devices support up to four hard memory controllers for DDR3 and DDR2 SDRAM devices. Each controller supports 8 to 32 bit components of up to 4 gigabits (Gb) in density with two chip selects and optional ECC. For the Arria V SoC devices, an additional hard memory controller in the HPS supports DDR3, DDR2, and LPDDR2 SDRAM devices.

All Arria V devices support soft memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices, QDR II+, QDR II, and DDR II+ SRAM devices, and RLDRAM II devices for maximum flexibility.

**Note:** DDR3 SDRAM leveling is supported only in Arria V GZ devices.

## External Memory Performance

Table 18: External Memory Interface Performance in Arria V Devices

Interface	Voltage (V)	Hard Controller (MHz)	Soft Controller (MHz)	
		Arria V GX, GT, SX, and ST	Arria V GX, GT, SX, and ST	Arria V GZ
DDR3 SDRAM	1.5	533	667	800
	1.35	533	600	800
DDR2 SDRAM	1.8	400	400	400
LPDDR2 SDRAM	1.2	—	400	—
RLDRAM 3	1.2	—	—	667
RLDRAM II	1.8	—	400	533
	1.5	—	400	533
QDR II+ SRAM	1.8	—	400	500
	1.5	—	400	500
QDR II SRAM	1.8	—	400	333
	1.5	—	400	333
DDR II+ SRAM <sup>(12)</sup>	1.8	—	400	—
	1.5	—	400	—

### Related Information

#### [External Memory Interface Spec Estimator](#)

For the latest information and to estimate the external memory system performance specification, use Altera's External Memory Interface Spec Estimator tool.

## HPS External Memory Performance

Table 19: HPS External Memory Interface Performance

The hard processor system (HPS) is available in Arria V SoC devices only.

Interface	Voltage (V)	HPS Hard Controller (MHz)
DDR3 SDRAM	1.5	533
	1.35	533
LPDDR2 SDRAM	1.2	333

<sup>(12)</sup> Not available as Altera® IP.

Figure 9: Device Chip Overview for Arria V GX and GT Devices

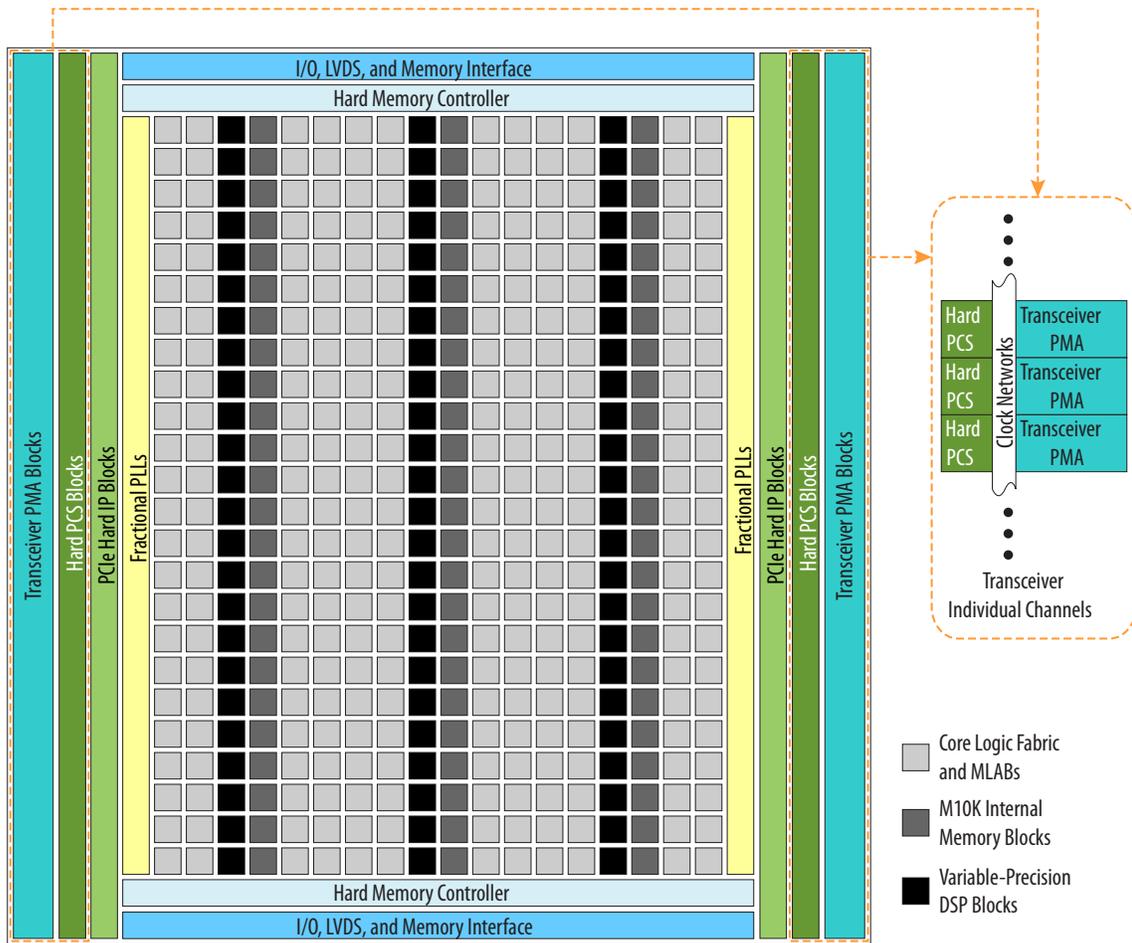
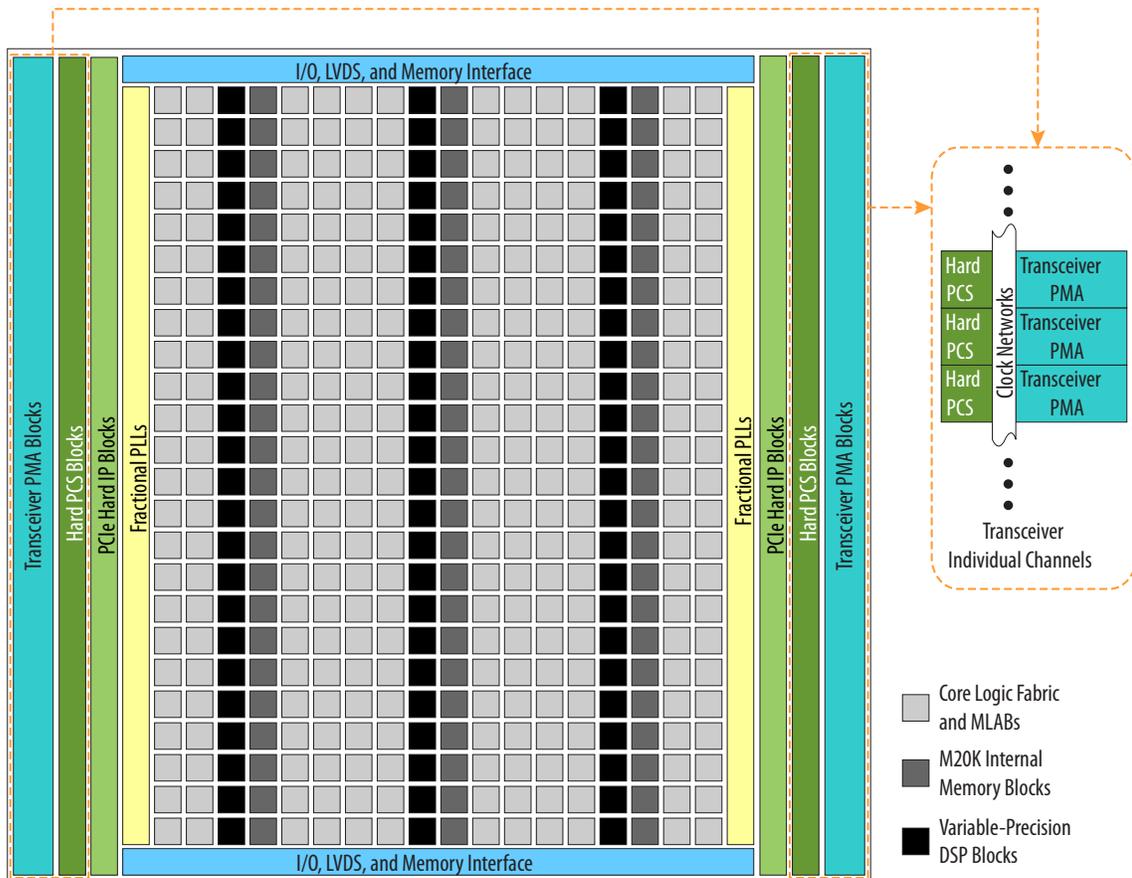


Figure 10: Device Chip Overview for Arria V GZ Devices



Features	Capability
PLL-based clock recovery	Superior jitter tolerance
Programmable serializer and deserializer (SERDES)	Flexible SERDES width
Equalization and pre-emphasis	<ul style="list-style-type: none"> <li>• Arria V GX, GT, SX, and ST devices—Up to 14.37 dB of pre-emphasis and up to 4.7 dB of equalization</li> <li>• Arria V GZ devices—4-tap pre-emphasis and de-emphasis</li> </ul>
Ring oscillator transmit PLLs	611 Mbps to 10.3125 Gbps
LC oscillator ATX transmit PLLs (Arria V GZ devices only)	600 Mbps to 12.5 Gbps
Input reference clock range	27 MHz to 710 MHz
Transceiver dynamic reconfiguration	Allows the reconfiguration of a single channel without affecting the operation of other channels

## PCS Features

The Arria V core logic connects to the PCS through an 8, 10, 16, 20, 32, 40, 64, 66, or 67 bit interface, depending on the transceiver data rate and protocol. Arria V devices contain PCS hard IP to support PCIe Gen1, Gen2, and Gen3, GbE, Serial RapidIO (SRIO), GPON, and CPRI.

All other standard and proprietary protocols within the following speed ranges are also supported:

- 611 Mbps to 6.5536 Gbps—supported through the custom double-width mode (up to 6.5536 Gbps) and custom single-width mode (up to 3.75 Gbps) of the transceiver PCS hard IP.
- 6.5536 Gbps to 10.3125 Gbps—supported through dedicated 80 or 64 bit interface that bypass the PCS hard IP and connects the PMA directly to the core logic. In Arria V GZ, this is supported in the transceiver PCS hard IP.

**Table 21: Transceiver PCS Features for Arria V GX, GT, ST, and SX Devices**

PCS Support <sup>(13)</sup>	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
Custom single- and double-width modes	0.611 to ~6.5536	<ul style="list-style-type: none"> <li>• Phase compensation FIFO</li> <li>• Byte serializer</li> <li>• 8B/10B encoder</li> </ul>	<ul style="list-style-type: none"> <li>• Word aligner</li> <li>• 8B/10B decoder</li> <li>• Byte deserializer</li> <li>• Phase compensation FIFO</li> </ul>
SRIO	1.25 to 6.25		
Serial ATA	1.5, 3.0, 6.0		

<sup>(13)</sup> Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through the soft PCS.

Protocol	Data Rates (Gbps)	Transmitter Data Path Features	Receiver Data Path Features
40GBASE-R Ethernet	4 x 10.3125	<ul style="list-style-type: none"> <li>TX FIFO</li> <li>64B/66B encoder</li> <li>Scrambler</li> <li>Alignment marker insertion</li> <li>Gearbox</li> <li>Block stripper</li> </ul>	<ul style="list-style-type: none"> <li>RX FIFO</li> <li>64B/66B decoder</li> <li>Descrambler</li> <li>Lane reorder</li> <li>Deskew</li> <li>Alignment marker lock</li> <li>Block synchronization</li> <li>Gear box</li> <li>Destripper</li> </ul>
100GBASE-R Ethernet	10 x 10.3125		
40G and 100G OTN	(4 +1) x 11.3	<ul style="list-style-type: none"> <li>TX FIFO</li> <li>Channel bonding</li> <li>Byte serializer</li> </ul>	<ul style="list-style-type: none"> <li>RX FIFO</li> <li>Lane deskew</li> <li>Byte deserializer</li> </ul>
	(10 +1) x 11.3		
GbE	1.25	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> <li>8B/10B encoder</li> <li>Bit-slip</li> <li>Channel bonding</li> <li>GbE state machine</li> </ul>	<ul style="list-style-type: none"> <li>Word aligner</li> <li>Deskew FIFO</li> <li>Rate match FIFO</li> <li>8B/10B decoder</li> <li>Byte deserializer</li> <li>Byte ordering</li> <li>GbE state machine</li> </ul>
XAUI	3.125 to 4.25	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> <li>8B/10B encoder</li> <li>Bit-slip</li> <li>Channel bonding</li> <li>XAUI state machine for bonding four channels</li> </ul>	<ul style="list-style-type: none"> <li>Word aligner</li> <li>Deskew FIFO</li> <li>Rate match FIFO</li> <li>8B/10B decoder</li> <li>Byte deserializer</li> <li>Byte ordering</li> <li>XAUI state machine for realigning four channels</li> </ul>
SRIO	1.25 to 6.25	<ul style="list-style-type: none"> <li>Phase compensation FIFO</li> <li>Byte serializer</li> <li>8B/10B encoder</li> <li>Bit-slip</li> <li>Channel bonding</li> <li>SRIO V2.1-compliant x2 and x4 channel bonding</li> </ul>	<ul style="list-style-type: none"> <li>Word aligner</li> <li>Deskew FIFO</li> <li>Rate match FIFO</li> <li>8B/10B decoder</li> <li>Byte deserializer</li> <li>Byte ordering</li> <li>SRIO V2.1-compliant x2 and x4 deskew state machine</li> </ul>

## SoC with HPS

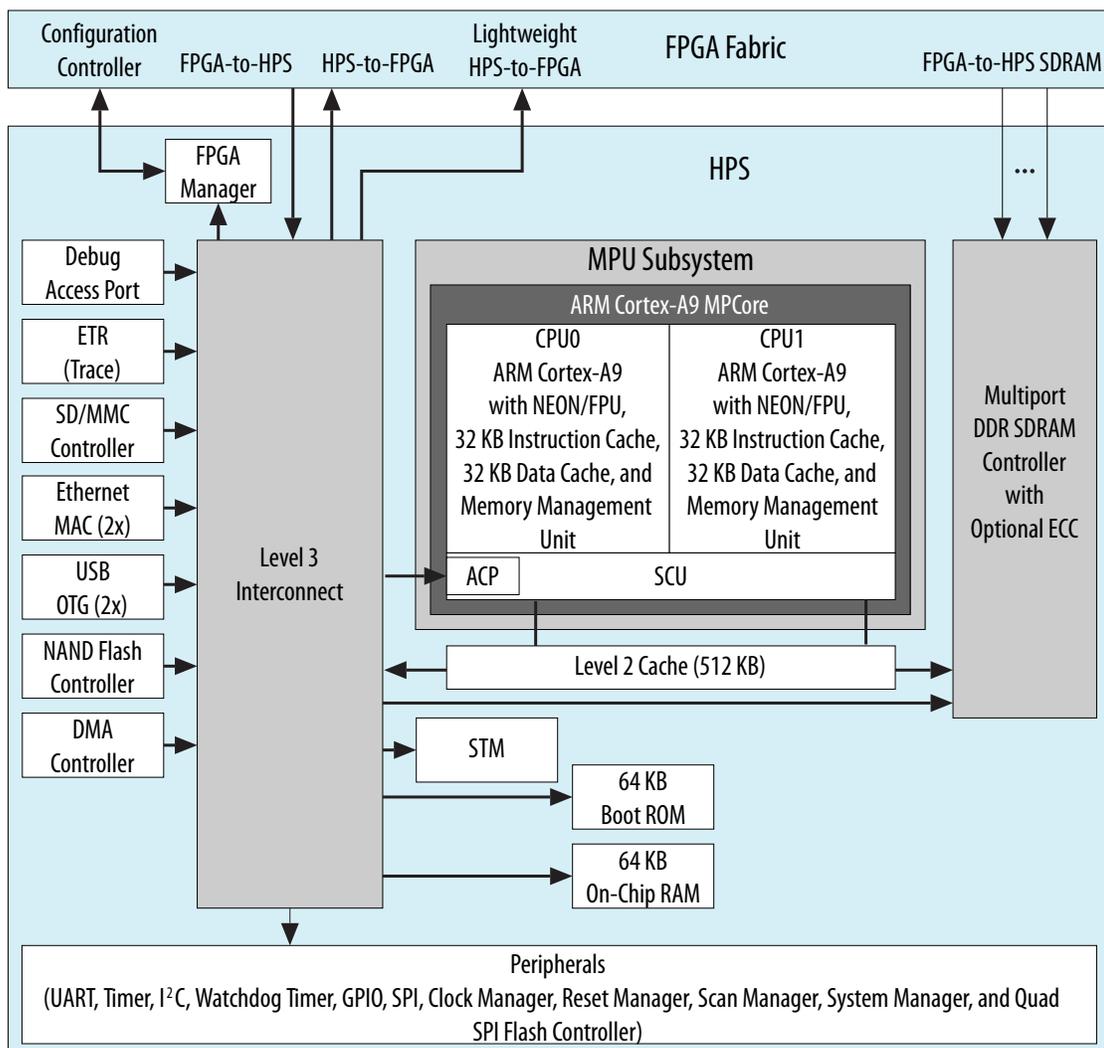
Each SoC combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

## HPS Features

The HPS consists of a dual-core ARM Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in the following figure.

Figure 12: HPS with Dual-Core ARM Cortex-A9 MPCore Processor



## Partial Reconfiguration

**Note:** Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

Partial reconfiguration allows you to reconfigure part of the device while other sections of the device remain operational. This capability is important in systems with critical uptime requirements because it allows you to make updates or adjust functionality without disrupting services.

Apart from lowering cost and power consumption, partial reconfiguration increases the effective logic density of the device because placing device functions that do not operate simultaneously is not necessary. Instead, you can store these functions in external memory and load them whenever the functions are required. This capability reduces the size of the device because it allows multiple applications on a single device—saving the board space and reducing the power consumption.

Altera simplifies the time-intensive task of partial reconfiguration by building this capability on top of the proven incremental compile and design flow in the Quartus Prime design software. With the Altera solution, you do not need to know all the intricate device architecture details to perform a partial reconfiguration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable simultaneous partial reconfiguration of both the device core and transceivers.

## Enhanced Configuration and Configuration via Protocol

**Table 23: Configuration Modes and Features of Arria V Devices**

Arria V devices support 1.8 V, 2.5 V, 3.0 V, and 3.3 V<sup>(19)</sup> programming voltages and several configuration modes.

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompression	Design Security	Partial Reconfiguration <sup>(20)</sup>	Remote System Update
AS through the EPCS and EPCQ serial configuration device	1 bit, 4 bits	100	—	Yes	Yes	—	Yes
PS through CPLD or external microcontroller	1 bit	125	125	Yes	Yes	—	—

<sup>(19)</sup> Arria V GZ does not support 3.3 V.

<sup>(20)</sup> Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompression	Design Security	Partial Reconfiguration <sup>(20)</sup>	Remote System Update
FPP	8 bits	125	—	Yes	Yes	—	Parallel flash loader
	16 bits	125	—	Yes	Yes	Yes <sup>(21)</sup>	
	32 bits <sup>(22)</sup>	100	—	Yes	Yes	—	
CvP (PCIe)	x1, x2, x4, and x8 lanes	—	—	Yes	Yes	Yes	—
JTAG	1 bit	33	33	—	—	—	—
Configuration via HPS	16 bits	125	—	Yes	Yes	Yes <sup>(21)</sup>	Parallel flash loader
	32 bits	100	—	Yes	Yes	—	

Instead of using an external flash or ROM, you can configure the Arria V devices through PCIe using CvP. The CvP mode offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. The Arria V CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

**Note:** Although Arria V GZ devices support PCIe Gen3, you can use only PCIe Gen1 and PCIe Gen2 for CvP configuration scheme.

#### Related Information

#### [Configuration via Protocol \(CvP\) Implementation in Altera FPGAs User Guide](#)

Provides more information about CvP.

## Power Management

Leveraging the FPGA architectural features, process technology advancements, and transceivers that are designed for power efficiency, the Arria V devices consume less power than previous generation Arria V FPGAs:

- Total device core power consumption—less by up to 50%.
- Transceiver channel power consumption—less by up to 50%.

Additionally, Arria V devices contain several hard IP blocks, including PCIe Gen1, Gen2, and Gen3, GbE, SRIO, GPON, and CPRI protocols, that reduce logic resources and deliver substantial power savings of up to 25% less power than equivalent soft implementations.

<sup>(20)</sup> Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.

<sup>(21)</sup> Supported at a maximum clock rate of 62.5 MHz.

<sup>(22)</sup> Arria V GZ only

Date	Version	Changes
June 2013	2013.06.03	<ul style="list-style-type: none"> <li>Removed statements about contacting Altera for SFF-8431 compliance requirements. Refer to the <a href="#">Transceiver Architecture in Arria V Devices</a> chapter for the requirements.</li> </ul>
May 2013	2013.05.06	<ul style="list-style-type: none"> <li>Moved all links to the Related Information section of respective topics for easy reference.</li> <li>Added link to the known document issues in the Knowledge Base.</li> <li>Updated the available options, maximum resource counts, and per package information for the Arria V SX and ST device variants.</li> <li>Updated the variable DSP multipliers counts for the Arria V SX and ST device variants.</li> <li>Clarified that partial reconfiguration is an advanced feature. Contact Altera for support of the feature.</li> <li>Added footnote to clarify that MLAB 64 bits depth is available only for Arria V GZ devices.</li> <li>Updated description about power-up sequence requirement for device migration to improve clarity.</li> </ul>
January 2013	2013.01.11	<ul style="list-style-type: none"> <li>Added the L optional suffix to the Arria V GZ ordering code for the – I3 speed grade.</li> <li>Added a note about the power-up sequence requirement if you plan to migrate your design from the Arria V GX A5 and A7, and Arria V GT C7 devices to other Arria V devices.</li> </ul>
November 2012	2012.11.19	<ul style="list-style-type: none"> <li>Updated the summary of features.</li> <li>Updated Arria V GZ information regarding 3.3 V I/O support.</li> <li>Removed Arria V GZ engineering sample ordering code.</li> <li>Updated the maximum resource counts for Arria V GX and GZ.</li> <li>Updated Arria V ST ordering codes for transceiver count.</li> <li>Updated transceiver counts for Arria V ST packages.</li> <li>Added simplified floorplan diagrams for Arria V GZ, SX, and ST.</li> <li>Added FPP x32 configuration mode for Arria V GZ only.</li> <li>Updated CvP (PCIe) remote system update support information.</li> <li>Added HPS external memory performance information.</li> <li>Updated template.</li> </ul>
October 2012	3.0	<ul style="list-style-type: none"> <li>Added Arria V GZ information.</li> <li>Updated Table 1, Table 2, Table 3, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, and Table 21.</li> <li>Added the “Arria V GZ” section.</li> <li>Added Table 8, Table 9 and Table 22.</li> </ul>