Zilog - EZ80190AZ050SG Datasheet

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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	eZ80
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	50MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	100-LQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/ez80190az050sg

Table 1. 100-Pin LQFP Pin Identification of the eZ80190 Device (Continued)

Pin No.	Symbol	Function	Signal Direction	Description
50	NMI	Nonmaskable Interrupt	Schmitt Trigger Input, Active Low	The $\overline{\text{NMI}}$ input is prioritized higher than the maskable interrupts. It is always recognized at the end of an instruction, regardless of the state of the interrupt enable control bits. This input includes a Schmitt trigger to allow RC rise times. This external $\overline{\text{NMI}}$ signal is combined with an internal $\overline{\text{NMI}}$ signal generated from the WDT block before being connected to the $\overline{\text{NMI}}$ input of the CPU.
51	HALT	Halt	Output, Active Low	A Low on this pin indicates the CPU has stopped because a HALT instruction is executed.
52	INSTRD	Instruction READ	Output, Active Low, tristate	$\overline{\text{INSTRD}}$ (with $\overline{\text{MREQ}}$ and $\overline{\text{RD}}$) indicates the eZ80190 device is fetching an instruction from code memory. The eZ80190 device does not drive this line during Reset or bus acknowledge cycles.
53	IORQ	Input/Output Request	Input/Output, Active Low	$\overline{\text{IORQ}}$ indicates the CPU is accessing a location in I/O space. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ indicate the type of access. The eZ80190 device does not drive this line during Reset and is an input in bus acknowledge cycles.
54	RESET	Reset	Schmitt Trigger Input, Active Low	This signal is used to initialize the eZ80190 device. This input must be Low for a minimum of 3 system clock cycles, and must be held Low until the clock is stable. This input includes a Schmitt trigger to allow RC rise times.
55	ZCL	ZDI Clock	Input with Pull-up	The ZCL pin is used to clock the data between the Zilog Debug Interface and the eZ80190 device. This pin features an internal pull-up.
56	ZDA	ZDI Data	Input/Output, Open-Drain with Pull-up	The ZDA pin is used to transfer data between the Zilog Debug Interface and the eZ80190 device. This pin is open-drain and features an internal pull-up.
57	PB0	GPIO Port B	Input/Output	The PB0 pin can be used for GPIO. It can be individually programmed as an input or output and can also be used individually as an interrupt input. Each Port B pin, when programmed as an output, can be selected to be an open-drain or open-source output.

Table 1. 100-Pin LQFP Pin Identification of the eZ80190 Device (Continued)

Pin No.	Symbol	Function	Signal Direction	Description
68	PC1	GPIO Port C	Input/Output	The PC1 pin can be used for GPIO. It can be individually programmed as an input or output and can also be used individually as an interrupt input. Each Port C pin, when programmed as an output, can be selected to be an open-drain or open-source output. Port C is multiplexed with one channel of the UZI interface.
	MOSI1	Master Out Slave In	Input/Output	The MOSI line is configured as an output when the eZ80190 device is an SPI master device and as an input when the eZ80190 device is an SPI slave device. This signal is multiplexed with PC1.
	RxD1	Receive Data	Input	The RxD1 pin is used by the UART to receive asynchronous serial data. This signal is multiplexed with PC1.
	SDA1	I^2C Serial Data	Input/Output	The SDA1 pin carries the I^2C data signal. This signal is multiplexed with PC1.
69	PC2	GPIO Port C	Input/Output	The PC2 pin can be used for GPIO. It can be individually programmed as an input or output and can also be used individually as an interrupt input. Each Port C pin, when programmed as an output, can be selected to be an open-drain or open-source output. Port C is multiplexed with one channel of the UZI interface.
	SCK1	SPI Serial Clock	Input/Output	SPI serial clock. This signal is multiplexed with PC2.
	RTS1	Request to Send	Output, Active Low	The $\overline{\text{RTS1}}$ pin carries the modem-control signal from the UART. This signal is multiplexed with PC2.

Table 2. Register Map (Continued)

Address (hex)	Mnemonic	Name	Reset (hex)	CPU Access	Page No.
DF	UZI1_CTL	UZI 1 Control Register	00	R/W	64
Multiply-Accumulator					
E0	MACC_*x*START	Multiply-Accumulator *x* Starting Address Register	00	R/W	134
E1	MACC_*x*END	Multiply-Accumulator *x* Ending Address Register	00	R/W	135
E2	MACC_*x*RELOAD	Multiply-Accumulator *x* Reload Register	00	R/W	137
E3	MACC_LENGTH	Multiply-Accumulator Length Register	00	R/W	138
E4	MACC_*y*START	Multiply-Accumulator *y* Starting Address Register	00	R/W	142
E5	MACC_*y*END	Multiply-Accumulator *y* Ending Address Register	00	R/W	143
E6	MACC_*y*RELOAD	Multiply-Accumulator *y* Reload Register	00	R/W	144
E7	MACC_CTL	Multiply-Accumulator Control Register	00	R/W	145
E8	MACC_AC0	Multiply-Accumulator Byte 0 Register	XX	R/W	145
E9	MACC_AC1	Multiply-Accumulator Byte 1 Register	XX	R/W	154
EA	MACC_AC2	Multiply-Accumulator Byte 2 Register	XX	R/W	155
EB	MACC_AC3	Multiply-Accumulator Byte 3 Register	XX	R/W	156
EC	MACC_AC4	Multiply-Accumulator Byte 4 Register	XX	R/W	156
ED	MACC_STAT	Multiply-Accumulator Status Register	XX	R/W	159
DMA Controllers					
EE	DMA0_SAR_L	DMA0 Source Address Register—Low Byte	XX	R/W	163
EF	DMA0_SAR_H	DMA0 Source Address Register—High Byte	XX	R/W	163
F0	DMA0_SAR_U	DMA0 Source Address Upper Byte Register	XX	R/W	163
F1	DMA0_DAR_L	DMA0 Destination Address Register—Low Byte	XX	R/W	163
F2	DMA0_DAR_H	DMA0 Destination Address Register—High Byte	XX	R/W	163

Table 3. PRT Single-Pass Mode Operation Example

Parameter	Control Register(s)	Value
PRT Enabled	TMRx_CTL[0]	1
Reload and Restart Enabled	TMRx_CTL[1]	1
PRT Clock Divider = 2	TMRx_CTL[3:2]	00b
Single-Pass Mode	TMRx_CTL[4]	0
PRT Interrupt Enabled	TMRx_CTL[6]	0
PRT Reload Value	{TMRx_RR_H, TMRx_RR_L}	0004h

CONTINUOUS Mode

In CONTINUOUS mode, when the end-of-count value, 0000h, is reached, the timer automatically reloads the 16-bit start value from the Timer Reload registers, TMRx_RR_H and TMRx_RR_L. Downcounting continues on the next clock edge. In CONTINUOUS mode, the PRT continues to count until disabled. Figure 5 displays an example of a PRT operating in CONTINUOUS mode. Timer register information is listed in Table 4.

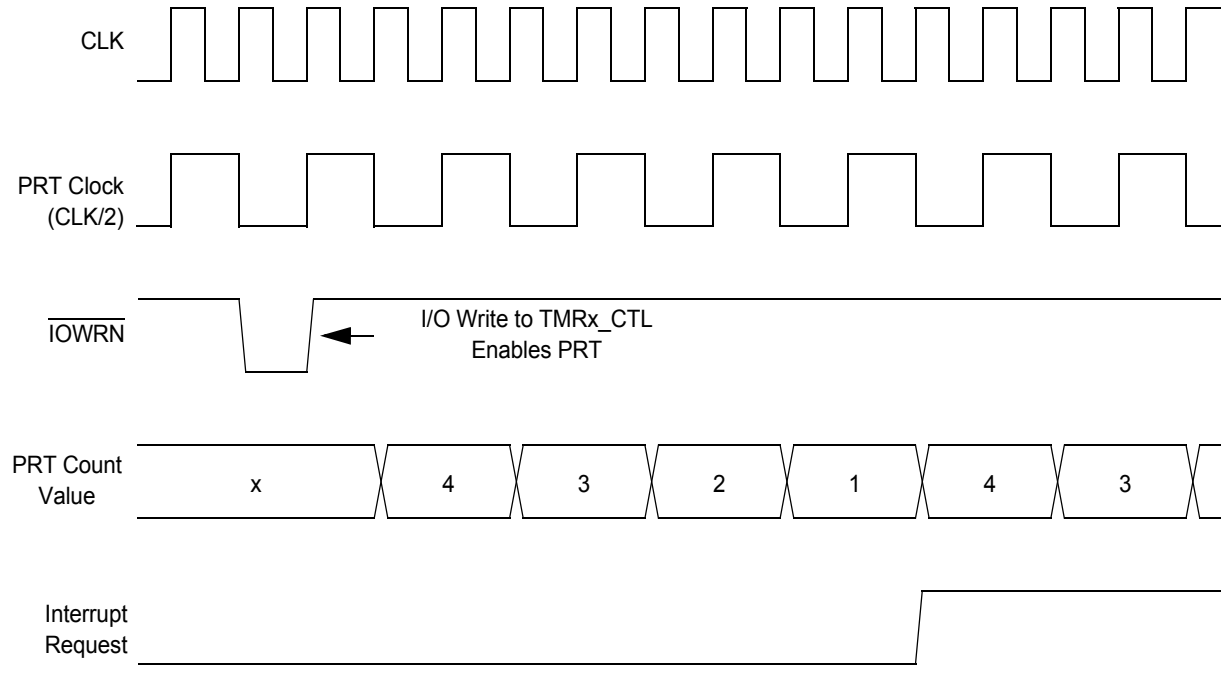

Figure 5. PRT Continuous Mode Operation Example

Table 18. Chip Select x Lower Bound Register (CS0_LBR = A8h, CS1_LBR = ABh, CS2_LBR = AEh, CS3_LBR = B1h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
[7:0] CS_LBR	00h–FFh	**For Memory Chip Selects (CS_io = 0)** This bit specifies the lower bound of the Chip Select address range. The upper byte of the address bus, ADDR[23:16], is compared to the values contained in these registers for determining if a Memory Chip Select signal should be generated.
		For I/O Chip Selects (CS_io = 1) This bit specifies the Chip Select address value. ADDR[11:4] is compared to the values contained in these registers for determining if an I/O Chip Select signal should be generated.

Chip Select x Upper Bound Register

For Memory Chip Selects, the Chip Select *x* Upper Bound register, listed in Table 19, defines the upper bound of the address range for which the corresponding Chip Select (if enabled) can be active. For I/O Chip Selects, this register produces no effect. The reset state for the Chip Select 0 Upper Bound register is FFh, while the reset state for the 3 other Chip Select upper bound registers is 00h.

Table 19. Chip Select x Upper Bound Register (CS0_UBR = A9h, CS1_UBR = ACh, CS2_UBR = AFh, CS3_UBR = B2h)

Bit	7	6	5	4	3	2	1	0
CS0 Reset	1	1	1	1	1	1	1	1
CS1 Reset	0	0	0	0	0	0	0	0
CS2 Reset	0	0	0	0	0	0	0	0
CS3 Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

- Clear UARTx_LCTL[7] to 0 to disable access of the BRG divisor registers.

UZI and BRG Control Registers

UZI Control Registers

The UZI Control registers select between the three available serial communication controllers: I^2C, SPI and UART. Each of the two UZI devices on the eZ80190 device features its own UZI Control register.

Table 23. UZI Control Registers (UZI0_CTL=CFh, UZI1_CTL=DFh)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R	R	R	R	R	R	R/W	R/W

Note: R = Read Only; R/W = Read/Write.

Bit Position	Value	Description
[7:2]	000000	Reserved
[1:0] UZI_MODE	00	All UZI devices are disabled.
	01	UART is enabled.
	10	SPI is enabled.
	11	I^2C is enabled.

BRG Divisor Latch Registers—Low Byte

This register holds the Low byte of the 16-bit divisor count loaded by the processor for baud rate generation. The 16-bit clock divisor value is returned by {BRGx_DLR_H, BRGx_DLR_L}, where x is either 0 or 1 to identify the two available UZI devices. Upon RESET, the 16-bit BRG divisor value resets to 0002h. The initial 16-bit divisor value must be between 0002h and FFFFh as the values 0000h and 0001h are invalid and proper operation is not guaranteed. Thus the minimum BRG clock divisor ratio is 2.

A write to either the Low or High byte registers for the BRG Divisor Latch causes both bytes to be loaded into the BRG counter and the count restarted.

Bit 7 of the associated UART Line Control register (UARTx_LCTL) must be set to 1 to access this register for each UZI device. For more information see UART Line Control Register on page 77 (UARTx_LCTL).

I²C Slave Address Register

The I2Cx_SAR register, indicated in Table 49, lists the 7-bit address of the I²C when in SLAVE mode and allows 10-bit addressing in conjunction with the I2Cx_xSAR register. I2Cx_SAR[7:1] = SLA[6:0] is the 7-bit address of the I²C when in 7-bit SLAVE mode. When the I²C receives this address after a START condition, it enters SLAVE mode. I2Cx_SAR[7] corresponds to the first bit received from the I²C bus.

When the register receives an address starting with F7h to F0h (I2Cx_SAR[7:3] = 11110b), the I²C recognizes that a 10-bit slave addressing mode is being selected. The I²C sends an ACK after receiving the I2Cx_SAR byte (the device does not generate an interrupt at this point). After the next byte of the address (I2Cx_*x*SAR) is received, the I²C generates an interrupt and enters SLAVE mode. Then I2Cx_SAR[2:1] is used as the upper 2 bits of the 10-bit extended address. The full 10-bit address is returned by {I2Cx_SAR[2:1], I2Cx_*x*SAR[7:0]}.

Table 49. I²C Slave Address Registers (I2C0_SAR = C8h, I2C1_SAR = D8h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
[7:1] SLA	00h–7Fh	The 7-bit slave address, or the lower 7 bits of the slave address, when operating in 10-bit mode.
0 GCE	0	The I²C is not enabled to recognize the General Call Address.
	1	The I²C is enabled to recognize the General Call Address.

I²C Extended Slave Address Register

The I2Cx_*x*SAR register, listed in Table 50, is used in conjunction with the I2Cx_SAR register to provide 10-bit addressing for the I²C when in SLAVE mode. The I2Cx_SAR value forms the lower 8 bits of the 10-bit slave address. The full 10-bit address is returned by {I2Cx_SAR[2:1], I2Cx_*x*SAR[7:0]}.

When the register receives an address starting with F7h to F0h (I2Cx_SAR[7:3] = 11110b), the I²C recognizes that a 10-bit slave addressing mode is being selected. The I²C sends an ACK after receiving the I2Cx_SAR byte (the device does not generate an interrupt at this point). After the next byte of the address (I2Cx_*x*SAR) is received, the I²C generates an interrupt and enters SLAVE mode. Then I2Cx_SAR[2:1] is used as the upper 2 bits of the 10-bit extended address. The full 10-bit address is returned by {I2Cx_SAR[2:1], I2Cx_*x*SAR[7:0]}.

To ensure correct detection of START and STOP conditions on the bus, the I^2C must sample the I^2C bus at least ten times faster than the bus clock speed of the fastest master on the bus. The sampling frequency should therefore be at least 1 MHz (4 MHz in FAST mode) to guarantee correct operation with other bus masters.

The I^2C sampling frequency is determined by the frequency of the eZ80190 device system clock and the value in the I2Cx_CCR bits 2 to 0. The bus clock speed generated by the I^2C in MASTER mode is determined by the frequency of the input clock and the values in I2Cx_CCR[2:0] and I2Cx_CCR[6:3].

I^2C Software Reset Register

The I2Cx_SRR register, listed in Table 56 on page 112, is a Write Only register. Writing any value to this register will perform a software reset of the I^2C module.

Table 56. I^2C Software Reset Register (I2C0_SRR = CDh, I2C1_SRR = DDh)

Bit	7	6	5	4	3	2	1	0
Reset	X	X	X	X	X	X	X	X
CPU Access	W	W	W	W	W	W	W	W

Note: W = Write Only.

Bit Position	Value	Description
[7:0] SRR	00h–FFh	Writing any value to this register performs a software reset of the I^2C module.

Bit Position	Value	Description
[7:0] MACC_*x*RELOAD	00h–FFh	The reload address for MACC RAM *x* DATA.

MACC Length Register

The MACC_LENGTH register, listed in Table 63, defines the total number of *x* and *y* data pairs that are multiplied and accumulated for the MACC operation.

Table 63. MACC Length Register (MACC_LENGTH = E3h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
[7:0] MACC_LENGTH	00h–FFh	Total number of address pairs to be multiplied and accumulated for the current MACC operation.

MACC *y* DATA Starting Address Register

The MACC_*y*START register, listed in Table 64, defines the starting address for the MACC to read 16-bit values from the *y* DATA for performing its calculations.

Table 64. MACC *y* DATA Starting Address Register (MACC_*y*START = E4h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
[7:0] MACC_*y*START	00h–FFh	Starting address for the *y* DATA of MACC RAM.

MACC *y* DATA Ending Address Register

The MACC_*y*END register, listed in Table 65 on page 130, defines the ending address for the MACC to read 16-bit values from the *y* DATA for performing its calculations.

Table 65. MACC *y* DATA Ending Address Register (MACC_*y*END = E5h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
[7:0] MACC_*y*END	00h–FFh	Ending address for the *y* DATA of MACC RAM.

MACC *y* DATA Reload Address Register

The MACC_*y*RELOAD register, listed in Table 66, defines the reload address within the *y* DATA of MACC RAM. When the *y* DATA address increments to the value in MACC_*y*END, the next *y* DATA address is taken from this MACC_*y*RELOAD register.

Table 66. MACC *y* DATA Reload Address Register (MACC_*y*RELOAD = E6h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
[7:0] MACC_*y*RELOAD	00h–FFh	Reload address for the *y* DATA of MACC RAM.

MACC Control Register

The MACC Control register, listed in Table 67, provides added MACC features including interrupt enable on completion of calculation. All writes to this register clear the 40-bit accumulator to 0 (MACC_ACx = 00h}.

Table 67. MACC Control Register (MACC_CTL = E7h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: R/W = Read/Write.

Bit Position	Value	Description
7 MACC_IE	0	MACC interrupt is disabled.
	1	The MACC interrupt is enabled for the calculation currently being defined. The MACC generates an interrupt request to the CPU when it completes this calculation (DONE).
6 NOISE	0	All NOISE bits added to the accumulator using IN_SHIFT are 0.
	1	All NOISE bits added to the accumulator using IN_SHIFT are 1.
[5:3] OUT_SHIFT	000	No right-shift is performed during READs from the MACC Accumulator registers by the CPU. DATA_OUT[40:0] = MACC_ACx[39:0].
	001	Reads from the MACC Accumulator registers by the CPU are right-shifted by 1 bit with a fill by the sign bit (msb = bit 39). DATA_OUT[40:0] = {2{MACC_ACx[39]}, MACC_ACx[38:1]}.
	010	Reads from the MACC Accumulator registers by the CPU are right-shifted by 2 bits with a fill by the sign bit (msb = bit 39). DATA_OUT[40:0] = {3{MACC_ACx[39]}, MACC_ACx[38:2]}.
	011	Reads from the MACC Accumulator registers by the CPU are right-shifted by 3 bits with a fill by the sign bit (msb = bit 39). DATA_OUT[40:0] = {4{MACC_ACx[39]}, MACC_ACx[38:3]}.
	100	Reads from the MACC Accumulator registers by the CPU are right-shifted by 4 bits with a fill by the sign bit (msb = bit 39). DATA_OUT[40:0] = {5{MACC_ACx[39]}, MACC_ACx[38:4]}.
	101	Reads from the MACC Accumulator registers by the CPU are right-shifted by 5 bits with a fill by the sign bit (msb = bit 39). DATA_OUT[40:0] = {6{MACC_ACx[39]}, MACC_ACx[38:5]}.
	110	Reads from the MACC Accumulator registers by the CPU are right-shifted by 6 bits with a fill by the sign bit (msb = bit 39). DATA_OUT[40:0] = {7{MACC_ACx[39]}, MACC_ACx[38:6]}.
	111	Reads from the MACC Accumulator registers by the CPU are right-shifted by 7 bits with a fill by the sign bit (msb = bit 39). DATA_OUT[40:0] = {8{MACC_ACx[39]}, MACC_ACx[38:7]}.

MACC Status Register

The MACC_STAT register, listed in Table 73, reflects the current status of the Multiply-Accumulator. Writing a value of 80h to the MACC_STAT register when the CALC bank has completed its calculation (DONE) and the DATA register is not loaded with a new calculation (EMPTY) swaps the banks to allow the pending result to be retrieved.

The eZ80190 device uses two distinct numbered banks, banks 0 and 1. The value in bit 4 of the MACC_STAT register indicates which of these two banks is currently accessible as the DATA bank. In general, there is no requirement for software to monitor which numbered bank is currently the DATA bank and which is the CALC bank.

Table 73. MACC Status Register (MACC_STAT = EDh)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	W	R	R	R	R	R	R	R

Note: R = Read; W = Write.

Bit Position	Value	Description
[7:5]	000	Reserved.
4 BANK	0	The current DATA bank is Bank 0. The current DATA bank is always reset to Bank 0 when both banks are EMPTY.
	1	The current CALC bank is Bank 1.
[3:2] CALC_STAT	00	The CALC bank is EMPTY. No calculation is set up for execution.
	01	Invalid.
	10	The CALC bank is IN PROGRESS. The MACC is currently executing on a data set.
	11	The CALC bank is DONE. The MACC has completed execution of the operations defined by the CALC bank control registers. The result is stored in the CALC bank accumulator registers. The CALC bank must be swapped with the DATA bank to allow the CPU to access the result.

Table 97. Block Transfer and Compare Instructions

Mnemonic	Instruction
CPD (CPDR)	Compare and Decrement (with Repeat)
CPI (CPIR)	Compare and Increment (with Repeat)
LDD (LDDR)	Load and Decrement (with Repeat)
LDI (LDIR)	Load and Increment (with Repeat)

Table 98. Exchange Instructions

Mnemonic	Instruction
EX	Exchange registers
EXX	Exchange CPU Multibyte register banks

Table 99. Input/Output Instructions

Mnemonic	Instruction
IN	Input from I/O
IN0	Input from I/O on Page 0
IND (INDR)	Input from I/O and Decrement (with Repeat)
IND2 (IND2R)	Input from I/O and Decrement (with Repeat)
INDM (INDMR)	Input from I/O and Decrement (with Repeat)
INI (INIR)	Input from I/O and Increment (with Repeat)
INI2 (INI2R)	Input from I/O and Increment (with Repeat)
INIM (INIMR)	Input from I/O and Increment (with Repeat)
OTDM (OTDMR)	Output to I/O and Decrement (with Repeat)
OTIM (OTIMR)	Output to I/O and Increment (with Repeat)
OUT	Output to I/O
OUT0	Output to I/0 on Page 0
OUTD (OTDR)	Output to I/O and Decrement (with Repeat)
OUTD2 (OTD2R)	Output to I/O and Decrement (with Repeat)

Table 99. Input/Output Instructions (Continued)

Mnemonic	Instruction
OUTI (OTIR)	Output to I/O and Increment (with Repeat)
OUTI2 (OTI2R)	Output to I/O and Increment (with Repeat)
TSTIO	Test I/O

Table 100. Load Instructions

Mnemonic	Instruction
LD	Load
LEA	Load Effective Address
PEA	Push Effective Address
POP	Pop
PUSH	Push

Table 101. Logical Instructions

Mnemonic	Instruction
AND	Logical AND
CPL	Complement Accumulator
OR	Logical OR
TST	Test Accumulator
XOR	Logical Exclusive OR

Table 102. Processor Control Instructions

Mnemonic	Instruction
CCF	Complement Carry Flag
DI	Disable Interrupts
EI	Enable Interrupts
HALT	Halt

DC Characteristics

Table 113 lists the Direct Current characteristics of the eZ80190 device.

Table 113. DC Characteristics

		Standard Temperature Range = 0 °C to 70 °C		Extended Temperature Range = –40 °Cto 105 °C			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Conditions**
V_{DD}	Supply Voltage	3.0	3.6	3.0	3.6	V	
V_{IL}	Low Level Input Voltage	–0.3	0.8V	–0.3	0.8V	V	
V_{IH}	High Level Input Voltage	$0.7xV_{DD}$	5.5	$0.7xV_{DD}$	5.5	V	
V_{OL}	Low Level Output Voltage		0.4		0.4	V	V_{DD} = 3.0 V; I_{OL} = 1 mA
V_{OH}	High Level Output Voltage	2.4		2.4		V	V_{DD} = 3.0 V; I_{OH} = ,— mA
I_{IL}	Input Leakage Current	–10	+10	–10	+10	µA	V_{DD} = 3.6 V; V_{IN} = V_{DD} or V_{SS}*
I_{TL}	Tri-State Leakage Current	–10	+10	–10	+10	µA	V_{DD} = 3.6 V

* This condition excludes the ZDA and ZCL pins, when driven Low, due to the presence of on-chip pull-ups.

In the following pages, Figure 36 displays the typical current consumption of the eZ80190 device versus the number of WAIT states while operating 25 °C, 3.3 V, and with either a 1 MHz or 5 MHz system clock. Figure 37 displays the typical current consumption of the eZ80190 device versus the number of WAIT states while operating 25 °C, 3.3 V, and with either a 20 MHz or 50 MHz system clock. Figure 38 displays the typical current consumption of the eZ80190 device versus the system clock frequency while operating 25 °C, 3.3 V, and using 0, 2, or 7 WAIT states. Figure 39 displays the typical current consumption of the eZ80190 device versus the system clock frequency while operating at 3.3 V, 7 WAIT states, and with either a 5 MHz, 20 MHz, or 50 MHz system clock.

Table 116. External Write Timing

		Delay (ns)	
Parameter	**Description**	**Min.**	**Max.**
T_1	Clock Rise to ADDR Valid Delay	—	10.2
T_2	Clock Rise to ADDR Hold Time	1.6	—
T_3	Clock Rise to Output DATA Valid Delay	—	10.2
T_4	DATA Hold Time from Clock Rise	5.0	—
T_5	Clock Rise to $\overline{CSx}$ Assertion Delay	3.0	10.5
T_6	Clock Rise to $\overline{CSx}$ Deassertion Delay	3.0	9.7
T_7	Clock Rise to $\overline{MREQ}$ Assertion Delay	2.8	9.6
T_8	Clock Rise to $\overline{MREQ}$ Deassertion Delay	1.6	6.9
T_9	Clock Fall to $\overline{WR}$ Assertion Delay	1.5	3.9
T_{10}	Clock Rise to $\overline{WR}$ Deassertion Delay*	1.4	4.1

* At the conclusion of a write cycle, deassertion of $\overline{WR}$ always occurs before any change to ADDR, DATA, $\overline{CSx}$, or $\overline{MREQ}$.

Table 117. External I/O Read Timing (Continued)

		Delay (ns)	
Parameter	**Description**	**Min**	**Max**
T_9	Clock Rise to $\overline{RD}$ Assertion Delay	3.0	9.8
T_{10}	Clock Rise to $\overline{RD}$ Deassertion Delay	2.5	7.1

External I/O Write Timing

Figure 43 and Table 118 display the timing for external I/O writes.

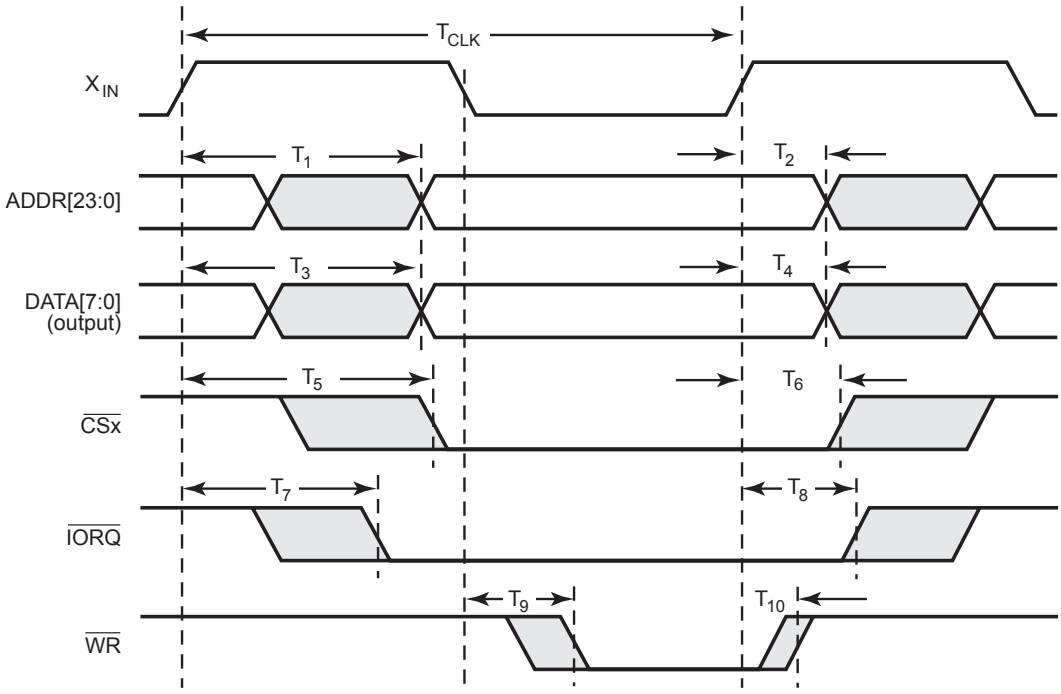

Figure 43. External I/O Write Timing

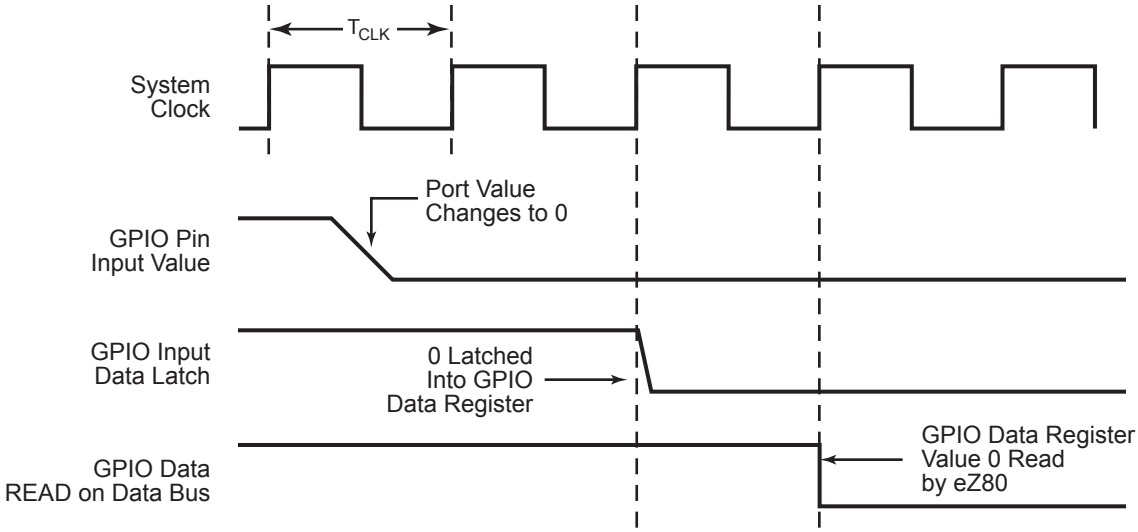

Figure 46. Port Input Sample Timing

General-Purpose I/O Port Output Timing

Figure 47 and Table 119 on page 194 display the timing of the GPIO outputs.

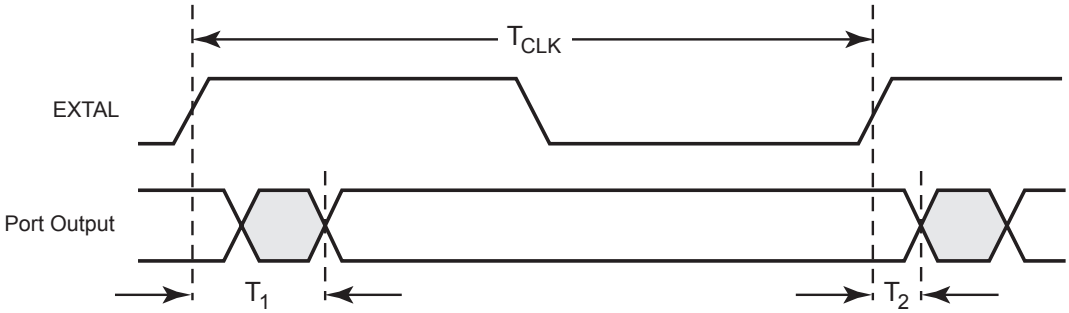

Figure 47. GPIO Port Output Timing

Ordering Information

Order eZ80190 from Zilog®, using the following part numbers. For more information regarding ordering, consult your local Zilog sales office. Zilog website www.zilog.com, lists all regional offices and provides additional eZ80190 product information.

Table 122 lists a part number, a product specification index code, and a brief description of each eZ80190 part.

Table 122. Ordering Information

Part	PSI	Description
eZ80190	eZ80190AZ050SC	100-pin LQFP, 50MHz, Standard Temperature
	eZ80190AZ050EC	100-pin LQFP, 50MHz, Extended Temperature
eZ80190 Development Kit	eZ8019000100ZCO	Complete Development Kit

The latest information regarding software and other product updates is available for download at www.zilog.com.

Part Number Description

Zilog part numbers consist of a number of components, as indicated in the following examples:

Zilog Base Products	
eZ80®	eZ80 CPU Zilog prefix
190	Product Number
AZ	Package
050	Speed
S or E	Temperature
C	Environmental Flow

Package	AZ = LQFP (also called the VQFP)
Speed	050 = 50 MHz
Standard Temperature	S = 0 °C to +70 °C
Extended Temperature	E = –40 °C to +105 °C
Environmental Flow	C = Plastic Standard

Example. Part number eZ80190AZ050SC is an eZ80® CPU product in an LQFP package, operating with a 50 MHz external clock frequency over a 0 °C to +70 °C temperature range, and built using the Plastic Standard environmental flow.