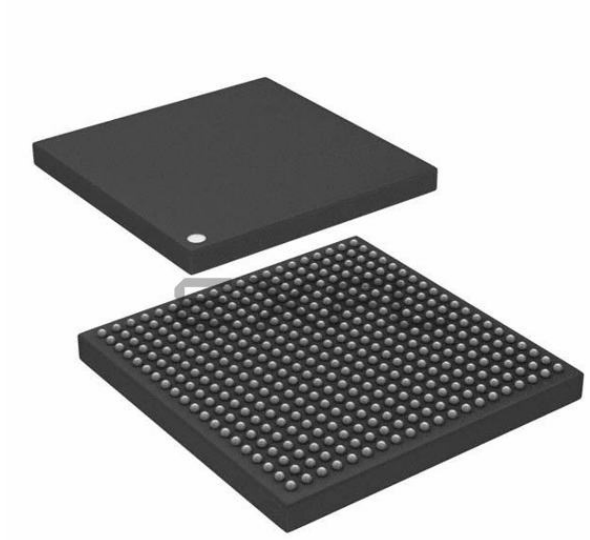

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, I²C, UART
Clock Rate	300MHz
Non-Volatile Memory	ROM (8kB)
On-Chip RAM	464kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmsc7119vf1200

Table 1. MSC7119 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
F6	V_{DDC}					
F7	GND					
F8	GND					
F9	GND					
F10	V_{DDM}					
F11	V_{DDM}					
F12	GND					
F13	GND					
F14	GND					
F15	V_{DDIO}					
F16	V_{DDC}					
F17	V_{DDC}					
F18	NC					
F19	NC					
F20	NC					
G1	GND					
G2	D13					
G3	GND					
G4	V_{DDM}					
G5	V_{DDM}					
G6	GND					
G7	GND					
G8	GND					
G9	GND					
G10	GND					
G11	GND					
G12	GND					
G13	GND					
G14	GND					
G15	V_{DDIO}					
G16	V_{DDIO}					
G17	V_{DDC}					
G18	NC					
G19	NC					
G20	NC					
H1	D14					

Table 1. MSC7119 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
H2	D12					
H3	D11					
H4	V_{DDM}					
H5	V_{DDM}					
H6	GND					
H7	GND					
H8	GND					
H9	GND					
H10	GND					
H11	GND					
H12	GND					
H13	GND					
H14	GND					
H15	V_{DDIO}					
H16	V_{DDIO}					
H17	V_{DDC}					
H18	NC					
H19	reserved				HA2	
H20	reserved				HA1	
J1	D10					
J2	V_{DDM}					
J3	D9					
J4	V_{DDM}					
J5	V_{DDM}					
J6	V_{DDM}					
J7	GND					
J8	GND					
J9	GND					
J10	GND					
J11	GND					
J12	GND					
J13	GND					
J14	GND					
J15	GND					
J16	V_{DDIO}					
J17	V_{DDC}					

Table 1. MSC7119 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
J18	GPIC11			GPOC11	HA3	
J19	reserved				$\overline{\text{HACK}}$/HACK or $\overline{\text{HRRQ}}$/HRRQ	
J20	HDSP	reserved			$\overline{\text{HREQ}}$/HREQ or $\overline{\text{HTRQ}}$/HTRQ	
K1	D0					
K2	GND					
K3	D8					
K4	V_{DDC}					
K5	V_{DDM}					
K6	GND					
K7	GND					
K8	GND					
K9	GND					
K10	GND					
K11	GND					
K12	GND					
K13	GND					
K14	GND					
K15	V_{DDIO}					
K16	V_{DDIO}					
K17	V_{DDC}					
K18	reserved				HA0	
K19	reserved				HDDS	
K20	reserved				$\overline{\text{HDS}}$/HDS or $\overline{\text{HWR}}$/HWR	
L1	D1					
L2	GND					
L3	D3					
L4	V_{DDC}					
L5	V_{DDM}					
L6	GND					
L7	GND					
L8	GND					
L9	GND					
L10	GND					
L11	GND					
L12	GND					
L13	GND					

Table 1. MSC7119 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
L14	V_{DDIO}					
L15	V_{DDIO}					
L16	V_{DDIO}					
L17	V_{DDC}					
L18	GPIB11			GPOB11	$\overline{HCS2}$/HCS2	
L19	reserved				$\overline{HCS1}$/HCS1	
L20	reserved				HRW or $\overline{HRD}$/HRD	
M1	D2					
M2	V_{DDM}					
M3	D5					
M4	V_{DDM}					
M5	V_{DDM}					
M6	GND					
M7	GND					
M8	GND					
M9	GND					
M10	GND					
M11	GND					
M12	GND					
M13	GND					
M14	GND					
M15	GND					
M16	V_{DDC}					
M17	V_{DDC}					
M18	GPIA14		$\overline{IRQ15}$	GPOA14	SDA	
M19	GPIA12		$\overline{IRQ3}$	GPOA12	UTXD	
M20	GPIA13		$\overline{IRQ2}$	GPOA13	URXD	
N1	D4					
N2	D6					
N3	V_{REF}					
N4	V_{DDM}					
N5	V_{DDM}					
N6	V_{DDM}					
N7	GND					
N8	GND					
N9	GND					

Table 1. MSC7119 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
V18	GPIA24		$\overline{\text{IRQ24}}$	GPOA24	TX_EN	
V19	reserved				CRS	
V20	TDI					
W1	GND					
W2	V_{DDM}					
W3	A12					
W4	A8					
W5	A7					
W6	A6					
W7	A3					
W8	NC					
W9	GPIA17		$\overline{\text{IRQ13}}$	GPOA17	EVNT1	CLKO
W10	BM0	GPIC14		GPOC14	EVNT2	
W11	GPIA10		$\overline{\text{IRQ5}}$	GPOA10	T0RFS	
W12	GPIA7		$\overline{\text{IRQ7}}$	GPOA7	T0TFS	
W13	GPIA3		$\overline{\text{IRQ8}}$	GPOA3	T1RD	
W14	GPIA1		$\overline{\text{IRQ10}}$	GPOA1	T1TFS	
W15	GPID4			GPOD4	TXD2	reserved
W16	GPIA27		$\overline{\text{IRQ18}}$	GPOA27	RXD3	reserved
W17	GPIA19		$\overline{\text{IRQ19}}$	GPOA19	TXD1	
W18	GPIA23		$\overline{\text{IRQ23}}$	GPOA23	TXCLK or REFCLK	
W19	GPIA26		$\overline{\text{IRQ26}}$	GPOA26	RX_ER	
W20	H8BIT	reserved			MDC	
Y1	V_{DDM}					
Y2	GND					
Y3	A9					
Y4	A1					
Y5	A0					
Y6	A4					
Y7	BA1					
Y8	reserved		$\overline{\text{NMI}}$	reserved		
Y9	BM1	GPIC15		GPOC15	EVNT3	
Y10	GPIA11		$\overline{\text{IRQ4}}$	GPOA11	T0RCK	
Y11	GPIA9			GPOA9	T0RD	
Y12	GPIA6			GPOA6	T0TD	
Y13	GPIA5		$\overline{\text{IRQ0}}$	GPOA5	T1RCK	

2.3 Thermal Characteristics

Table 4 describes thermal characteristics of the MSC7119 for the MAP-BGA package.

Table 4. Thermal Characteristics for MAP-BGA Package

Characteristic	Symbol	MAP-BGA 17 × 17 mm[5]		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	39	31	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$	23	20	°C/W
Junction-to-board[4]	$R_{\theta JB}$	12		°C/W
Junction-to-case[5]	$R_{\theta JC}$	7		°C/W
Junction-to-package-top[6]	Ψ_{JT}	2		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Section 3.1, *Thermal Design Considerations* explains these characteristics in detail.

2.4 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC7119.

Note: The leakage current is measured for nominal voltage values must vary in the same direction (for example, both V_{DDIO} and V_{DDC} vary by +2 percent or both vary by –2 percent).

Table 5. DC Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Core and PLL voltage	V_{DDC} V_{DDPLL}	1.14	1.2	1.26	V
DRAM interface I/O voltage[1]	V_{DDM}	2.375	2.5	2.625	V
I/O voltage	V_{DDIO}	3.135	3.3	3.465	V
DRAM interface I/O reference voltage[2]	V_{REF}	$0.49 \times V_{DDM}$	1.25	$0.51 \times V_{DDM}$	V
DRAM interface I/O termination voltage[3]	VTT	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
Input high CLKIN voltage	V_{IHCLK}	2.4	3.0	3.465	V
DRAM interface input high I/O voltage	V_{IHM}	$V_{REF} + 0.28$	V_{DDM}	$V_{DDM} + 0.3$	V
DRAM interface input low I/O voltage	V_{ILM}	–0.3	GND	$V_{REF} - 0.18$	V
Input leakage current, $V_{IN} = V_{DDIO}$	I_{IN}	–1.0	0.09	1	µA
V_{REF} input leakage current	I_{VREF}	—	—	5	µA

2.5.3.2 Reset Configuration

The MSC7119 has two mechanisms for writing the reset configuration:

- From a host through the host interface (HDI16)
- From memory through the I^2C interface

Five signal levels (see **Chapter 1** for signal description details) are sampled on $\overline{\text{PORESET}}$ deassertion to define the boot and operating conditions:

- BM[0–1]
- SWTE
- H8BIT
- HDSP

2.5.3.3 Reset Timing Tables

Table 16 and **Figure 4** describe the reset timing for a reset configuration write.

Table 16. Timing for a Reset Configuration Write

No.	Characteristics	Expression	Unit
1	Required external $\overline{\text{PORESET}}$ duration minimum	$16/F_{CLKIN}$	clocks
2	Delay from $\overline{\text{PORESET}}$ deassertion to $\overline{\text{HRESET}}$ deassertion	$521/F_{CLKIN}$	clocks
Note:	Timings are not tested, but are guaranteed by design.		

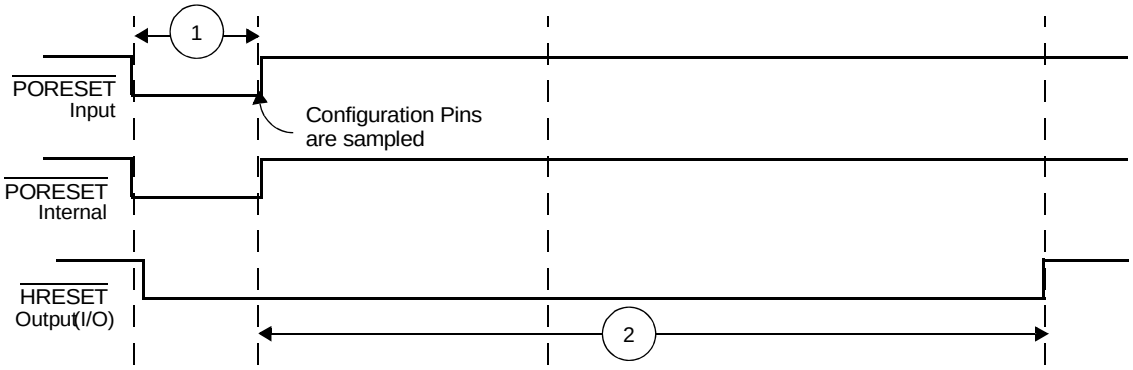

Figure 4. Timing Diagram for a Reset Configuration Write

2.5.6.4 Management Interface Timing

Table 24. Ethernet Controller Management Interface Timing

No.	Characteristics	Min	Max	Unit
808	MDC period	400	—	ns
809	MDC pulse width high	160	—	ns
810	MDC pulse width low	160	—	ns
811	MDS falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
812	MDS falling edge to MDIO output valid (maximum propagation delay)	—	15	ns
813	MDIO input to MDC rising edge setup time	10	—	ns
814	MDC rising edge to MDIO input hold time	10	—	ns

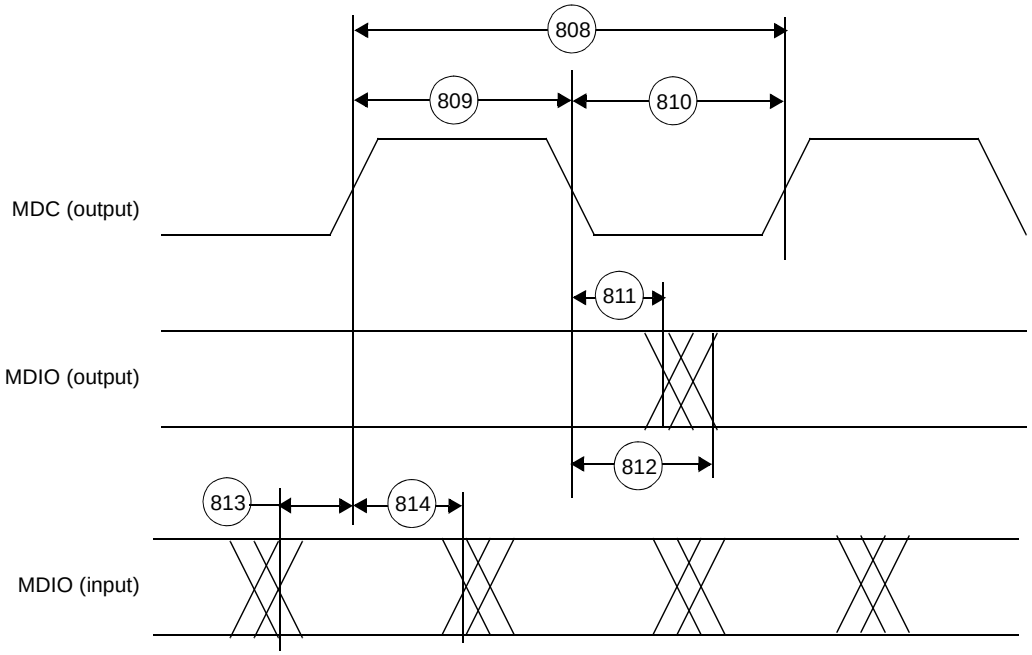

Figure 13. Serial Management Channel Timing

2.5.7 HDI16 Signals

Table 25. Host Interface (HDI16) Timing[1, 2]

No.	Characteristics[3]	Expression	Value	Unit
40	Host Interface Clock period	T_{CORE}	Note 1	ns
44a	Read data strobe minimum assertion width[4] HACK read minimum assertion width	$2.0 \times T_{CORE} + 9.0$	Note 11	ns
44b	Read data strobe minimum deassertion width[4] HACK read minimum deassertion width	$1.5 \times T_{CORE}$	Note 11	ns
44c	Read data strobe minimum deassertion width[4] after “Last Data Register” reads[5,6], or between two consecutive CVR, ICR, or ISR reads[7] HACK minimum deassertion width after “Last Data Register” reads[5,6]	$2.5 \times T_{CORE}$	Note 11	ns
45	Write data strobe minimum assertion width[8] HACK write minimum assertion width	$1.5 \times T_{CORE}$	Note 11	ns
46	Write data strobe minimum deassertion width[8] HACK write minimum deassertion width after ICR, CVR and Data Register writes[5]	$2.5 \times T_{CORE}$	Note 11	ns
47	Host data input minimum setup time before write data strobe deassertion[8] Host data input minimum setup time before HACK write deassertion	—	2.5	ns
48	Host data input minimum hold time after write data strobe deassertion[8] Host data input minimum hold time after HACK write deassertion	—	2.5	ns
49	Read data strobe minimum assertion to output data active from high impedance[4] HACK read minimum assertion to output data active from high impedance	—	1.0	ns
50	Read data strobe maximum assertion to output data valid[4] HACK read maximum assertion to output data valid	$(2.0 \times T_{CORE}) + 8.0$	Note 11	ns
51	Read data strobe maximum deassertion to output data high impedance[4] HACK read maximum deassertion to output data high impedance	—	9.0	ns
52	Output data minimum hold time after read data strobe deassertion[4] Output data minimum hold time after HACK read deassertion	—	1.0	ns
53	HCS[1–2] minimum assertion to read data strobe assertion[4]	—	0.5	ns
54	HCS[1–2] minimum assertion to write data strobe assertion[8]	—	0.0	ns
55	HCS[1–2] maximum assertion to output data valid	$(2.0 \times T_{CORE}) + 6.0$	Note 11	ns
56	HCS[1–2] minimum hold time after data strobe deassertion[9]	—	0.5	ns
57	HA[0–2], HRW minimum setup time before data strobe assertion[9]	—	5.0	ns
58	HA[0–2], HRW minimum hold time after data strobe deassertion[9]	—	5.0	ns
61	Maximum delay from read data strobe deassertion to host request deassertion for “Last Data Register” read[4, 5, 10]	$(3.0 \times T_{CORE}) + 6.0$	Note 11	ns
62	Maximum delay from write data strobe deassertion to host request deassertion for “Last Data Register” write[5,8,10]	$(3.0 \times T_{CORE}) + 6.0$	Note 11	ns
63	Minimum delay from DMA HACK (OAD=0) or Read/Write data strobe(OAD=1) deassertion to HREQ assertion.	$(2.0 \times T_{CORE}) + 1.0$	Note 11	ns
64	Maximum delay from DMA HACK (OAD=0) or Read/Write data strobe(OAD=1) assertion to HREQ deassertion	$(5.0 \times T_{CORE}) + 6.0$	Note 11	ns

Notes:
1. T_{CORE} = core clock period. At 300 MHz, T_{CORE} = 3.333 ns.
2. In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.
3. V_{DD} = 3.3 V ± 0.15 V; T_J = –40°C to +105 °C, C_L = 30 pF for maximum delay timings and C_L = 0 pF for minimum delay timings.
4. The read data strobe is HRD/HRD in the dual data strobe mode and HDS/HDS in the single data strobe mode.
5. For 64-bit transfers, the “last data register” is the register at address 0x7, which is the last location to be read or written in data transfers. This is RX0/TX0 in the little endian mode (HBE = 0), or RX3/TX3 in the big endian mode (HBE = 1).
6. This timing is applicable only if a read from the “last data register” is followed by a read from the RX[0–3] registers without first polling RXDF or HREQ bits, or waiting for the assertion of the HREQ/HREQ signal.
7. This timing is applicable only if two consecutive reads from one of these registers are executed.
8. The write data strobe is HWR in the dual data strobe mode and HDS in the single data strobe mode.
9. The data strobe is host read (HRD/HRD) or host write (HWR/HWR) in the dual data strobe mode and host data strobe (HDS/HDS) in the single data strobe mode.
10. The host request is HREQ/HREQ in the single host request mode and HRRQ/HRRQ and HTRQ/HTRQ in the double host request mode. HRRQ/HRRQ is deasserted only when HOTX fifo is empty, HTRQ/HTRQ is deasserted only if HORX fifo is full
11. Compute the value using the expression.
12. The read and write data strobe minimum deassertion width for non-”last data register” accesses in single and dual data strobe modes is based on timings 57 and 58.

Figure 14 and **Figure 15** show HDI16 read signal timing. **Figure 16** and **Figure 17** show HDI16 write signal timing.

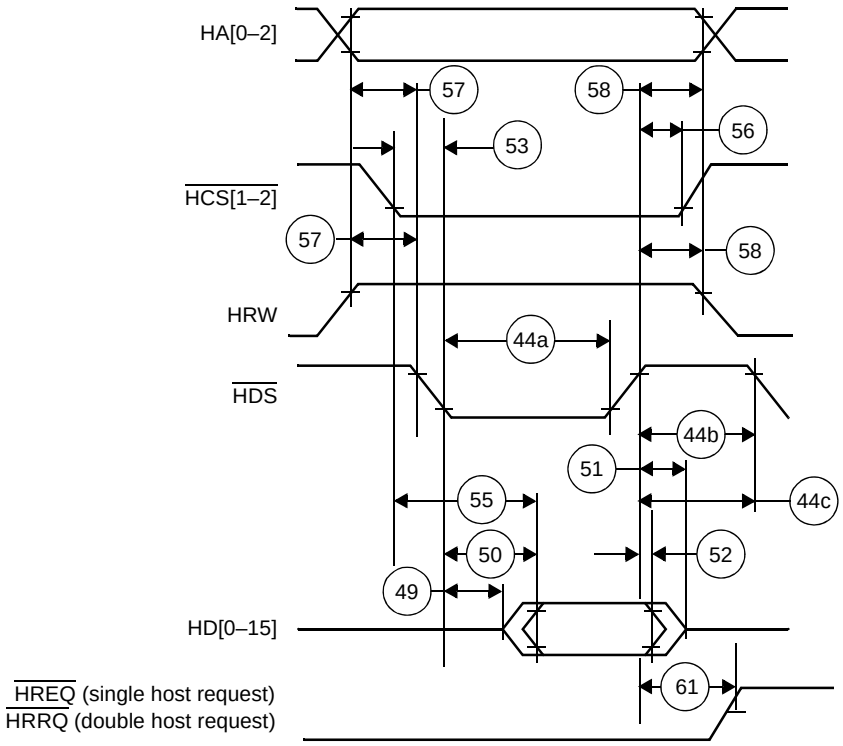

Figure 14. Read Timing Diagram, Single Data Strobe

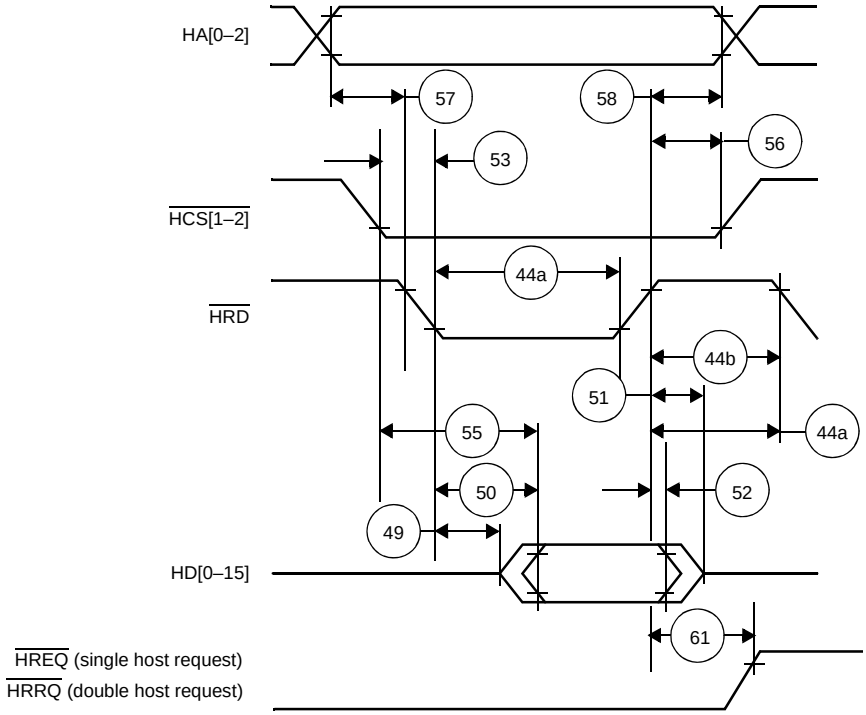

Figure 15. Read Timing Diagram, Double Data Strobe

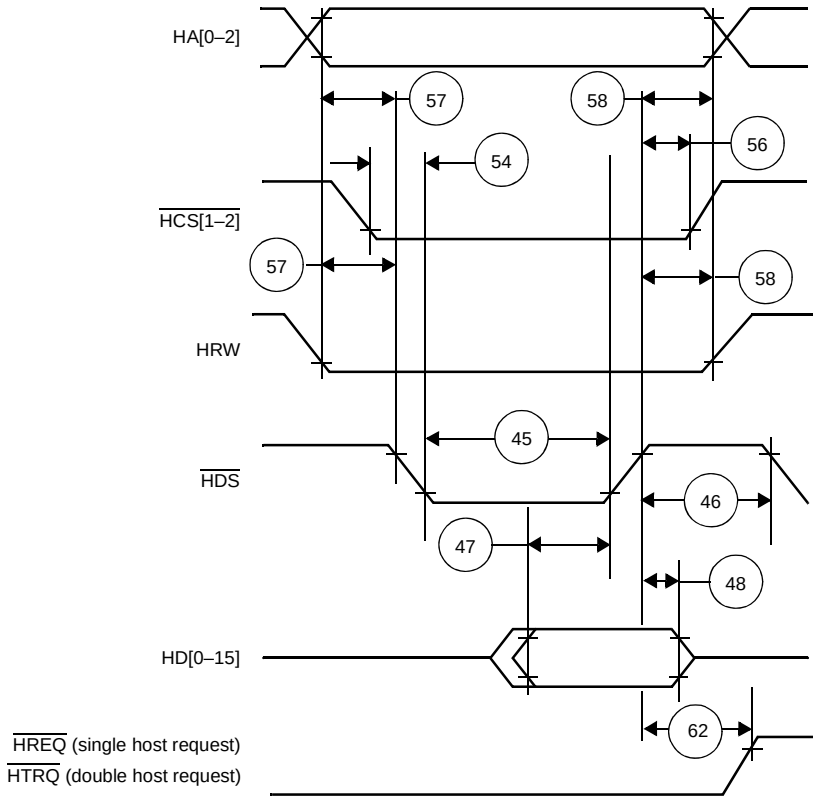

Figure 16. Write Timing Diagram, Single Data Strobe

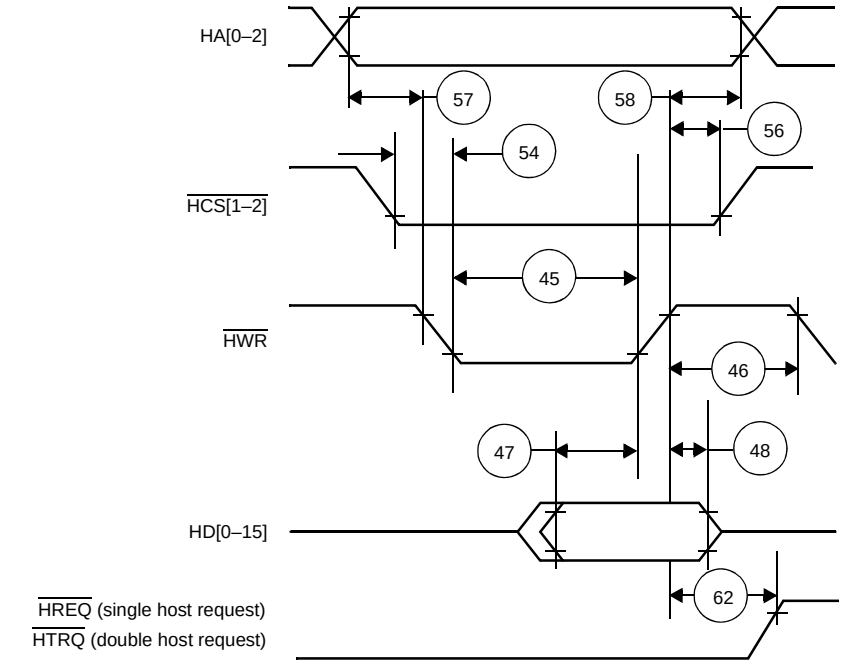

Figure 17. Write Timing Diagram, Double Data Strobe

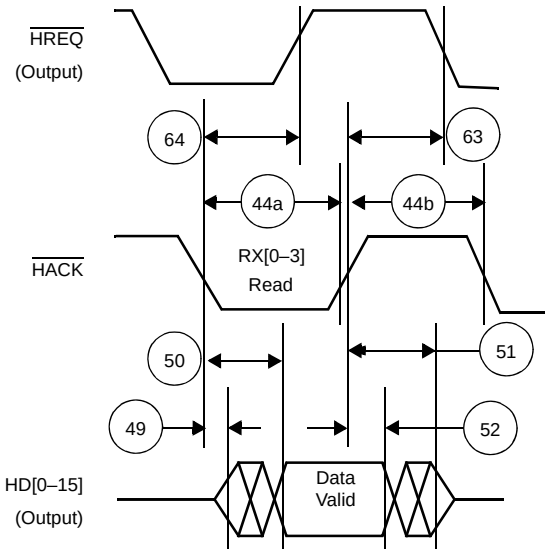

Figure 18. Host DMA Read Timing Diagram, HPCR[OAD] = 0

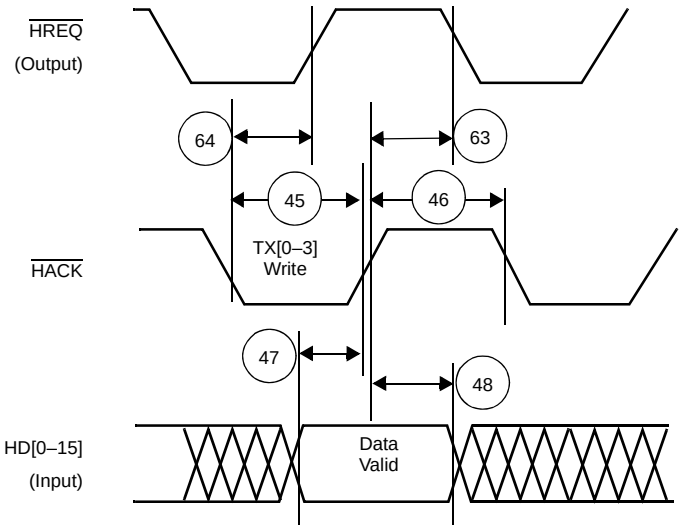

Figure 19. Host DMA Write Timing Diagram, HPCR[OAD] = 0

2.5.8 I²C Timing

Table 26. I²C Timing

No.	Characteristic	Fast		Unit
		Min	Max	
450	SCL clock frequency	0	400	kHz
451	Hold time START condition	(SCL clock period/2) – 0.3	—	µs
452	SCL low period	(SCL clock period/2) – 0.3	—	µs
453	SCL high period	(SCL clock period/2) – 0.1	—	µs
454	Repeated START set-up time (not shown in figure)	$2 \times 1/F_{BCK}$	—	µs
455	Data hold time	0	—	µs
456	Data set-up time	250	—	ns
457	SDA and SCL rise time	—	700	ns
458	SDA and SCL fall time	—	300	ns
459	Set-up time for STOP	(SCL clock period/2) – 0.7	—	µs
460	Bus free time between STOP and START	(SCL clock period/2) – 0.3	—	µs
Note:	SDA set-up time is referenced to the rising edge of SCL. SDA hold time is referenced to the falling edge of SCL. Load capacitance on SDA and SCL is 400 pF.			

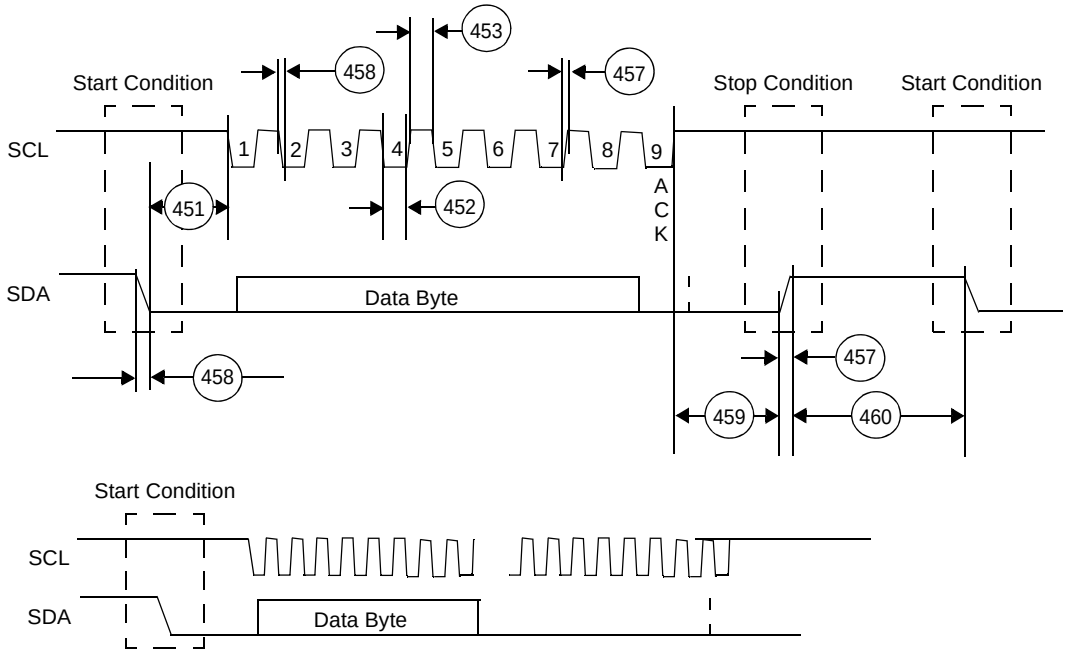

Figure 20. I²C Timing Diagram

2.5.9 UART Timing

Table 27. UART Timing

No.	Characteristics	Expression	Min	Max	Unit
—	Internal bus clock (APBCLK)	$F_{CORE}/2$	—	150	MHz
—	Internal bus clock period (1/APBCLK)	T_{APBCLK}	6.67	—	ns
400	URXD and UTXD inputs high/low duration	$16 \times T_{APBCLK}$	106.67	—	ns
401	URXD and UTXD inputs rise/fall time		—	5	ns
402	UTXD output rise/fall time		—	5	ns

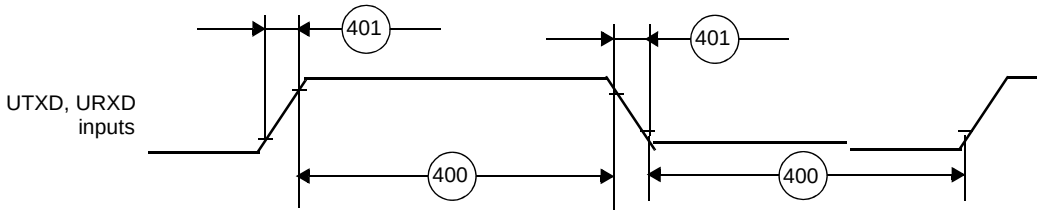

Figure 21. UART Input Timing

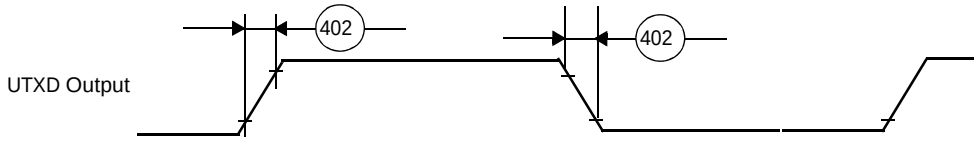

Figure 22. UART Output Timing

2.5.10 EE Timing

Table 28. EE0 Timing

Number	Characteristics	Type	Min
65	EE0 input to the core	Asynchronous	4 core clock periods
66	EE0 output from the core	Synchronous to core clock	1 core clock period

Notes:
1. The core clock is the SC1400 core clock. The ratio between the core clock and CLKOUT is configured during power-on-reset.
2. Configure the direction of the EE pin in the EE_CTRL register (see the *SC140/SC1400 Core Reference Manual* for details.
3. Refer to **Table 1-11** on page 1-16 for details on EE pin functionality.

Figure 24 shows the signal behavior of the EE pin.

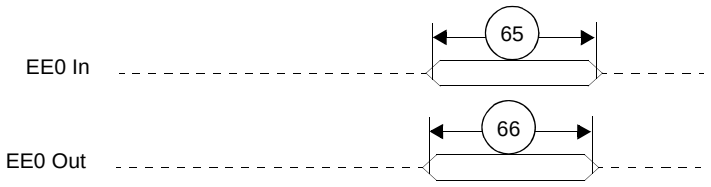

Figure 23. EE Pin Timing

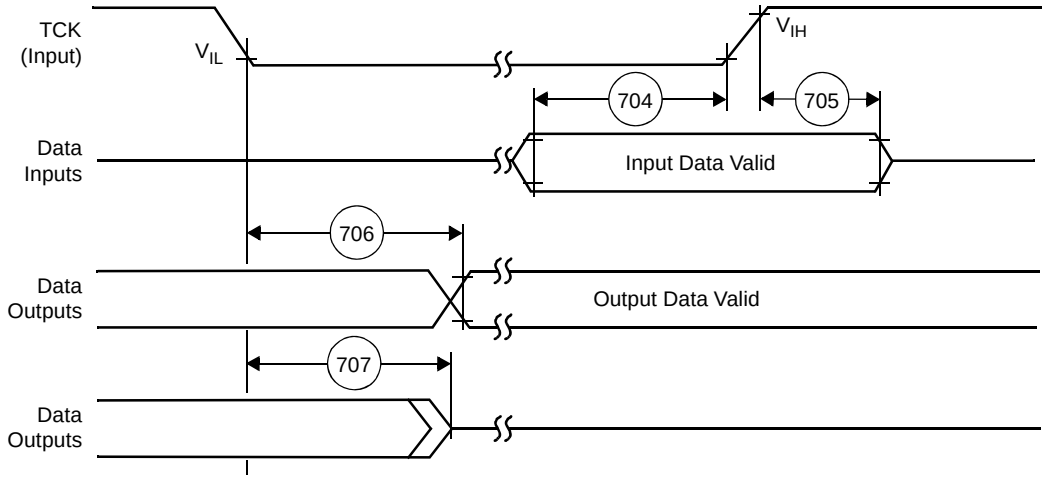

Figure 27. Boundary Scan (JTAG) Timing Diagram

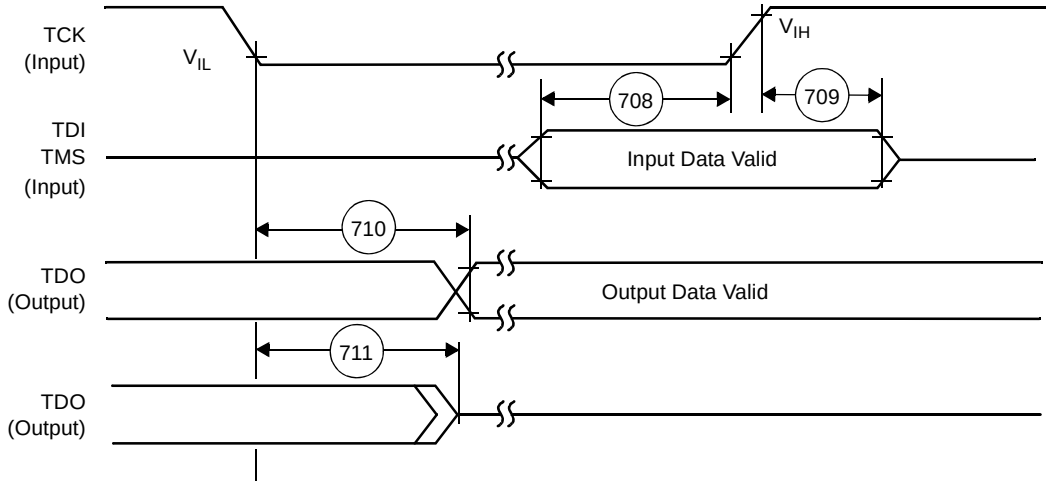

Figure 28. Test Access Port Timing Diagram

Figure 29. $\overline{\text{TRST}}$ Timing Diagram

3.2 Power Supply Design Considerations

This section outlines the MSC7119 power considerations: power supply, power sequencing, power planes, decoupling, power supply filtering, and power consumption. It also presents a recommended power supply design and options for low-power consumption. For information on AC/DC electrical specifications and thermal characteristics, refer to **Section 2**.

3.2.1 Power Supply

The MSC7119 requires four input voltages, as shown in **Table 32**.

Table 32. MSC7119 Voltages

Voltage	Symbol	Value
Core	V_{DDC}	1.2 V
Memory	V_{DDM}	2.5 V
Reference	V_{REF}	1.25 V
I/O	V_{DDIO}	3.3 V

You should supply the MSC7119 core voltage via a variable switching supply or regulator to allow for compatibility with possible core voltage changes on future silicon revisions. The core voltage is supplied with 1.2 V (+5% and –10%) across V_{DDC} and GND and the I/O section is supplied with 3.3 V (± 10%) across V_{DDIO} and GND. The memory and reference voltages supply the DDR memory controller block. The memory voltage is supplied with 2.5 V across V_{DDM} and GND. The reference voltage is supplied across V_{REF} and GND and must be between $0.49 \times V_{DDM}$ and $0.51 \times V_{DDM}$. Refer to the JEDEC standard JESD8 (*Stub Series Terminated Logic for 2.5 Volts* (STTL_2)) for memory voltage supply requirements.

3.2.2 Power Sequencing

One consequence of multiple power supplies is that the voltage rails ramp up at different rates when power is initially applied. The rates depend on the power supply, the type of load on each power supply, and the way different voltages are derived. It is extremely important to observe the power up and power down sequences at the board level to avoid latch-up, forward biasing of ESD devices, and excessive currents, which all lead to severe device damage.

Note: There are five possible power-up/power-down sequence cases. The first four cases listed in the following sections are recommended for new designs. The fifth case is not recommended for new designs and must be carefully evaluated for current spike risks based on actual information for the specific application.

3.2.2.1 Case 1

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDC} (1.2 V) supply second.
3. Turn on the V_{DDM} (2.5 V) supply third.
4. Turn on the V_{REF} (1.25 V) supply fourth (last).

The power-down sequence is as follows:

1. Turn off the V_{REF} (1.25 V) supply first.
2. Turn off the V_{DDM} (2.5 V) supply second.
3. Turn off the V_{DDC} (1.2 V) supply third.
4. Turn of the V_{DDIO} (3.3 V) supply fourth (last).

Use the following guidelines:

- Make sure that the time interval between the ramp-down of V_{DDIO} and V_{DDC} is less than 10 ms.
- Make sure that the time interval between the ramp-up or ramp-down for V_{DDC} and V_{DDM} is less than 10 ms for power-up and power-down.
- Refer to **Figure 30** for relative timing for power sequencing case 1.

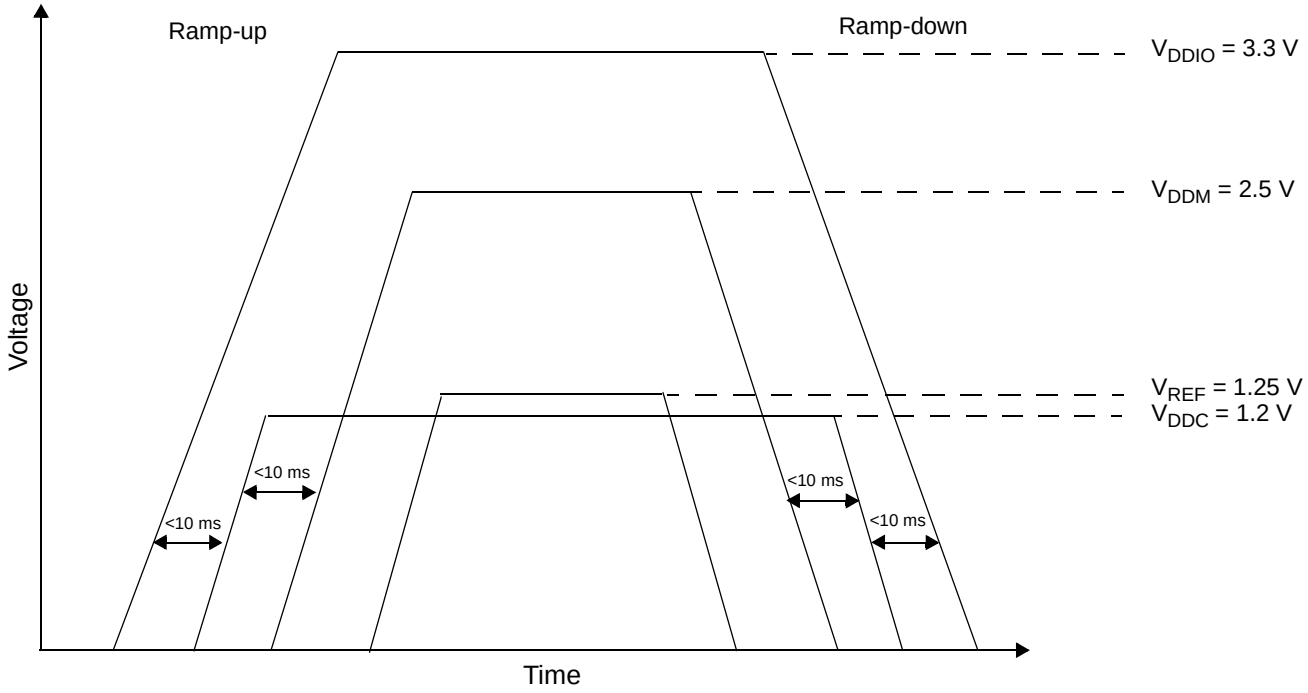

Figure 30. Voltage Sequencing Case 1

3.2.2.3 Case 3

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDC} (1.2 V) supply second.
3. Turn on the V_{DDM} (2.5 V) and V_{REF} (1.25 V) supplies simultaneously (third).

Note: Make sure that the time interval between the ramp-up of V_{DDIO} and V_{DDC} is less than 10 ms.

The power-down sequence is as follows:

1. Turn off the V_{DDM} (2.5 V) and V_{REF} (1.25 V) supplies simultaneously (first).
2. Turn off the V_{DDC} (1.2 V) supply second.
3. Turn of the V_{DDIO} (3.3 V) supply third (last).

Use the following guidelines:

- Make sure that the time interval between the ramp-down for V_{DDIO} and V_{DDC} is less than 10 ms.
- Make sure that the time interval between the ramp-up or ramp-down time for V_{DDC} and V_{DDM} is less than 10 ms for power-up and power-down.
- Refer to **Figure 32** for relative timing for Case 3.

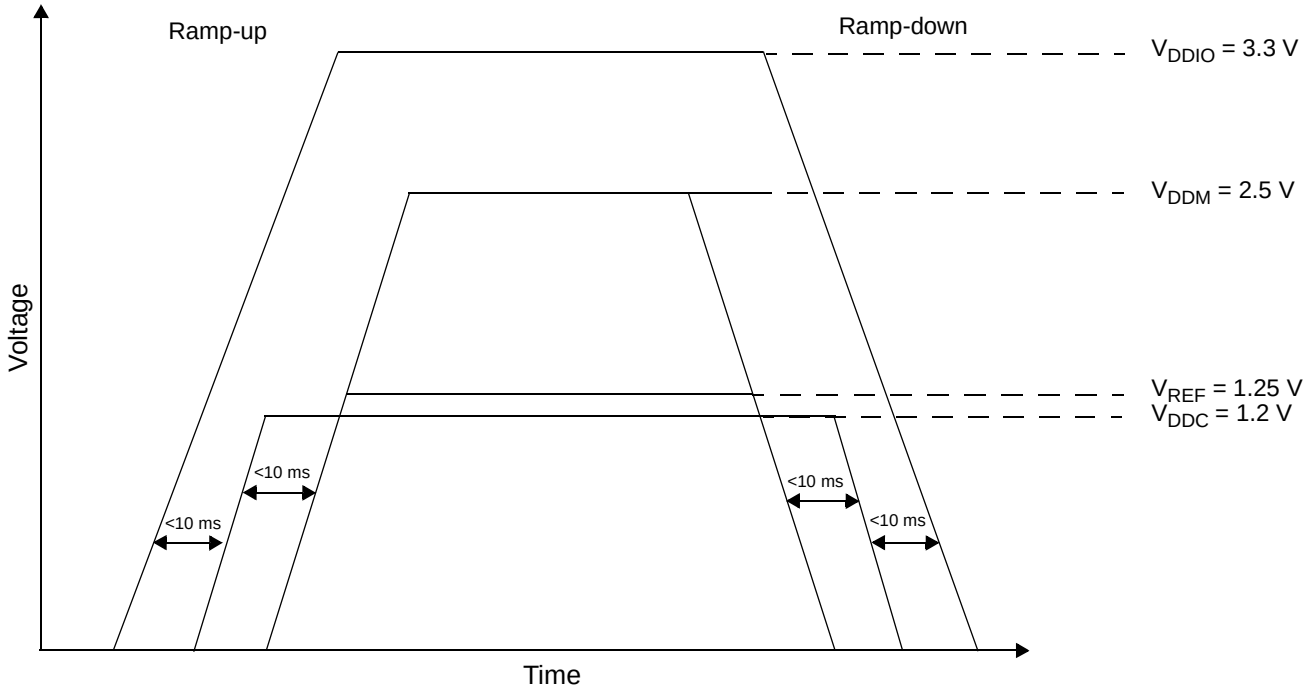

Figure 32. Voltage Sequencing Case 3

3.2.2.4 Case 4

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDC} (1.2 V), V_{DDM} (2.5 V), and V_{REF} (1.25 V) supplies simultaneously (second).

Note: Make sure that the time interval between the ramp-up of V_{DDIO} and V_{DDC} is less than 10 ms.

The power-down sequence is as follows:

1. Turn off the V_{DDC} (1.2 V), V_{REF} (1.25 V), and V_{DDM} (2.5 V) supplies simultaneously (first).
2. Turn of the V_{DDIO} (3.3 V) supply last.

Use the following guidelines:

- Make sure that the time interval between the ramp-up or ramp-down time for V_{DDC} and V_{DDM} is less than 10 ms for power-up and power-down.
- Refer to **Figure 33** for relative timing for Case 4.

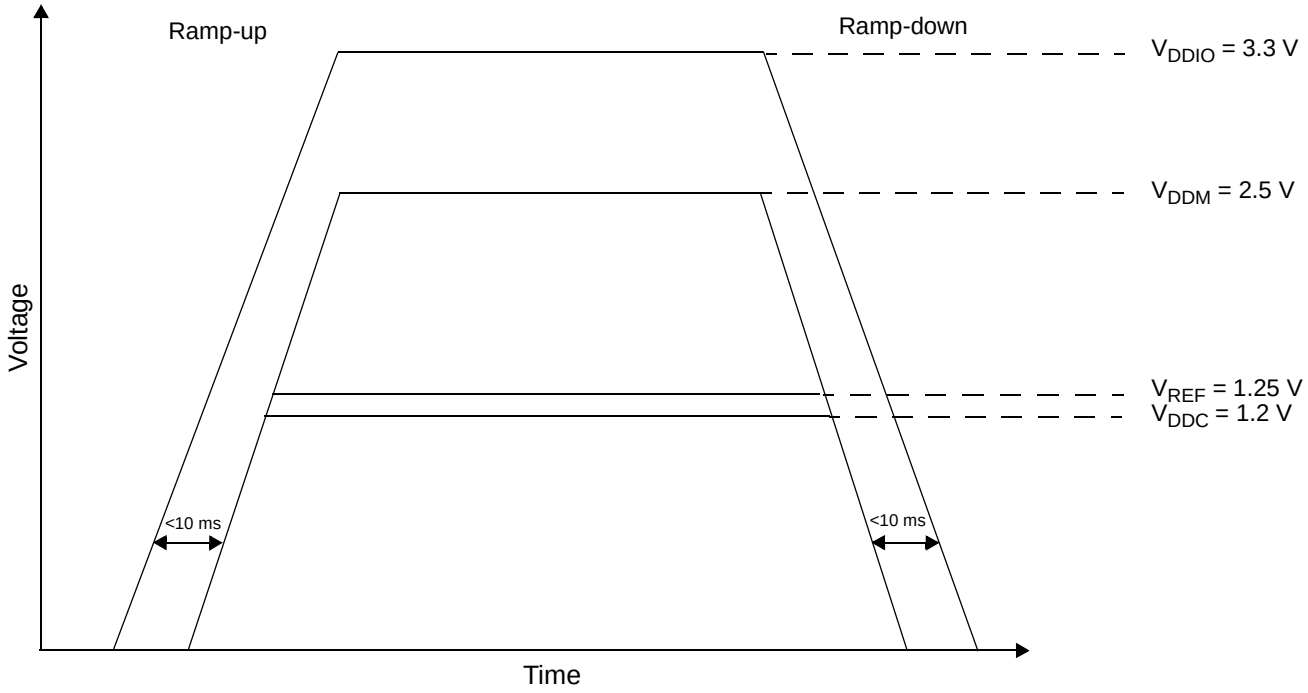

Figure 33. Voltage Sequencing Case 4

3.3.6 Example Total Power Consumption

Using the examples in this section and assuming four peripherals and 10 I/O lines active, a total power consumption value is estimated as the following:

$$P_{TOTAL} = 324.0 + (4 \times 4.32) + 326.3 + (10 \times 5.44) + 64 = 784.98\ mW \qquad \textit{Eqn. 13}$$

3.4 Reset and Boot

This section describes the recommendations for configuring the MSC7119 at reset and boot.

3.4.1 Reset Circuit

$\overline{\text{HRESET}}$ is a bidirectional signal and, if driven as an input, should be driven with an open collector or open-drain device. For an open-drain output such as $\overline{\text{HRESET}}$, take care when driving many buffers that implement input bus-hold circuitry. The bus-hold currents can cause enough voltage drop across the pull-up resistor to change the logic level to low. Either a smaller value of pull-up or less current loading from the bus-hold drivers overcomes this issue. To avoid exceeding the MSC7119 output current, the pull-up value should not be too small (a 1 KΩ pull-up resistor is used in the MSC711xADS reference design).

3.4.2 Reset Configuration Pins

Table 34 shows the MSC7119 reset configuration signals. These signals are sampled at the deassertion (rising edge) of $\overline{\text{PORESET}}$. For details, refer to the Reset chapter of the *MSC711x Reference Manual*.

Table 34. Reset Configuration Signals

Signal	Description	Settings
BM[3–0]	Determines boot mode.	See **Table 35** for details.
SWTE	Determines watchdog functionality.	0 Watchdog timer disabled. 1 Watchdog timer enabled.
HDSP	Configures HDI16 strobe polarity.	0 Host Data strobes active low. 1 Host Data strobes active high.
H8BIT	Configures HDI16 operation mode.	0 HDI16 port configured for 16-bit operation. 1 HDI16 port configured for 8-bit operation.