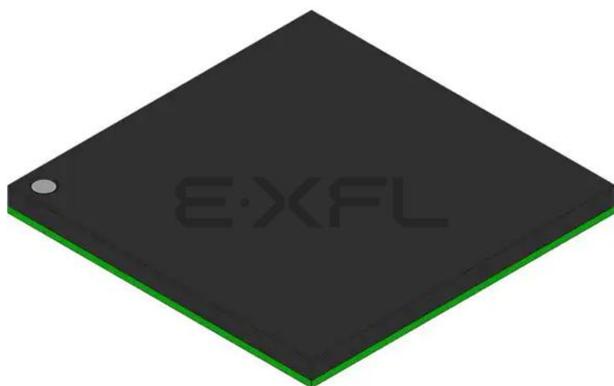

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, I²C, UART
Clock Rate	300MHz
Non-Volatile Memory	ROM (8kB)
On-Chip RAM	464kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	400-LFBGA
Supplier Device Package	400-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=msc7119vf1200

Bottom View

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	NC	NC	NC	NC	BM3	GND	HD0	HD1	HD4	HD6	HD7	HD10	HD12	HD15	$\overline{CK}$	CK	DQS2	DQM1	GND	GND
B	NC	NC	NC	NC	NC	BM2	NC	HD2	HD5	HD8	HD11	HD14	$\overline{WE}$	CKE	DQS0	DQS3	DQM2	$\overline{CS0}$	NC	V_{DDM}
C	NC	NC	NC	NC	NC	NC	NC	NC	HD3	HD9	HD13	$\overline{CAS}$	$\overline{RAS}$	DQS1	DQM0	DQM3	$\overline{CS1}$	D25	D30	D24
D	NC	NC	NC	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	GND	D27	D28	V_{DDM}
E	NC	NC	NC	V_{DD}	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDM}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DDM}	V_{DDM}	D31	D26	GND
F	NC	NC	NC	V_{DD}	V_{DD}	V_{DDIO}	GND	GND	GND	V_{DDM}	V_{DDM}	GND	GND	GND	V_{DD}	V_{DD}	V_{DD}	D29	D15	V_{DDM}
G	NC	NC	NC	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	GND	D13	GND
H	HA1	HA2	NC	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	D11	D12	D14
J	$\overline{HREQ}$	$\overline{HACK}$	HA3	V_{DD}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	V_{DDM}	D9	V_{DDM}	D10
K	$\overline{HDS}$	HDDS	HA0	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DD}	D8	GND	D0
L	HRW	$\overline{HCS1}$	$\overline{HCS2}$	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DD}	D3	GND	D1
M	URXD	UTXD	SDA	V_{DD}	V_{DD}	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	D5	V_{DDM}	D2
N	V_{SSPLL}	SCL	CLKIN	V_{DD}	V_{DD}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	V_{DDM}	V_{REF}	D6	D4
P	V_{DDPLL}	TPSEL	$\overline{PORESET}$	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	V_{DDM}	D16	D17	D7
R	TEST0	EE0	TDO	V_{DD}	V_{DDIO}	V_{DDIO}	GND	V_{DDIO}	GND	GND	V_{DDM}	GND	V_{DDM}	GND	V_{DDM}	V_{DDM}	V_{DDM}	D18	D19	GND
T	$\overline{HRESET}$	TMS	MDIO	V_{DD}	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDM}	V_{DDM}	V_{DD}	V_{DDM}	V_{DDM}	V_{DD}	V_{DDM}	V_{DDM}	D22	D20	V_{DDM}
U	$\overline{TRST}$	TCK	COL	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DDM}	D23	D21	GND
V	TDI	CRS	TX_EN	RXD0	RXD2	TX_ER	T1TD	T1RFS	T0TCK	EVNT4	EVNT0	NC	BA0	A2	A5	A10	A11	A13	NC	V_{DDM}
W	MDC	RX_ER	TXCLK	TXD1	RXD3	TXD2	T1TFS	T1RD	T0TFS	T0RFS	EVNT2	EVNT1	NC	A3	A6	A7	A8	A12	V_{DDM}	GND
Y	RX_DV	GND	RXD1	TXD0	RXCLK	TXD3	T1TCK	T1RCK	TOTD	T0RD	T0RCK	EVNT3	$\overline{NMI}$	BA1	A4	A0	A1	A9	GND	V_{DDM}

Figure 3. MSC7119 Molded Array Process-Ball Grid Array (MAP-BGA), Bottom View

Table 1. MSC7119 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
D10	V_{DDM}					
D11	V_{DDIO}					
D12	V_{DDIO}					
D13	V_{DDIO}					
D14	V_{DDIO}					
D15	V_{DDIO}					
D16	V_{DDIO}					
D17	V_{DDC}					
D18	NC					
D19	NC					
D20	NC					
E1	GND					
E2	D26					
E3	D31					
E4	V_{DDM}					
E5	V_{DDM}					
E6	V_{DDC}					
E7	V_{DDC}					
E8	V_{DDC}					
E9	V_{DDC}					
E10	V_{DDM}					
E11	V_{DDIO}					
E12	V_{DDIO}					
E13	V_{DDIO}					
E14	V_{DDIO}					
E15	V_{DDIO}					
E16	V_{DDC}					
E17	V_{DDC}					
E18	NC					
E19	NC					
E20	NC					
F1	V_{DDM}					
F2	D15					
F3	D29					
F4	V_{DDC}					
F5	V_{DDC}					

Table 1. MSC7119 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
H2	D12					
H3	D11					
H4	V_{DDM}					
H5	V_{DDM}					
H6	GND					
H7	GND					
H8	GND					
H9	GND					
H10	GND					
H11	GND					
H12	GND					
H13	GND					
H14	GND					
H15	V_{DDIO}					
H16	V_{DDIO}					
H17	V_{DDC}					
H18	NC					
H19	reserved				HA2	
H20	reserved				HA1	
J1	D10					
J2	V_{DDM}					
J3	D9					
J4	V_{DDM}					
J5	V_{DDM}					
J6	V_{DDM}					
J7	GND					
J8	GND					
J9	GND					
J10	GND					
J11	GND					
J12	GND					
J13	GND					
J14	GND					
J15	GND					
J16	V_{DDIO}					
J17	V_{DDC}					

Table 1. MSC7119 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
U2	D21					
U3	D23					
U4	V_{DDM}					
U5	V_{DDC}					
U6	V_{DDC}					
U7	V_{DDC}					
U8	V_{DDC}					
U9	V_{DDC}					
U10	V_{DDC}					
U11	V_{DDC}					
U12	V_{DDC}					
U13	V_{DDC}					
U14	V_{DDC}					
U15	V_{DDC}					
U16	V_{DDC}					
U17	V_{DDC}					
U18	reserved				COL	
U19	TCK					
U20	$\overline{TRST}$					
V1	V_{DDM}					
V2	NC					
V3	A13					
V4	A11					
V5	A10					
V6	A5					
V7	A2					
V8	BA0					
V9	NC					
V10	reserved				EVNT0	
V11	SWTE	GPIA16	$\overline{IRQ12}$	GPOA16	EVNT4	
V12	GPIA8		$\overline{IRQ6}$	GPOA8	T0TCK	
V13	GPIA4		$\overline{IRQ1}$	GPOA4	T1RFS	
V14	GPIA0		$\overline{IRQ11}$	GPOA0	T1TD	
V15	GPIA28		$\overline{IRQ17}$	GPOA28	TX_ER	reserved
V16	GPID6			GPOD6	RXD2	reserved
V17	GPIA22		$\overline{IRQ22}$	GPOA22	RXD0	

Table 1. MSC7119 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
Y14	GPIA2		$\overline{\text{IRQ9}}$	GPOA2	T1TCK	
Y15	GPIA29		$\overline{\text{IRQ16}}$	GPOA29	TXD3	reserved
Y16	GPID5			GPOD5	RXCLK	reserved
Y17	GPIA20		$\overline{\text{IRQ20}}$	GPOA20	TXD0	
Y18	GPIA21		$\overline{\text{IRQ21}}$	GPOA21	RXD1	
Y19	GND					
Y20	GPIA25		$\overline{\text{IRQ25}}$	GPOA25	RX_DV or CRS_DV	

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC711x Reference Manual*.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

2.3 Thermal Characteristics

Table 4 describes thermal characteristics of the MSC7119 for the MAP-BGA package.

Table 4. Thermal Characteristics for MAP-BGA Package

Characteristic	Symbol	MAP-BGA 17 × 17 mm[5]		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	39	31	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$	23	20	°C/W
Junction-to-board[4]	$R_{\theta JB}$	12		°C/W
Junction-to-case[5]	$R_{\theta JC}$	7		°C/W
Junction-to-package-top[6]	Ψ_{JT}	2		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Section 3.1, *Thermal Design Considerations* explains these characteristics in detail.

2.4 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC7119.

Note: The leakage current is measured for nominal voltage values must vary in the same direction (for example, both V_{DDIO} and V_{DDC} vary by +2 percent or both vary by –2 percent).

Table 5. DC Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Core and PLL voltage	V_{DDC} V_{DDPLL}	1.14	1.2	1.26	V
DRAM interface I/O voltage[1]	V_{DDM}	2.375	2.5	2.625	V
I/O voltage	V_{DDIO}	3.135	3.3	3.465	V
DRAM interface I/O reference voltage[2]	V_{REF}	$0.49 \times V_{DDM}$	1.25	$0.51 \times V_{DDM}$	V
DRAM interface I/O termination voltage[3]	VTT	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
Input high CLKIN voltage	V_{IHCLK}	2.4	3.0	3.465	V
DRAM interface input high I/O voltage	V_{IHM}	$V_{REF} + 0.28$	V_{DDM}	$V_{DDM} + 0.3$	V
DRAM interface input low I/O voltage	V_{ILM}	–0.3	GND	$V_{REF} - 0.18$	V
Input leakage current, $V_{IN} = V_{DDIO}$	I_{IN}	–1.0	0.09	1	µA
V_{REF} input leakage current	I_{VREF}	—	—	5	µA

Table 5. DC Electrical Characteristics (continued)

Characteristic	Symbol	Min	Typical	Max	Unit
Tri-state (high impedance off state) leakage current, $V_{IN} = V_{DDIO}$	I_{OZ}	–1.0	0.09	1	μA
Signal low input current, V_{IL} = 0.4 V	I_L	–1.0	0.09	1	μA
Signal high input current, V_{IH} = 2.0 V	I_H	–1.0	0.09	1	μA
Output high voltage, I_{OH} = –2 mA, except open drain pins	V_{OH}	2.0	3.0	—	V
Output low voltage, I_{OL}= 5 mA	V_{OL}	—	0	0.4	V
Typical power at 300 MHz[5]	P	—	324.0	—	mW

Notes:
1. The value of V_{DDM} at the MSC7119 device must remain within 50 mV of V_{DDM} at the DRAM device at all times.
2. V_{REF} must be equal to 50% of V_{DDM} and track V_{DDM} variations as measured at the receiver. Peak-to-peak noise must not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the MSC7119 device. It is the level measured at the far end signal termination. It should be equal to V_{REF}. This rail should track variations in the DC level of V_{REF}.
4. Output leakage for the memory interface is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ V_{DDM}.
5. The core power values were measured.using a standard EFR pattern at typical conditions (25°C, 300 MHz, 1.2 V core).

Table 6 lists the DDR DRAM capacitance.

Table 6. DDR DRAM Capacitance

Parameter/Condition	Symbol	Max	Unit
Input/output capacitance: DQ, DQS	C_{IO}	30	pF
Delta input/output capacitance: DQ, DQS	C_{DIO}	30	pF

Note: These values were measured under the following conditions:
- V_{DDM} = 2.5 V ± 0.125 V
- f = 1 MHz
- T_A = 25°C
- $V_{OUT} = V_{DDM}/2$
- V_{OUT} (peak to peak) = 0.2 V

2.5.2.3 Multiplication Factor Range

The multiplier block output frequency ranges depend on the divided input clock frequency as shown in **Table 10**.

Table 10. PLLMLTF Ranges

Multiplier Block (Loop) Output Range	Minimum PLLMLTF Value	Maximum PLLMLTF Value
266 ≤ [Divided Input Clock × (PLLMLTF + 1)] ≤ 532 MHz	266/Divided Input Clock	532/Divided Input Clock
Note: This table results from the allowed range for F_{Loop}. The minimum and maximum multiplication factors are dependent on the frequency of the Divided Input Clock.		

2.5.2.4 Allowed Core Clock Frequency Range

The frequency delivered to the core, extended core, and peripherals depends on the value of the CLKCTRL[RNG] bit as shown in **Table 11**.

Table 11. F_{vco} Frequency Ranges

CLKCTRL[RNG] Value	Allowed Range of F_{vco}
1	$266 \le F_{vco} \le 532$ MHz
0	$133 \le F_{vco} \le 266$ MHz
Note: This table results from the allowed range for F_{vco}, which is F_{Loop} modified by CLKCTRL[RNG].	

This bit along with the CKSEL determines the frequency range of the core clock.

Table 12. Resulting Ranges Permitted for the Core Clock

CLKCTRL[CKSEL]	CLKCTRL[RNG]	Resulting Division Factor	Allowed Range of Core Clock	Comments
11	1	1	266 ≤ core clock ≤ 300 MHz	Limited by maximum core frequency
11	0	2	133 ≤ core clock ≤ 266 MHz	Limited by range of PLL
01	1	2	133 ≤ core clock ≤ 266 MHz	Limited by range of PLL
01	0	4	66.5 ≤ core clock ≤ 133 MHz	Limited by range of PLL
Note: This table results from the allowed range for F_{OUT}, which depends on clock selected via CLKCTRL[CKSEL].				

2.5.2.5 Core Clock Frequency Range When Using DDR Memory

The core clock can also be limited by the frequency range of the DDR devices in the system. **Table 13** summarizes this restriction.

Table 13. Core Clock Ranges When Using DDR

DDR Type	Allowed Frequency Range for DDR CK	Corresponding Range for the Core Clock	Comments
DDR 200 (PC-1600)	83–100 MHz	166 ≤ core clock ≤ 200 MHz	Core limited to 2 × maximum DDR frequency
DDR 266 (PC-2100)	83–133 MHz	166 ≤ core clock ≤ 266 MHz	Core limited to 2 × maximum DDR frequency
DDR 333 (PC-2600)	83–150 MHz	166 ≤ core clock ≤ 300 MHz	Core limited to 2 × maximum DDR frequency

2.5.3 Reset Timing

The MSC7119 device has several inputs to the reset logic. All MSC7119 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 14** describes the reset sources.

Table 14. Reset Sources

Name	Direction	Description
Power-on reset (PORESET)	Input	Initiates the power-on reset flow that resets the MSC7119 and configures various attributes of the MSC7119. On PORESET, the entire MSC7119 device is reset. SPLL and DLL states are reset, HRESET is driven, the SC1400 extended core is reset, and system configuration is sampled. The system is configured only when PORESET is asserted.
External Hard reset (HRESET)	Input/ Output	Initiates the hard reset flow that configures various attributes of the MSC7119. While HRESET is asserted, HRESET is an open-drain output. Upon hard reset, HRESET is driven and the SC1400 extended core is reset.
Software watchdog reset	Internal	When the MSC7119 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence.
Bus monitor reset	Internal	When the MSC7119 bus monitor count reaches zero, a bus monitor hard reset is asserted. The enabled bus monitor event then generates an internal hard reset sequence.
JTAG EXTEST, CLAMP, or HIGHZ command	Internal	When a Test Access Port (TAP) executes an EXTEST, CLAMP, or HIGHZ command, the TAP logic asserts an internal reset signal that generates an internal soft reset sequence.

Table 15 summarizes the reset actions that occur as a result of the different reset sources.

Table 15. Reset Actions for Each Reset Source

Reset Action/Reset Source	Power-On Reset (PORESET)	Hard Reset (HRESET)	Soft Reset (SRESET)
	External only	External or Internal (Software Watchdog or Bus Monitor)	JTAG Command: EXTEST, CLAMP, or HIGHZ
Configuration pins sampled (refer to **Section 2.5.3.1** for details).	Yes	No	No
PLL and clock synthesis states Reset	Yes	No	No
HRESET Driven	Yes	Yes	No
Software watchdog and bus time-out monitor registers	Yes	Yes	Yes
Clock synthesis modules (STOPCTRL, HLTREQ, and HLTACK) reset	Yes	Yes	Yes
Extended core reset	Yes	Yes	Yes
Peripheral modules reset	Yes	Yes	Yes

2.5.3.1 Power-On Reset (PORESET) Pin

Asserting PORESET initiates the power-on reset flow. PORESET must be asserted externally for at least 16 CLKIN cycles after external power to the MSC7119 reaches at least 2/3 V_{DD}.

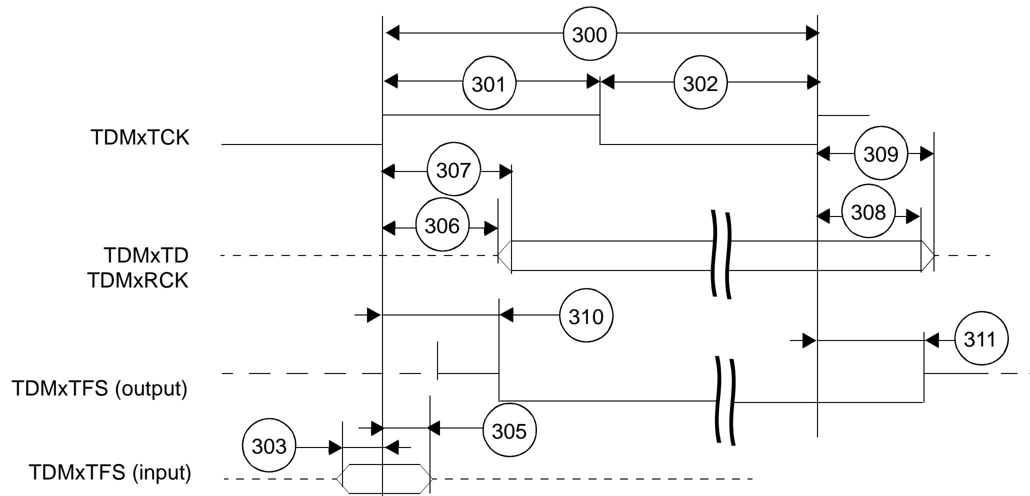

Figure 9. TDM Transmit Signals

2.5.6 Ethernet Timing

2.5.6.1 Receive Signal Timing

Table 21. Receive Signal Timing

No.	Characteristics	Min	Max	Unit
800	Receive clock period: • MII: RXCLK (max frequency = 25 MHz) • RMII: REFCLK (max frequency = 50 MHz)	 40 20	 — —	 ns ns
801	Receive clock pulse width high—as a percent of clock period • MII: RXCLK • RMII: REFCLK	35 14 7	65 — —	% ns ns
802	Receive clock pulse width low—as a percent of clock period: • MII: RXCLK • RMII: REFCLK	35 14 7	65 — —	% ns ns
803	RXDn, RX_DV, CRS_DV, RX_ER to receive clock rising edge setup time	4	—	ns
804	Receive clock rising edge to RXDn, RX_DV, CRS_DV, RX_ER hold time	2	—	ns

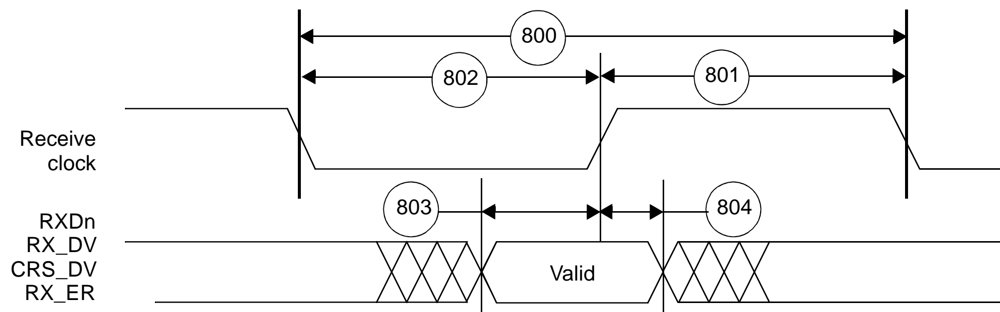

Figure 10. Ethernet Receive Signal Timing

2.5.6.4 Management Interface Timing

Table 24. Ethernet Controller Management Interface Timing

No.	Characteristics	Min	Max	Unit
808	MDC period	400	—	ns
809	MDC pulse width high	160	—	ns
810	MDC pulse width low	160	—	ns
811	MDS falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
812	MDS falling edge to MDIO output valid (maximum propagation delay)	—	15	ns
813	MDIO input to MDC rising edge setup time	10	—	ns
814	MDC rising edge to MDIO input hold time	10	—	ns

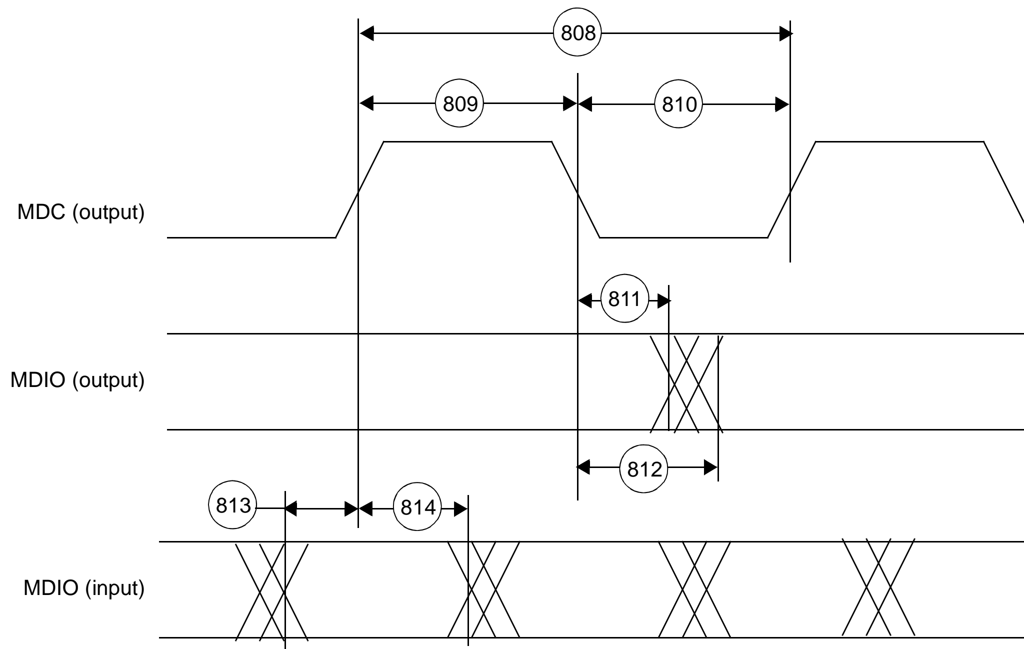

Figure 13. Serial Management Channel Timing

2.5.7 HDI16 Signals

Table 25. Host Interface (HDI16) Timing[1, 2]

No.	Characteristics[3]	Expression	Value	Unit
40	Host Interface Clock period	T_{CORE}	Note 1	ns
44a	Read data strobe minimum assertion width[4] HACK read minimum assertion width	$2.0 \times T_{CORE} + 9.0$	Note 11	ns
44b	Read data strobe minimum deassertion width[4] HACK read minimum deassertion width	$1.5 \times T_{CORE}$	Note 11	ns
44c	Read data strobe minimum deassertion width[4] after "Last Data Register" reads[5,6], or between two consecutive CVR, ICR, or ISR reads[7] HACK minimum deassertion width after "Last Data Register" reads[5,6]	$2.5 \times T_{CORE}$	Note 11	ns
45	Write data strobe minimum assertion width[8] HACK write minimum assertion width	$1.5 \times T_{CORE}$	Note 11	ns
46	Write data strobe minimum deassertion width[8] HACK write minimum deassertion width after ICR, CVR and Data Register writes[5]	$2.5 \times T_{CORE}$	Note 11	ns
47	Host data input minimum setup time before write data strobe deassertion[8] Host data input minimum setup time before HACK write deassertion	—	2.5	ns
48	Host data input minimum hold time after write data strobe deassertion[8] Host data input minimum hold time after HACK write deassertion	—	2.5	ns
49	Read data strobe minimum assertion to output data active from high impedance[4] HACK read minimum assertion to output data active from high impedance	—	1.0	ns
50	Read data strobe maximum assertion to output data valid[4] HACK read maximum assertion to output data valid	$(2.0 \times T_{CORE}) + 8.0$	Note 11	ns
51	Read data strobe maximum deassertion to output data high impedance[4] HACK read maximum deassertion to output data high impedance	—	9.0	ns
52	Output data minimum hold time after read data strobe deassertion[4] Output data minimum hold time after HACK read deassertion	—	1.0	ns
53	HCS[1–2] minimum assertion to read data strobe assertion[4]	—	0.5	ns
54	HCS[1–2] minimum assertion to write data strobe assertion[8]	—	0.0	ns
55	HCS[1–2] maximum assertion to output data valid	$(2.0 \times T_{CORE}) + 6.0$	Note 11	ns
56	HCS[1–2] minimum hold time after data strobe deassertion[9]	—	0.5	ns
57	HA[0–2], HRW minimum setup time before data strobe assertion[9]	—	5.0	ns
58	HA[0–2], HRW minimum hold time after data strobe deassertion[9]	—	5.0	ns
61	Maximum delay from read data strobe deassertion to host request deassertion for "Last Data Register" read[4, 5, 10]	$(3.0 \times T_{CORE}) + 6.0$	Note 11	ns
62	Maximum delay from write data strobe deassertion to host request deassertion for "Last Data Register" write[5,8,10]	$(3.0 \times T_{CORE}) + 6.0$	Note 11	ns
63	Minimum delay from DMA HACK (OAD=0) or Read/Write data strobe(OAD=1) deassertion to HREQ assertion.	$(2.0 \times T_{CORE}) + 1.0$	Note 11	ns
64	Maximum delay from DMA HACK (OAD=0) or Read/Write data strobe(OAD=1) assertion to HREQ deassertion	$(5.0 \times T_{CORE}) + 6.0$	Note 11	ns

Notes:

1. T_{CORE} = core clock period. At 300 MHz, T_{CORE} = 3.333 ns.
2. In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.
3. V_{DD} = 3.3 V ± 0.15 V; T_J = –40°C to +105 °C, C_L = 30 pF for maximum delay timings and C_L = 0 pF for minimum delay timings.
4. The read data strobe is HRD/HRD in the dual data strobe mode and HDS/HDS in the single data strobe mode.
5. For 64-bit transfers, the "last data register" is the register at address 0x7, which is the last location to be read or written in data transfers. This is RX0/TX0 in the little endian mode (HBE = 0), or RX3/TX3 in the big endian mode (HBE = 1).
6. This timing is applicable only if a read from the "last data register" is followed by a read from the RX[0–3] registers without first polling RXDF or HREQ bits, or waiting for the assertion of the HREQ/HREQ signal.
7. This timing is applicable only if two consecutive reads from one of these registers are executed.
8. The write data strobe is HWR in the dual data strobe mode and HDS in the single data strobe mode.
9. The data strobe is host read (HRD/HRD) or host write (HWR/HWR) in the dual data strobe mode and host data strobe (HDS/HDS) in the single data strobe mode.
10. The host request is HREQ/HREQ in the single host request mode and HRRQ/HRRQ and HTRQ/HTRQ in the double host request mode. HRRQ/HRRQ is deasserted only when HOTX fifo is empty, HTRQ/HTRQ is deasserted only if HORX fifo is full
11. Compute the value using the expression.
12. The read and write data strobe minimum deassertion width for non-"last data register" accesses in single and dual data strobe modes is based on timings 57 and 58.

3.2.2.5 Case 5 (not recommended for new designs)

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDM} (2.5 V) supply second.
3. Turn on the V_{DDC} (1.2 V) supply third.
4. Turn on the V_{REF} (1.25 V) supply fourth (last).

Note: Make sure that the time interval between the ramp-up of V_{DDIO} and V_{DDM} is less than 10 ms.

The power-down sequence is as follows:

1. Turn off the V_{REF} (1.25 V) supply first.
2. Turn off the V_{DDC} (1.2 V) supply second.
3. Turn off the V_{DDM} (2.5 V) supply third.
4. Turn of the V_{DDIO} (3.3 V) supply fourth (last).

Use the following guidelines:

- Make sure that the time interval between the ramp-down of V_{DDIO} and V_{DDM} is less than 10 ms.
- Make sure that the time interval between the ramp-up or ramp-down for V_{DDC} and V_{DDM} is less than 2 ms for power-up and power-down.
- Refer to **Figure 34** for relative timing for power sequencing case 5.

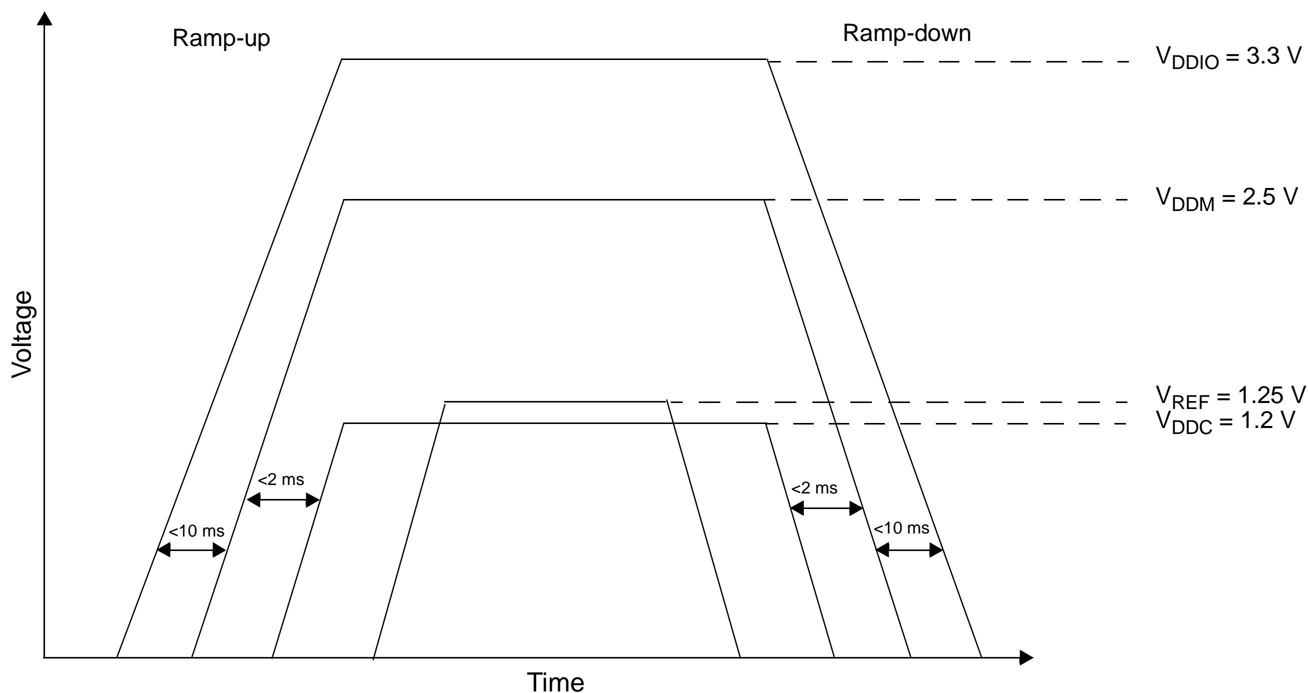

Figure 34. Voltage Sequencing Case 5

Note: Cases 1, 2, 3, and 4 are recommended for system design. Designs that use Case 5 may have large current spikes on the V_{DDM} supply at startup and is not recommended for most designs. If a design uses case 5, it must accommodate the potential current spikes. Verify risks related to current spikes using actual information for the specific application.

3.2.7 Power Supply Design

One of the most common ways to derive power is to use either a simple fixed or adjustable linear regulator. For the system I/O voltage supply, a simple fixed 3.3 V supply can be used. However, a separate adjustable linear regulator supply for the core voltage V_{DDC} should be implemented. For the memory power supply, regulators are available that take care of all DDR power requirements.

Table 33. Recommended Power Supply Ratings

Supply	Symbol	Nominal Voltage	Current Rating
Core	V_{DDC}	1.2 V	1.5 A per device
Memory	V_{DDM}	2.5 V	0.5 A per device
Reference	V_{REF}	1.25 V	10 µA per device
I/O	V_{DDIO}	3.3 V	1.0 A per device

3.3 Estimated Power Usage Calculations

The following equations permit estimated power usage to be calculated for individual design conditions. Overall power is derived by totaling the power used by each of the major subsystems:

$$P_{TOTAL} = P_{CORE} + P_{PERIPHERALS} + P_{DDRIO} + P_{IO} + P_{LEAKAGE} \quad \text{Eqn. 3}$$

This equation combines dynamic and static power. Dynamic power is determined using the generic equation:

$$C \times V^2 \times F \times 10^{-3}\ mW \quad \text{Eqn. 4}$$

where,

C = load capacitance in pF

V = peak-to-peak voltage swing in V

F = frequency in MHz

3.3.1 Core Power

Estimation of core power is straightforward. It uses the generic dynamic power equation and assumes that the core load capacitance is 750 pF, core voltage swing is 1.2 V, and the core frequency is 300 MHz. This yields:

$$P_{CORE} = 750\ pF \times (1.2\ V)^2 \times 300\ MHz \times 10^{-3} = 324.0\ mW \quad \text{Eqn. 5}$$

This equation allows for adjustments to voltage and frequency if necessary.

Table 35. Boot Mode Source Selection

BM[3–0]	Boot Port	Input Clock Frequency	Clock Divide	PLL	CKSEL	RNG Bit	Core Clock Frequency	Comments
HDI Boot Modes								
0000	HDI16	$< F_{max}$	N/A	N/A	00	0	$< F_{max}$	Not clocked by the PLL. Can boot as 8- or 16-bit HDI.
0101	HDI16	22.2-25 MHz	1	12	11	1	266–300 MHz	Can boot as 8- or 16-bit HDI.
0010	HDI16	25-33.3 MHz	2	32	01	1	200–266 MHz	
0111	HDI16	33-66 MHz	3	12	11	1	132–264 MHz	
0100	HDI16	44.3-50 MHz	2	12	11	1	266–300 MHz	
SPI Boot Modes - Using HA3, HCS2, BM3, BM2 Pins								
1000	SPI (SW)	$< F_{max}$	N/A	N/A	00	0	$< F_{max}$	The boot program automatically determines whether EEPROM or Flash memory.
1001	SPI (SW)	15.6-25 MHz	1	17	11	0	133–212.5 MHz	
1010	SPI (SW)	33-50 MHz	2	16	11	0	132–200 MHz	
1011	SPI (SW)	44.3-75 MHz	3	18	11	0	133–225 MHz	
SPI Boot Modes - Using URXD, UTXD, SCL, SDA Pins								
1100	SPI (SW)	$< F_{max}$	N/A	N/A	00	0	$< F_{max}$	Boots through different set of pins.
I^2C Boot Modes								
0001	I^2C	< 100 MHz	N/A	N/A	00	0	< 100 MHz	Not clocked by the PLL. I^2C is limited to a maximum bit rate of 400 Kbps. With a clock divider of 128, this limits the maximum input clock frequency to 100 MHz.
Reserved								
0011	Reserved	—	—	—	—	—	—	—
0110	Reserved	—	—	—	—	—	—	—
1101	Reserved	—	—	—	—	—	—	—
1110	Reserved	—	—	—	—	—	—	—
1111	Reserved	—	—	—	—	—	—	—

Notes:
1. The clock divider determines the value used in the clock module CLKCTRL[PLLDVF] field.
2. The clock multiplier determines the value used in the clock module CLKCTRL[PLLMLTF] field.
3. F_{max} is determined by the maximum frequency of the peripheral and of the SC1400 core as specified in the data sheet.

3.4.3 Boot

After a power-on reset, the PLL is bypassed and the device is directly clocked from the CLKIN pin. Thus, the device operates slowly during the boot process. After the boot program is loaded, it can enable the PLL and start the device operating at a higher speed. The MSC7119 can boot from an external host through the HDI16 or download a user program through the I^2C port. The boot operating mode is set by configuring the BM[0–3] signals sampled at the rising edge of $\overline{PORESET}$, as shown in **Table 35**. See the *MSC711x Reference Manual* for details of boot program operation.

3.4.3.1 HDI16 Boot

If the MSC7119 device boots from an external host through the HDI16, the port is configured as follows:

- Operate in Non-DMA mode.
- Operate in polled mode on the device side.
- Operate in polled mode on the external host side.
- External host must write four 16-bit values at a time with the first word as the most significant and the fourth word as the least significant.

When booting from a power-on reset, the HDI16 is additionally configurable as follows:

- 8- or 16-bit mode as specified by the H8BIT pin.
- Data strobe as specified by the HDSP and HDDS pins.

These pins are sampled only on the deassertion of power-on reset. During a boot from a hard reset, the configuration of these pins is unaffected.

Note: When the HDI16 is used for booting or other purposes, bit 0 is the least significant bit and not the most significant bit as for other DSP products.

3.4.3.2 I^{2}C Boot

When the MSC7119 device is configured to boot from the I^{2}C port, the boot program configures the GPIO pins for I^{2}C operation. Then the MSC7118 device initiates accesses to the I^{2}C module, downloading data to the MSC7118 device. The I^{2}C interface is configured as follows:

- PLL is disabled and bypassed so that the I^{2}C module is clocked with the IPBus clock.
- I^{2}C interface operates in master mode and polling is used.
- EPROM operates in slave mode.
- Clock divider is set to 128.
- Address of slave during boot is 0xA0.

The IPBus clock is internally divided to generate the bit clock, as follows:

- CLKIN must be a maximum of 100 MHz
- PLL is bypassed.
- IPBus clock = CLKIN/2 is a maximum of 50 MHz.
- I^{2}C bit clock must be less than or equal to:
  - IPBus clock/I^{2}C clock divider
  - 50 MHz (max)/128
  - 390.6 KHz

This satisfies the maximum clock rate requirement of 400 kbps for the I^{2}C interface. For details on the boot procedure, see the “Boot Program” chapter of the *MSC711x Reference Manual*.

3.4.3.3 SPI Boot

When the MSC7119 device is configured to boot from the SPI port, the boot program configures the GPIO pins for SPI operation. Then the MSC7118 device initiates accesses to the SPI module, downloading data to the MSC7118 device. When the SPI routines run in the boot ROM, the MSC7118 is always configured as the SPI master. Booting through the SPI is supported for serial EEPROM devices and serial Flash devices. When a READ_ID instruction is issued to the serial memory device and the device returns a value of 0x00 or 0xFF, the routines for accessing a serial EEPROM are used, at a maximum frequency of 4 Mbps. Otherwise, the routines for accessing a serial Flash are used, and they can run at faster speeds. Booting is performed through one of two sets of pins:

- Main set: BM[2–3], HA3, and HCS2, which allow use of the PLL.
- Alternate set: UTXD, URXD, SDA, and SCL, which cannot be used with the PLL.

In either configuration, an error during SPI boot is flagged on the EVNT3 pin. For details on the boot procedure, see the “Boot Program” chapter of the *MSC711x Reference Manual*.

3.5.3 General Routing

The general routing considerations for the DDR are as follows:

- All DDR signals must be routed next to a solid reference:
  - For data, next to solid ground planes.
  - For address/command, power planes if necessary.
- All DDR signals must be impedance controlled. This is system dependent, but typical values are 50–60 ohm.
- Minimize other cross-talk opportunities. As possible, maintain at least a four times the trace width spacing between all DDR signals to non-DDR signals.
- Keep the number of vias to a minimum to eliminate additional stubs and capacitance.
- Signal group routing priorities are as follows:
  - DDR clocks.
  - Route MVTT/MVREF.
  - Data group.
  - Command/address.
- Minimize data bit jitter by trace matching.

3.5.4 Routing Clock Distribution

The DDR clock distribution considerations are as follows:

- DDR controller supports six clock pairs:
  - 2 DIMM modules.
  - Up to 36 discrete chips.
- For route traces as for any other differential signals:
  - Maintain proper difference pair spacing.
  - Match pair traces within 25 mm.
- Match all clock traces to within 100 mm.
- Keep all clocks equally loaded in the system.
- Route clocks on inner critical layers.

3.5.5 Data Routing

The DDR data routing considerations are as follows:

- Route each data group (8-bits data + DQS + DM) on the same layer. Avoid switching layers within a byte group.
- Take care to match trace lengths, which is extremely important.
- To make trace matching easier, let adjacent groups be routed on alternate critical layers.
- Pin swap bits within a byte group to facilitate routing (discrete case).
- Tight trace matching is recommended within the DDR data group. Keep each 8-bit datum and its DM signal within ± 25 mm of its respective strobe.
- Minimize lengths across the entire DDR channel:
  - Between all groups maintain a delta of no more than 500 mm.
  - Allows greater flexibility in the design for readjustments as needed.
- DDR data group separation:
  - If stack-up allows, keep DDR data groups away from the address and control nets.
  - Route address and control on separate critical layers.
  - If resistor networks (RNs) are used, attempt to keep data and command lines in separate packages.

3.6 Connectivity Guidelines

This section summarizes the connections and special conditions, such as pull-up or pull-down resistors, for the MSC7119 device. Following are guidelines for signal groups and configuration settings:

- *Clock and reset signals*.
  - SWTE is used to configure the MSC7119 device and is sampled on the deassertion of $\overline{\text{PORESET}}$, so it should be tied to V_{DDC} or GND either directly or through pull-up or pull-down resistors until $\overline{\text{PORESET}}$ is deasserted. After $\overline{\text{PORESET}}$, this signal can be left floating.
  - BM[0–1] configure the MSC7119 device and are sampled until $\overline{\text{PORESET}}$ is deasserted, so they should be tied to V_{DDIO} or GND either directly or through pull-up or pull-down resistors.
  - $\overline{\text{HRESET}}$ should be pulled up.
- *Interrupt signals*. When used, $\overline{\text{IRQ}}$ pins must be pulled up.
- *HDI16 signals*.
  - When they are configured for open-drain, the $\overline{\text{HREQ}}$/HREQ or $\overline{\text{HTRQ}}$/HTRQ signals require a pull-up resistor. However, these pins are also sampled at power-on reset to determine the HDI16 boot mode and may need to be pulled down. When these pins must be pulled down on reset and pulled up otherwise, a buffer can be used with the $\overline{\text{HRESET}}$ signal as the enable.
  - When the device boots through the HDI16, the HDDS, HDSP and H8BIT pins should be pulled up or down, depending on the required boot mode settings.
- *Ethernet MAC/TDM2 signals*. The MDIO signal requires an external pull-up resistor.
- *I^2C signals*. The SCL and SDA signals, when programmed for I^2C, requires an external pull-up resistor.
- *General-purpose I/O (GPIO) signals*. An unused GPIO pin can be disconnected. After boot, program it as an output pin.
- Other signals.
  - The $\overline{\text{TEST0}}$ pin must be connected to ground.
  - The $\overline{\text{TPSEL}}$ pin should be pulled up to enable debug access via the EOnCE port and pulled down for boundary scan.
  - Pins labelled NO CONNECT (NC) must not be connected.
  - When a 16-pin double data rate (DDR) interface is used, the 16 unused data pins should be no connects (floating) if the used lines are terminated.
  - Do not connect DBREQ to DONE (as you would for the MSC8101 device). Connect DONE to one of the EVNT pins, and DBREQ to HRRQ.

4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Supply Voltage	Package Type	Pin Count	Core Frequency (MHz)	Solder Spheres	Order Number
MSC7119	1.2 V core 2.5 V memory 3.3 V I/O	Molded Array Process-Ball Grid Array (MAP-BGA)	400	300	Lead-free	MSC7119VM1200
					Lead-bearing	MSC7119VF1200

7 Revision History

Table 36 provides a revision history for this data sheet.

Table 36. Document Revision History

Revision	Date	Description
0	Sep. 2005	• Initial public release.
1	Oct 2005	• Added explanatory note to HDI16 timing table.
2	Oct. 2005	• Added information about signals GPIOB11, GPIOC11, GPIOD7, and GPIOD8 to the signal descriptions and pinout location lists.
3	Dec. 2005	• Added information about signals GPIOA16, GPIOA17, GPIOA27, GPIOA28, and GPIOA29 to signal description and pinout location lists.
4	Feb. 2006	• Updated orderable part numbers.
5	Nov. 2006	• Updated Reference Manual reference to MSC711x Reference Manual. • Updated arrows in Host DMA Writing Timing figure.
6	Jun. 2007	• Updated to new data sheet format. Reorganized and renumbered sections, figures, and tables. • Added a note to clarify the definition of TCK timing 700 in new **Table 31**. • Removed references to V_{CCSYN} and V_{CCSYN1} in the new power supply design recommendation **Section 3.2**.
7	Aug 2007	• The power-up and power-down sequences described in **Section 3.2** starting on page 42 have been expanded to five possible design scenarios/cases. These cases replace the previously recommended power-up/power-down sequence recommendations. **Section 3.2** has been clarified by adding subsection headings.
8	Apr 2008	• Change the PLL filter resistor from 20 Ω to 2 Ω in **Section 3.2.5**.

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