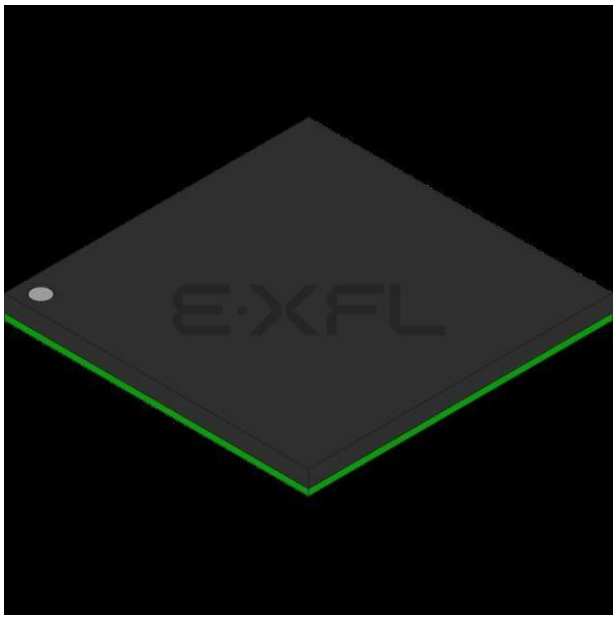

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, I²C, UART
Clock Rate	300MHz
Non-Volatile Memory	ROM (8kB)
On-Chip RAM	464kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	400-LFBGA
Supplier Device Package	400-PBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=msc7119vm1200

Bottom View

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	NC	NC	NC	NC	BM3	GND	HD0	HD1	HD4	HD6	HD7	HD10	HD12	HD15	$\overline{CK}$	CK	DQS2	DQM1	GND	GND
B	NC	NC	NC	NC	NC	BM2	NC	HD2	HD5	HD8	HD11	HD14	$\overline{WE}$	CKE	DQS0	DQS3	DQM2	$\overline{CS0}$	NC	V_{DDM}
C	NC	NC	NC	NC	NC	NC	NC	NC	HD3	HD9	HD13	$\overline{CAS}$	$\overline{RAS}$	DQS1	DQM0	DQM3	$\overline{CS1}$	D25	D30	D24
D	NC	NC	NC	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	GND	D27	D28	V_{DDM}
E	NC	NC	NC	V_{DD}	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDM}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DDM}	V_{DDM}	D31	D26	GND
F	NC	NC	NC	V_{DD}	V_{DD}	V_{DDIO}	GND	GND	GND	V_{DDM}	V_{DDM}	GND	GND	GND	V_{DD}	V_{DD}	V_{DD}	D29	D15	V_{DDM}
G	NC	NC	NC	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	GND	D13	GND
H	HA1	HA2	NC	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	D11	D12	D14
J	$\overline{HREQ}$	$\overline{HACK}$	HA3	V_{DD}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	V_{DDM}	D9	V_{DDM}	D10
K	$\overline{HDS}$	HDDS	HA0	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DD}	D8	GND	D0
L	HRW	$\overline{HCS1}$	$\overline{HCS2}$	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DD}	D3	GND	D1
M	URXD	UTXD	SDA	V_{DD}	V_{DD}	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	D5	V_{DDM}	D2
N	V_{SSPLL}	SCL	CLKIN	V_{DD}	V_{DD}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	V_{DDM}	V_{REF}	D6	D4
P	V_{DDPLL}	TPSEL	$\overline{PORESET}$	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	V_{DDM}	D16	D17	D7
R	TEST0	EE0	TDO	V_{DD}	V_{DDIO}	V_{DDIO}	GND	V_{DDIO}	GND	GND	V_{DDM}	GND	V_{DDM}	GND	V_{DDM}	V_{DDM}	V_{DDM}	D18	D19	GND
T	$\overline{HRESET}$	TMS	MDIO	V_{DD}	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDM}	V_{DDM}	V_{DD}	V_{DDM}	V_{DDM}	V_{DD}	V_{DDM}	V_{DDM}	D22	D20	V_{DDM}
U	$\overline{TRST}$	TCK	COL	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DDM}	D23	D21	GND
V	TDI	CRS	TX_EN	RXD0	RXD2	TX_ER	T1TD	T1RFS	T0TCK	EVNT4	EVNT0	NC	BA0	A2	A5	A10	A11	A13	NC	V_{DDM}
W	MDC	RX_ER	TXCLK	TXD1	RXD3	TXD2	T1TFS	T1RD	T0TFS	T0RFS	EVNT2	EVNT1	NC	A3	A6	A7	A8	A12	V_{DDM}	GND
Y	RX_DV	GND	RXD1	TXD0	RXCLK	TXD3	T1TCK	T1RCK	TOTD	T0RD	T0RCK	EVNT3	$\overline{NMI}$	BA1	A4	A0	A1	A9	GND	V_{DDM}

Figure 3. MSC7119 Molded Array Process-Ball Grid Array (MAP-BGA), Bottom View

Table 1. MSC7119 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
D10	V_{DDM}					
D11	V_{DDIO}					
D12	V_{DDIO}					
D13	V_{DDIO}					
D14	V_{DDIO}					
D15	V_{DDIO}					
D16	V_{DDIO}					
D17	V_{DDC}					
D18	NC					
D19	NC					
D20	NC					
E1	GND					
E2	D26					
E3	D31					
E4	V_{DDM}					
E5	V_{DDM}					
E6	V_{DDC}					
E7	V_{DDC}					
E8	V_{DDC}					
E9	V_{DDC}					
E10	V_{DDM}					
E11	V_{DDIO}					
E12	V_{DDIO}					
E13	V_{DDIO}					
E14	V_{DDIO}					
E15	V_{DDIO}					
E16	V_{DDC}					
E17	V_{DDC}					
E18	NC					
E19	NC					
E20	NC					
F1	V_{DDM}					
F2	D15					
F3	D29					
F4	V_{DDC}					
F5	V_{DDC}					

Table 1. MSC7119 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
F6	V_{DDC}					
F7	GND					
F8	GND					
F9	GND					
F10	V_{DDM}					
F11	V_{DDM}					
F12	GND					
F13	GND					
F14	GND					
F15	V_{DDIO}					
F16	V_{DDC}					
F17	V_{DDC}					
F18	NC					
F19	NC					
F20	NC					
G1	GND					
G2	D13					
G3	GND					
G4	V_{DDM}					
G5	V_{DDM}					
G6	GND					
G7	GND					
G8	GND					
G9	GND					
G10	GND					
G11	GND					
G12	GND					
G13	GND					
G14	GND					
G15	V_{DDIO}					
G16	V_{DDIO}					
G17	V_{DDC}					
G18	NC					
G19	NC					
G20	NC					
H1	D14					

Table 1. MSC7119 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
J18	GPIC11			GPOC11	HA3	
J19	reserved				$\overline{\text{HACK}}$/HACK or $\overline{\text{HRRQ}}$/HRRQ	
J20	HDSP	reserved			$\overline{\text{HREQ}}$/HREQ or $\overline{\text{HTRQ}}$/HTRQ	
K1	D0					
K2	GND					
K3	D8					
K4	V_{DDC}					
K5	V_{DDM}					
K6	GND					
K7	GND					
K8	GND					
K9	GND					
K10	GND					
K11	GND					
K12	GND					
K13	GND					
K14	GND					
K15	V_{DDIO}					
K16	V_{DDIO}					
K17	V_{DDC}					
K18	reserved				HA0	
K19	reserved				HDDS	
K20	reserved				$\overline{\text{HDS}}$/HDS or $\overline{\text{HWR}}$/HWR	
L1	D1					
L2	GND					
L3	D3					
L4	V_{DDC}					
L5	V_{DDM}					
L6	GND					
L7	GND					
L8	GND					
L9	GND					
L10	GND					
L11	GND					
L12	GND					
L13	GND					

Table 5. DC Electrical Characteristics (continued)

Characteristic	Symbol	Min	Typical	Max	Unit
Tri-state (high impedance off state) leakage current, $V_{IN} = V_{DDIO}$	I_{OZ}	–1.0	0.09	1	µA
Signal low input current, V_{IL} = 0.4 V	I_L	–1.0	0.09	1	µA
Signal high input current, V_{IH} = 2.0 V	I_H	–1.0	0.09	1	µA
Output high voltage, I_{OH} = –2 mA, except open drain pins	V_{OH}	2.0	3.0	—	V
Output low voltage, I_{OL}= 5 mA	V_{OL}	—	0	0.4	V
Typical power at 300 MHz[5]	P	—	324.0	—	mW

Notes:
1. The value of V_{DDM} at the MSC7119 device must remain within 50 mV of V_{DDM} at the DRAM device at all times.
2. V_{REF} must be equal to 50% of V_{DDM} and track V_{DDM} variations as measured at the receiver. Peak-to-peak noise must not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the MSC7119 device. It is the level measured at the far end signal termination. It should be equal to V_{REF}. This rail should track variations in the DC level of V_{REF}.
4. Output leakage for the memory interface is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ V_{DDM}.
5. The core power values were measured.using a standard EFR pattern at typical conditions (25°C, 300 MHz, 1.2 V core).

Table 6 lists the DDR DRAM capacitance.

Table 6. DDR DRAM Capacitance

Parameter/Condition	Symbol	Max	Unit
Input/output capacitance: DQ, DQS	C_{IO}	30	pF
Delta input/output capacitance: DQ, DQS	C_{DIO}	30	pF

Note: These values were measured under the following conditions:
- V_{DDM} = 2.5 V ± 0.125 V
- f = 1 MHz
- T_A = 25°C
- $V_{OUT} = V_{DDM}/2$
- V_{OUT} (peak to peak) = 0.2 V

2.5 AC Timings

This section presents timing diagrams and specifications for individual signals and parallel I/O outputs and inputs. All AC timings are based on a 30 pF load, except where noted otherwise, and a 50 Ω transmission line. For any additional pF, use the following equations to compute the delay:

— Standard interface: 2.45 + (0.054 × C_{load}) ns
— DDR interface: 1.6 + (0.002 × C_{load}) ns

2.5.1 Clock and Timing Signals

The following tables describe clock signal characteristics. **Table 6** shows the maximum frequency values for internal (core, reference, and peripherals) and external (CLKO) clocks. You must ensure that maximum frequency values are not exceeded (see **Section 2.5.2** for the allowable ranges when using the PLL).

Table 6. Maximum Frequencies

Characteristic	Maximum in MHz
Core clock frequency (CLOCK)	300
External output clock frequency (CLKO)	75
Memory clock frequency (CK, $\overline{CK}$)	150
TDM clock frequency (TxRCK, TxTCK)	50

Table 7. Clock Frequencies in MHz

Characteristic	Symbol	Min	Max
CLKIN frequency	F_{CLKIN}	10	100
CLOCK frequency	F_{CORE}	—	300
CK, $\overline{CK}$ frequency	F_{CK}	—	150
TDMxRCK, TDMxTCK frequency	F_{TDMCK}	—	50
CLKO frequency	F_{CKO}	—	75
AHB/IPBus/APB clock frequency	F_{BCK}	—	150
Note: The rise and fall time of external clocks should be 5 ns maximum			

Table 8. System Clock Parameters

Characteristic	Min	Max	Unit
CLKIN frequency	10	100	MHz
CLKIN slope	—	5	ns
CLKIN frequency jitter (peak-to-peak)	—	1000	ps
CLKO frequency jitter (peak-to-peak)	—	150	ps

2.5.3 Reset Timing

The MSC7119 device has several inputs to the reset logic. All MSC7119 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 14** describes the reset sources.

Table 14. Reset Sources

Name	Direction	Description
Power-on reset (PORESET)	Input	Initiates the power-on reset flow that resets the MSC7119 and configures various attributes of the MSC7119. On PORESET, the entire MSC7119 device is reset. SPLL and DLL states are reset, HRESET is driven, the SC1400 extended core is reset, and system configuration is sampled. The system is configured only when PORESET is asserted.
External Hard reset (HRESET)	Input/ Output	Initiates the hard reset flow that configures various attributes of the MSC7119. While HRESET is asserted, HRESET is an open-drain output. Upon hard reset, HRESET is driven and the SC1400 extended core is reset.
Software watchdog reset	Internal	When the MSC7119 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence.
Bus monitor reset	Internal	When the MSC7119 bus monitor count reaches zero, a bus monitor hard reset is asserted. The enabled bus monitor event then generates an internal hard reset sequence.
JTAG EXTEST, CLAMP, or HIGHZ command	Internal	When a Test Access Port (TAP) executes an EXTEST, CLAMP, or HIGHZ command, the TAP logic asserts an internal reset signal that generates an internal soft reset sequence.

Table 15 summarizes the reset actions that occur as a result of the different reset sources.

Table 15. Reset Actions for Each Reset Source

Reset Action/Reset Source	Power-On Reset (PORESET)	Hard Reset (HRESET)	Soft Reset (SRESET)
	External only	External or Internal (Software Watchdog or Bus Monitor)	JTAG Command: EXTEST, CLAMP, or HIGHZ
Configuration pins sampled (refer to **Section 2.5.3.1** for details).	Yes	No	No
PLL and clock synthesis states Reset	Yes	No	No
HRESET Driven	Yes	Yes	No
Software watchdog and bus time-out monitor registers	Yes	Yes	Yes
Clock synthesis modules (STOPCTRL, HLTREQ, and HLTACK) reset	Yes	Yes	Yes
Extended core reset	Yes	Yes	Yes
Peripheral modules reset	Yes	Yes	Yes

2.5.3.1 Power-On Reset (PORESET) Pin

Asserting PORESET initiates the power-on reset flow. PORESET must be asserted externally for at least 16 CLKIN cycles after external power to the MSC7119 reaches at least 2/3 V_{DD}.

2.5.3.2 Reset Configuration

The MSC7119 has two mechanisms for writing the reset configuration:

- From a host through the host interface (HDI16)
- From memory through the I^2C interface

Five signal levels (see **Chapter 1** for signal description details) are sampled on $\overline{\text{PORESET}}$ deassertion to define the boot and operating conditions:

- BM[0–1]
- SWTE
- H8BIT
- HDSP

2.5.3.3 Reset Timing Tables

Table 16 and **Figure 4** describe the reset timing for a reset configuration write.

Table 16. Timing for a Reset Configuration Write

No.	Characteristics	Expression	Unit
1	Required external $\overline{\text{PORESET}}$ duration minimum	$16/F_{CLKIN}$	clocks
2	Delay from $\overline{\text{PORESET}}$ deassertion to $\overline{\text{HRESET}}$ deassertion	$521/F_{CLKIN}$	clocks
Note:	Timings are not tested, but are guaranteed by design.		

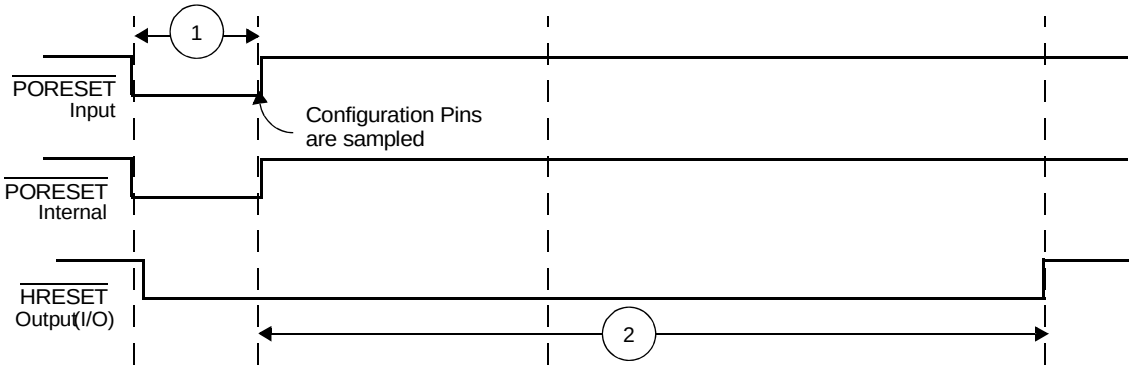


Figure 4. Timing Diagram for a Reset Configuration Write

2.5.4 DDR DRAM Controller Timing

This section provides the AC electrical characteristics for the DDR DRAM interface.

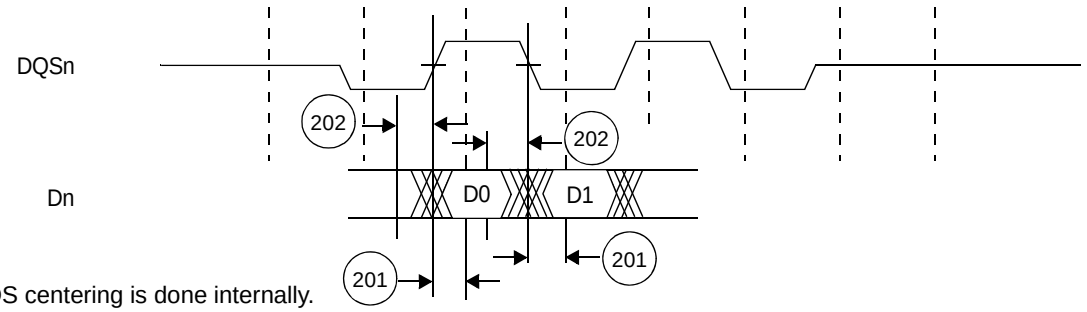
2.5.4.1 DDR DRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR DRAM interface.

Table 17. DDR DRAM Input AC Timing

No.	Parameter	Symbol	Min	Max	Unit
—	AC input low voltage	V_{IL}	—	V_{REF} – 0.31	V
—	AC input high voltage	V_{IH}	V_{REF} + 0.31	V_{DDM} + 0.3	V
201	Maximum Dn input setup skew relative to DQSn input	—	—	900	ps
202	Maximum Dn input hold skew relative to DQSn input	—	—	900	ps

Notes:
1. Maximum possible skew between a data strobe (DQSn) and any corresponding bit of data (D[8n + {0...7}] if 0 ≤ n ≤ 7).
2. See **Table 18** for t_{CK} value.
3. Dn should be driven at the same time as DQSn. This is necessary because the DQSn centering on the DQn data tenure is done internally.



Note: DQS centering is done internally.

Figure 5. DDR DRAM Input Timing Diagram

2.5.4.2 DDR DRAM Output AC Timing Specifications

Table 18 and **Table 19** list the output AC timing specifications and measurement conditions for the DDR DRAM interface.

Table 18. DDR DRAM Output AC Timing

No.	Parameter	Symbol	Min	Max	Unit
200	CK cycle time, (CK/$\overline{CK}$ crossing)[1] • 100 MHz (DDR200) • 150 MHz (DDR300)	t_{CK}	 10 6.67	 — —	 ns ns
204	An/$\overline{RAS}$/$\overline{CAS}$/$\overline{WE}$/CKE output setup with respect to CK	t_{DDKHAS}	0.5 × t_{CK} – 1000	—	ps
205	An/$\overline{RAS}$/$\overline{CAS}$/$\overline{WE}$/CKE output hold with respect to CK	t_{DDKHAX}	0.5 × t_{CK} – 1000	—	ps
206	$\overline{CSn}$ output setup with respect to CK	t_{DDKHCS}	0.5 × t_{CK} – 1000	—	ps
207	$\overline{CSn}$ output hold with respect to CK	t_{DDKHCX}	0.5 × t_{CK} – 1000	—	ps
208	CK to DQSn[2]	t_{DDKHMH}	–600	600	ps

Table 18. DDR DRAM Output AC Timing (continued)

No.	Parameter	Symbol	Min	Max	Unit
209	Dn/DQMn output setup with respect to DQSn[3]	t_{DDKHDS}, t_{DDKLDS}	$0.25 \times t_{CK} - 750$	—	ps
210	Dn/DQMn output hold with respect to DQSn[3]	t_{DDKHDX}, t_{DDKLDX}	$0.25 \times t_{CK} - 750$	—	ps
211	DQSn preamble start[4]	t_{DDKHMP}	$-0.25 \times t_{CK}$	—	ps
212	DQSn epilogue end[5]	t_{DDKHME}	–600	600	ps

Notes:
1. All CK/$\overline{CK}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
2. t_{DDKHMH} can be modified through the TCFG2[WRDD] DQSS override bits. The DRAM requires that the first write data strobe arrives 75–125% of a DRAM cycle after the write command is issued. Any skew between DQSn and CK must be considered when trying to achieve this 75%–125% goal. The TCFG2[WRDD] bits can be used to shift DQSn by 1/4 DRAM cycle increments. The skew in this case refers to an internal skew existing at the signal connections. By default, the CK/$\overline{CK}$ crossing occurs in the middle of the control signal (An/$\overline{RAS}$/$\overline{CAS}$/$\overline{WE}$/CKE) tenure. Setting TCFG2[ACSM] bit shifts the control signal assertion 1/2 DRAM cycle earlier than the default timing. This means that the signal is asserted no earlier than 600 ps before the CK/$\overline{CK}$ crossing and no later than 600 ps after the crossing time; the device uses 1200 ps of the skew budget (the interval from –600 to +600 ps). Timing is verified by referencing the falling edge of CK. See Chapter 10 of the *MSC711x Reference Manual* for details.
3. Determined by maximum possible skew between a data strobe (DQS) and any corresponding bit of data. The data strobe should be centered inside of the data eye.
4. Please note that this spec is in reference to the DQSn first rising edge. It could also be referenced from CK(r), but due to programmable delay of the write strobes (TCFG2[WRDD]), there pre-amble may be extended for a full DRAM cycle. For this reason, we reference from DQSn.
5. All outputs are referenced to the rising edge of CK. Note that this is essentially the CK/DQSn skew in spec 208. In addition there is no real “maximum” time for the epilogue end. JEDEC does not require this is as a device limitation, but simply for the chip to guarantee fast enough write-to-read turn-around times. This is already guaranteed by the memory controller operation.

Figure 6 shows the DDR DRAM output timing diagram.

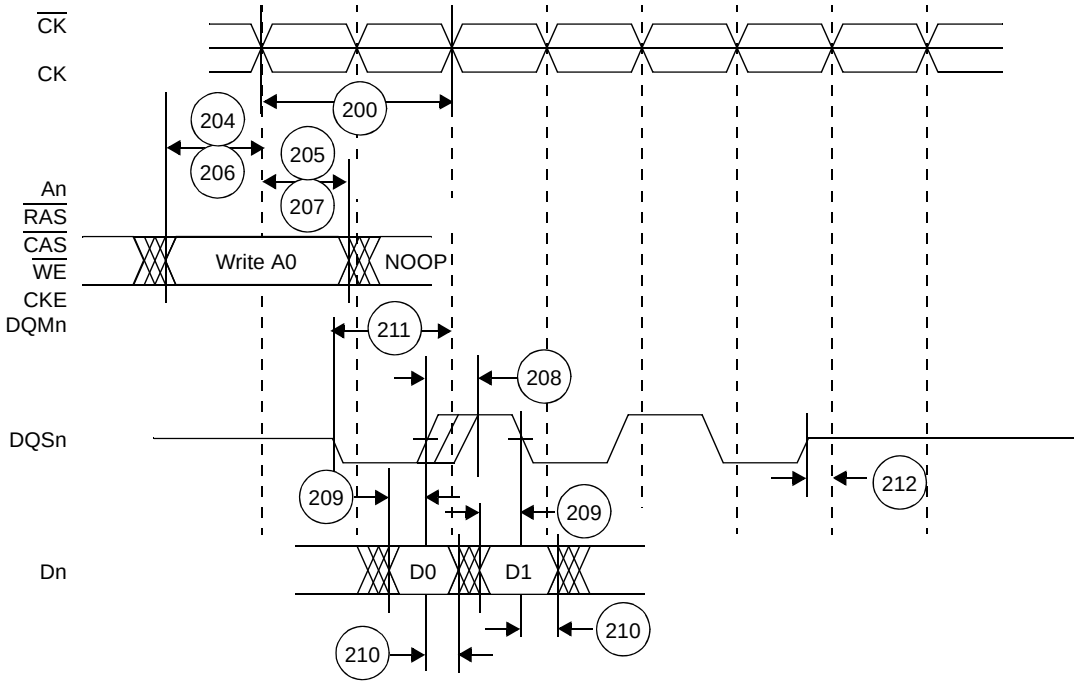


Figure 6. DDR DRAM Output Timing Diagram

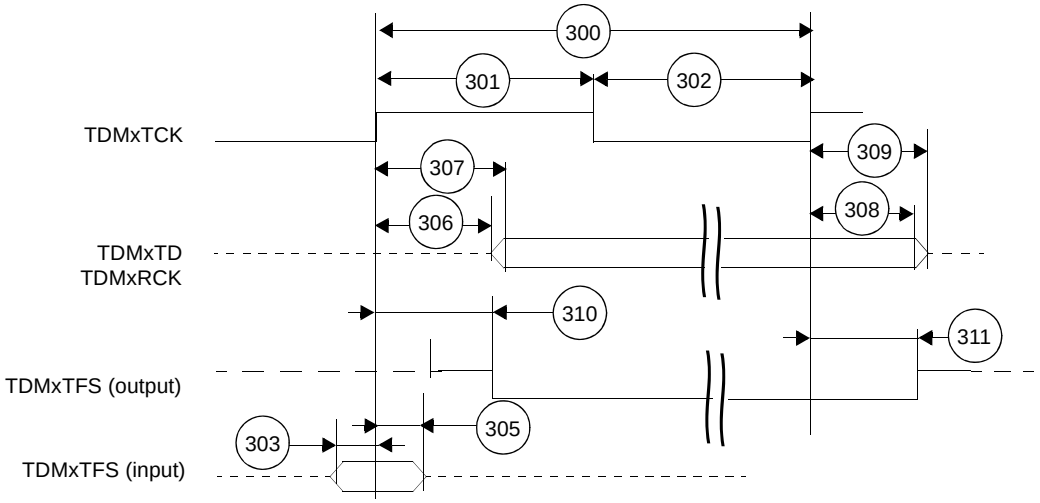


Figure 9. TDM Transmit Signals

2.5.6 Ethernet Timing

2.5.6.1 Receive Signal Timing

Table 21. Receive Signal Timing

No.	Characteristics	Min	Max	Unit
800	Receive clock period: • MII: RXCLK (max frequency = 25 MHz) • RMII: REFCLK (max frequency = 50 MHz)	 40 20	 — —	 ns ns
801	Receive clock pulse width high—as a percent of clock period • MII: RXCLK • RMII: REFCLK	35 14 7	65 — —	% ns ns
802	Receive clock pulse width low—as a percent of clock period: • MII: RXCLK • RMII: REFCLK	35 14 7	65 — —	% ns ns
803	RXDn, RX_DV, CRS_DV, RX_ER to receive clock rising edge setup time	4	—	ns
804	Receive clock rising edge to RXDn, RX_DV, CRS_DV, RX_ER hold time	2	—	ns

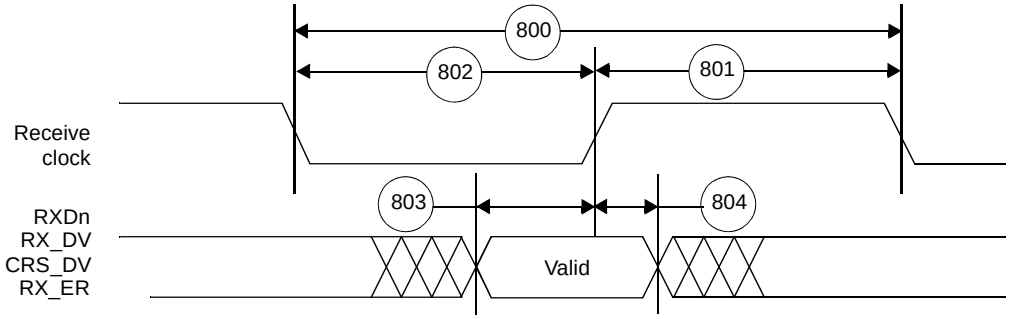


Figure 10. Ethernet Receive Signal Timing

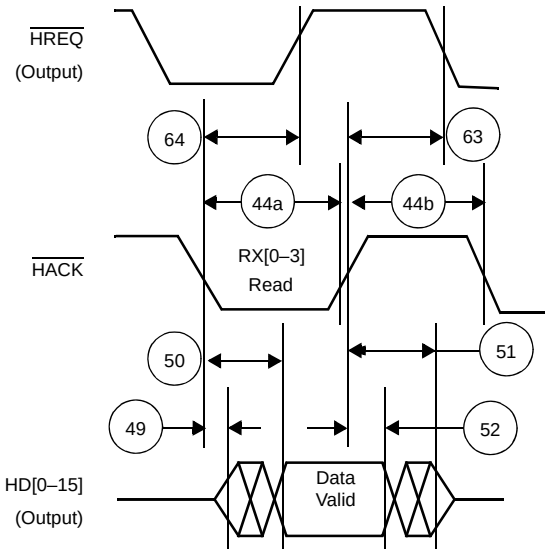


Figure 18. Host DMA Read Timing Diagram, HPCR[OAD] = 0

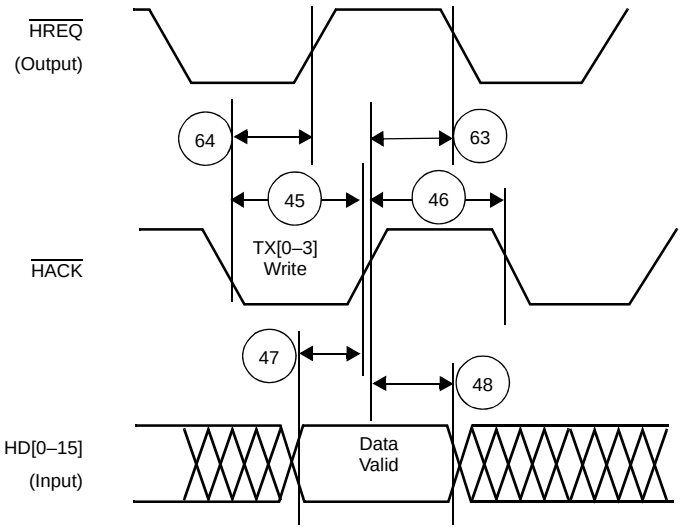


Figure 19. Host DMA Write Timing Diagram, HPCR[OAD] = 0

2.5.13 JTAG Signals

Table 31. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
700	TCK frequency of operation (1/($T_C \times 3$) **Note:** T_C = 1/CLOCK which is the period of the core clock. The TCK frequency must less than 1/3 of the core frequency with an absolute maximum limit of 40 MHz.	0.0	40.0	MHz
701	TCK cycle time	25.0	—	ns
702	TCK clock pulse width measured at V_M = 1.6 V	11.0	—	ns
703	TCK rise and fall times	0.0	3.0	ns
704	Boundary scan input data set-up time	5.0	—	ns
705	Boundary scan input data hold time	14.0	—	ns
706	TCK low to output data valid	0.0	20.0	ns
707	TCK low to output high impedance	0.0	20.0	ns
708	TMS, TDI data set-up time	5.0	—	ns
709	TMS, TDI data hold time	14.0	—	ns
710	TCK low to TDO data valid	0.0	24.0	ns
711	TCK low to TDO high impedance	0.0	10.0	ns
712	$\overline{\text{TRST}}$ assert time	100.0	—	ns

Note: All timings apply to OCE module data transfers as the OCE module uses the JTAG port as an interface.

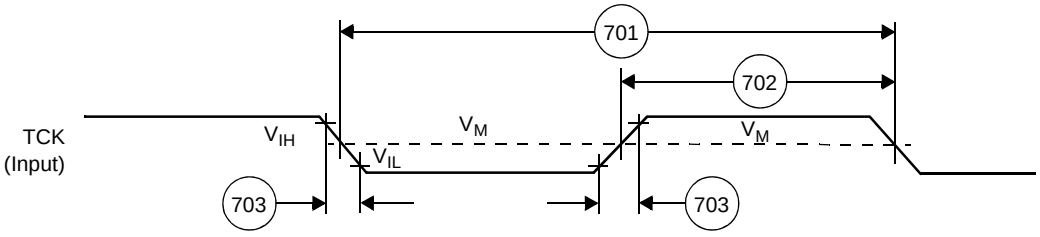


Figure 26. Test Clock Input Timing Diagram

3 Hardware Design Considerations

This section described various areas to consider when incorporating the MSC7119 device into a system design.

3.1 Thermal Design Considerations

An estimation of the chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textit{Eqn. 1}$$

where

T_A = ambient temperature near the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$P_D = P_{INT} + P_{I/O}$ = power dissipation in the package (W)

$P_{INT} = I_{DD} \times V_{DD}$ = internal power dissipation (W)

$P_{I/O}$ = power dissipated from device on output pins (W)

The power dissipation values for the MSC7119 are listed in **Table 4**. The ambient temperature for the device is the air temperature in the immediate vicinity that would cool the device. The junction-to-ambient thermal resistances are JEDEC standard values that provide a quick and easy estimation of thermal performance. There are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. The value that more closely approximates a specific application depends on the power dissipated by other components on the printed circuit board (PCB). The value obtained using a single layer board is appropriate for tightly packed PCB configurations. The value obtained using a board with internal planes is more appropriate for boards with low power dissipation (less than 0.02 W/cm^2 with natural convection) and well separated components. Based on an estimation of junction temperature using this technique, determine whether a more detailed thermal analysis is required. Standard thermal management techniques can be used to maintain the device thermal junction temperature below its maximum. If T_J appears to be too high, either lower the ambient temperature or the power dissipation of the chip.

You can verify the junction temperature by measuring the case temperature using a small diameter thermocouple (40 gauge is recommended) or an infrared temperature sensor on a spot on the device case. Use the following equation to determine T_J:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 2}$$

where

T_T = thermocouple (or infrared) temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

3.2 Power Supply Design Considerations

This section outlines the MSC7119 power considerations: power supply, power sequencing, power planes, decoupling, power supply filtering, and power consumption. It also presents a recommended power supply design and options for low-power consumption. For information on AC/DC electrical specifications and thermal characteristics, refer to **Section 2**.

3.2.1 Power Supply

The MSC7119 requires four input voltages, as shown in **Table 32**.

Table 32. MSC7119 Voltages

Voltage	Symbol	Value
Core	V_{DDC}	1.2 V
Memory	V_{DDM}	2.5 V
Reference	V_{REF}	1.25 V
I/O	V_{DDIO}	3.3 V

You should supply the MSC7119 core voltage via a variable switching supply or regulator to allow for compatibility with possible core voltage changes on future silicon revisions. The core voltage is supplied with 1.2 V (+5% and –10%) across V_{DDC} and GND and the I/O section is supplied with 3.3 V (± 10%) across V_{DDIO} and GND. The memory and reference voltages supply the DDR memory controller block. The memory voltage is supplied with 2.5 V across V_{DDM} and GND. The reference voltage is supplied across V_{REF} and GND and must be between $0.49 \times V_{DDM}$ and $0.51 \times V_{DDM}$. Refer to the JEDEC standard JESD8 (*Stub Series Terminated Logic for 2.5 Volts* (STTL_2)) for memory voltage supply requirements.

3.2.2 Power Sequencing

One consequence of multiple power supplies is that the voltage rails ramp up at different rates when power is initially applied. The rates depend on the power supply, the type of load on each power supply, and the way different voltages are derived. It is extremely important to observe the power up and power down sequences at the board level to avoid latch-up, forward biasing of ESD devices, and excessive currents, which all lead to severe device damage.

Note: There are five possible power-up/power-down sequence cases. The first four cases listed in the following sections are recommended for new designs. The fifth case is not recommended for new designs and must be carefully evaluated for current spike risks based on actual information for the specific application.

3.2.7 Power Supply Design

One of the most common ways to derive power is to use either a simple fixed or adjustable linear regulator. For the system I/O voltage supply, a simple fixed 3.3 V supply can be used. However, a separate adjustable linear regulator supply for the core voltage V_{DDC} should be implemented. For the memory power supply, regulators are available that take care of all DDR power requirements.

Table 33. Recommended Power Supply Ratings

Supply	Symbol	Nominal Voltage	Current Rating
Core	V_{DDC}	1.2 V	1.5 A per device
Memory	V_{DDM}	2.5 V	0.5 A per device
Reference	V_{REF}	1.25 V	10 µA per device
I/O	V_{DDIO}	3.3 V	1.0 A per device

3.3 Estimated Power Usage Calculations

The following equations permit estimated power usage to be calculated for individual design conditions. Overall power is derived by totaling the power used by each of the major subsystems:

$$P_{TOTAL} = P_{CORE} + P_{PERIPHERALS} + P_{DDRIO} + P_{IO} + P_{LEAKAGE} \quad \textit{Eqn. 3}$$

This equation combines dynamic and static power. Dynamic power is determined using the generic equation:

$$C \times V^2 \times F \times 10^{-3}\ mW \quad \textit{Eqn. 4}$$

where,

C = load capacitance in pF

V = peak-to-peak voltage swing in V

F = frequency in MHz

3.3.1 Core Power

Estimation of core power is straightforward. It uses the generic dynamic power equation and assumes that the core load capacitance is 750 pF, core voltage swing is 1.2 V, and the core frequency is 300 MHz. This yields:

$$P_{CORE} = 750\ pF \times (1.2\ V)^2 \times 300\ MHz \times 10^{-3} = 324.0\ mW \quad \textit{Eqn. 5}$$

This equation allows for adjustments to voltage and frequency if necessary.

3.3.6 Example Total Power Consumption

Using the examples in this section and assuming four peripherals and 10 I/O lines active, a total power consumption value is estimated as the following:

$$P_{TOTAL} = 324.0 + (4 \times 4.32) + 326.3 + (10 \times 5.44) + 64 = 784.98\ mW \qquad \textit{Eqn. 13}$$

3.4 Reset and Boot

This section describes the recommendations for configuring the MSC7119 at reset and boot.

3.4.1 Reset Circuit

$\overline{\text{HRESET}}$ is a bidirectional signal and, if driven as an input, should be driven with an open collector or open-drain device. For an open-drain output such as $\overline{\text{HRESET}}$, take care when driving many buffers that implement input bus-hold circuitry. The bus-hold currents can cause enough voltage drop across the pull-up resistor to change the logic level to low. Either a smaller value of pull-up or less current loading from the bus-hold drivers overcomes this issue. To avoid exceeding the MSC7119 output current, the pull-up value should not be too small (a 1 KΩ pull-up resistor is used in the MSC711xADS reference design).

3.4.2 Reset Configuration Pins

Table 34 shows the MSC7119 reset configuration signals. These signals are sampled at the deassertion (rising edge) of $\overline{\text{PORESET}}$. For details, refer to the Reset chapter of the *MSC711x Reference Manual*.

Table 34. Reset Configuration Signals

Signal	Description	Settings
BM[3–0]	Determines boot mode.	See **Table 35** for details.
SWTE	Determines watchdog functionality.	0 Watchdog timer disabled. 1 Watchdog timer enabled.
HDSP	Configures HDI16 strobe polarity.	0 Host Data strobes active low. 1 Host Data strobes active high.
H8BIT	Configures HDI16 operation mode.	0 HDI16 port configured for 16-bit operation. 1 HDI16 port configured for 8-bit operation.

When booting from a power-on reset, the HDI16 is additionally configurable as follows:

- 8- or 16-bit mode as specified by the H8BIT pin.
- Data strobe as specified by the HDSP and HDDS pins.

These pins are sampled only on the deassertion of power-on reset. During a boot from a hard reset, the configuration of these pins is unaffected.

Note: When the HDI16 is used for booting or other purposes, bit 0 is the least significant bit and not the most significant bit as for other DSP products.

3.4.3.2 I^2C Boot

When the MSC7119 device is configured to boot from the I^2C port, the boot program configures the GPIO pins for I^2C operation. Then the MSC7118 device initiates accesses to the I^2C module, downloading data to the MSC7118 device. The I^2C interface is configured as follows:

- PLL is disabled and bypassed so that the I^2C module is clocked with the IPBus clock.
- I^2C interface operates in master mode and polling is used.
- EPROM operates in slave mode.
- Clock divider is set to 128.
- Address of slave during boot is 0xA0.

The IPBus clock is internally divided to generate the bit clock, as follows:

- CLKIN must be a maximum of 100 MHz
- PLL is bypassed.
- IPBus clock = CLKIN/2 is a maximum of 50 MHz.
- I^2C bit clock must be less than or equal to:
  - IPBus clock/I^2C clock divider
  - 50 MHz (max)/128
  - 390.6 KHz

This satisfies the maximum clock rate requirement of 400 kbps for the I^2C interface. For details on the boot procedure, see the "Boot Program" chapter of the *MSC711x Reference Manual*.

3.4.3.3 SPI Boot

When the MSC7119 device is configured to boot from the SPI port, the boot program configures the GPIO pins for SPI operation. Then the MSC7118 device initiates accesses to the SPI module, downloading data to the MSC7118 device. When the SPI routines run in the boot ROM, the MSC7118 is always configured as the SPI master. Booting through the SPI is supported for serial EEPROM devices and serial Flash devices. When a READ_ID instruction is issued to the serial memory device and the device returns a value of 0x00 or 0xFF, the routines for accessing a serial EEPROM are used, at a maximum frequency of 4 Mbps. Otherwise, the routines for accessing a serial Flash are used, and they can run at faster speeds. Booting is performed through one of two sets of pins:

- Main set: BM[2–3], HA3, and HCS2, which allow use of the PLL.
- Alternate set: UTXD, URXD, SDA, and SCL, which cannot be used with the PLL.

In either configuration, an error during SPI boot is flagged on the EVNT3 pin. For details on the boot procedure, see the "Boot Program" chapter of the *MSC711x Reference Manual*.

3.5.3 General Routing

The general routing considerations for the DDR are as follows:

- All DDR signals must be routed next to a solid reference:
  - For data, next to solid ground planes.
  - For address/command, power planes if necessary.
- All DDR signals must be impedance controlled. This is system dependent, but typical values are 50–60 ohm.
- Minimize other cross-talk opportunities. As possible, maintain at least a four times the trace width spacing between all DDR signals to non-DDR signals.
- Keep the number of vias to a minimum to eliminate additional stubs and capacitance.
- Signal group routing priorities are as follows:
  - DDR clocks.
  - Route MVTT/MVREF.
  - Data group.
  - Command/address.
- Minimize data bit jitter by trace matching.

3.5.4 Routing Clock Distribution

The DDR clock distribution considerations are as follows:

- DDR controller supports six clock pairs:
  - 2 DIMM modules.
  - Up to 36 discrete chips.
- For route traces as for any other differential signals:
  - Maintain proper difference pair spacing.
  - Match pair traces within 25 mm.
- Match all clock traces to within 100 mm.
- Keep all clocks equally loaded in the system.
- Route clocks on inner critical layers.

3.5.5 Data Routing

The DDR data routing considerations are as follows:

- Route each data group (8-bits data + DQS + DM) on the same layer. Avoid switching layers within a byte group.
- Take care to match trace lengths, which is extremely important.
- To make trace matching easier, let adjacent groups be routed on alternate critical layers.
- Pin swap bits within a byte group to facilitate routing (discrete case).
- Tight trace matching is recommended within the DDR data group. Keep each 8-bit datum and its DM signal within ± 25 mm of its respective strobe.
- Minimize lengths across the entire DDR channel:
  - Between all groups maintain a delta of no more than 500 mm.
  - Allows greater flexibility in the design for readjustments as needed.
- DDR data group separation:
  - If stack-up allows, keep DDR data groups away from the address and control nets.
  - Route address and control on separate critical layers.
  - If resistor networks (RNs) are used, attempt to keep data and command lines in separate packages.

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