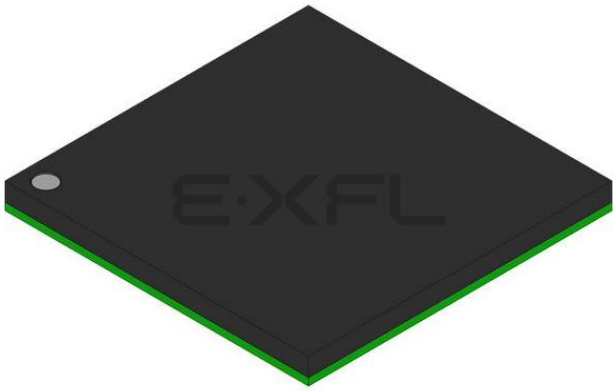

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	150MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-MAPBGA (15x15)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=dsp56311vf150

Signals/Connections 1

The DSP56311 input and output signals are organized into functional groups as shown in **Table 1-1**. **Figure 1-1** diagrams the DSP56311 signals by functional group. The remainder of this chapter describes the signal pins in each functional group.

Table 1-1. DSP56311 Functional Signal Groupings

Functional Group		Number of Signals
Power (V_{CC})		20
Ground (GND)		66
Clock		2
PLL		3
Address bus	Port A[1]	18
Data bus		24
Bus control		13
Interrupt and mode control		5
Host interface (HI08)	Port B[2]	16
Enhanced synchronous serial interface (ESSI)	Ports C and D[3]	12
Serial communication interface (SCI)	Port E[4]	3
Timer		3
OnCE/JTAG Port		6

Notes:
1. Port A signals define the external memory interface port, including the external address bus, data bus, and control signals.
2. Port B signals are the HI08 port signals multiplexed with the GPIO signals.
3. Port C and D signals are the two ESSI port signals multiplexed with the GPIO signals.
4. Port E signals are the SCI port signals multiplexed with the GPIO signals.
5. There are 5 signal connections that are not used. These are designated as no connect (NC) in the package description (see **Chapter 3**).

Note: The Clock Output (CLKOUT), BCLK, $\overline{\text{BCLK}}$, $\overline{\text{CAS}}$, and $\overline{\text{RAS[0–3]}}$ signals used by other DSP56300 family members are supported by the DSP56311 at operating frequencies up to 100 MHz. Therefore, above 100 MHz, you must enable bus arbitration by setting the Asynchronous Bus Arbitration Enable Bit (ABE) in the operating mode register. When set, the ABE bit eliminates the required set-up and hold times for $\overline{\text{BB}}$ and $\overline{\text{BG}}$ with respect to $\overline{\text{CLKOUT}}$. In addition, DRAM access is not supported above 100 MHz.

1.5.2 External Data Bus

Table 1-7. External Data Bus Signals

Signal Name	Type	State During Reset	State During Stop or Wait	Signal Description
D[0–23]	Input/ Output	Ignored Input	Last state: *Input*: Ignored *Output*: Last value	**Data Bus**—When the DSP is the bus master, D[0–23] are active-high, bidirectional input/outputs that provide the bidirectional data bus for external program and data memory accesses. Otherwise, D[0–23] drivers are tri-stated. If the last state is output, these lines have weak keepers to maintain the last output state if all drivers are tri-stated.

1.5.3 External Bus Control

Table 1-8. External Bus Control Signals

Signal Name	Type	State During Reset, Stop, or Wait	Signal Description
AA[0–3]	Output	Tri-stated	**Address Attribute**—When defined as AA, these signals can be used as chip selects or additional address lines. The default use defines a priority scheme under which only one AA signal can be asserted at a time. Setting the AA priority disable (APD) bit (Bit 14) of the Operating Mode Register, the priority mechanism is disabled and the lines can be used together as four external lines that can be decoded externally into 16 chip select signals.
$\overline{\text{RAS}}$[0–3]	Output		**Row Address Strobe**—When defined as $\overline{\text{RAS}}$, these signals can be used as $\overline{\text{RAS}}$ for DRAM interface. These signals are tri-statable outputs with programmable polarity. **Note:** DRAM access is not supported above 100 MHz.
$\overline{\text{RD}}$	Output	Tri-stated	**Read Enable**—When the DSP is the bus master, $\overline{\text{RD}}$ is an active-low output that is asserted to read external memory on the data bus (D[0–23]). Otherwise, $\overline{\text{RD}}$ is tri-stated.
$\overline{\text{WR}}$	Output	Tri-stated	**Write Enable**—When the DSP is the bus master, $\overline{\text{WR}}$ is an active-low output that is asserted to write external memory on the data bus (D[0–23]). Otherwise, the signals are tri-stated.
$\overline{\text{TA}}$	Input	Ignored Input	**Transfer Acknowledge**—If the DSP56311 is the bus master and there is no external bus activity, or the DSP56311 is not the bus master, the $\overline{\text{TA}}$ input is ignored. The $\overline{\text{TA}}$ input is a data transfer acknowledge (DTACK) function that can extend an external bus cycle indefinitely. Any number of wait states (1, 2. . .infinity) can be added to the wait states inserted by the bus control register (BCR) by keeping $\overline{\text{TA}}$ deasserted. In typical operation, $\overline{\text{TA}}$ is deasserted at the start of a bus cycle, asserted to enable completion of the bus cycle, and deasserted before the next bus cycle. The current bus cycle completes one clock period after $\overline{\text{TA}}$ is deasserted. The number of wait states is determined by the $\overline{\text{TA}}$ input or by the BCR, whichever is longer. The BCR sets the minimum number of wait states in external bus cycles. In order to use the $\overline{\text{TA}}$ functionality, the BCR must be programmed to at least one wait state. A zero wait state access cannot be extended by $\overline{\text{TA}}$ deassertion. At operating frequencies ≤100 MHz, $\overline{\text{TA}}$ can operate synchronously (with respect to CLKOUT) or asynchronously depending on the setting of the TAS bit in the Operating Mode Register (OMR). If synchronous mode is selected, the user is responsible for ensuring that $\overline{\text{TA}}$ transitions occur synchronous to CLKOUT to ensure correct operation. Synchronous operation is not supported above 100 MHz and the OMR[TAS] bit must be set to synchronize the $\overline{\text{TA}}$ signal with the internal clock.

Table 1-12. Enhanced Synchronous Serial Interface 0 (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
STD0	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the Serial Transmit Shift Register. STD0 is an output when data is transmitted.
PC5	Input or Output		**Port C 5**—The default configuration following reset is GPIO input PC5. When configured as PC5, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal STD0 through the Port C Control Register.

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

1.9 Enhanced Synchronous Serial Interface 1 (ESSI1)

Table 1-13. Enhanced Serial Synchronous Interface 1

Signal Name	Type	State During Reset[1,2]	Signal Description
SC10	Input or Output	Ignored Input	**Serial Control 0**—For asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For synchronous mode, this signal is used either for transmitter 1 output or for serial I/O flag 0.
PD0	Input or Output		**Port D 0**—The default configuration following reset is GPIO input PD0. When configured as PD0, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC10 through the Port D Control Register.
SC11	Input/Output	Ignored Input	**Serial Control 1**—For asynchronous mode, this signal is the receiver frame sync I/O. For synchronous mode, this signal is used either for Transmitter 2 output or for Serial I/O Flag 1.
PD1	Input or Output		**Port D 1**—The default configuration following reset is GPIO input PD1. When configured as PD1, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC11 through the Port D Control Register.
SC12	Input/Output	Ignored Input	**Serial Control Signal 2**—The frame sync for both the transmitter and receiver in synchronous mode and for the transmitter only in asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
PD2	Input or Output		**Port D 2**—The default configuration following reset is GPIO input PD2. When configured as PD2, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC12 through the Port D Control Register.

Table 1-14. Serial Communication Interface (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
SCLK	Input/Output	Ignored Input	**Serial Clock**—Provides the input or output clock used by the transmitter and/or the receiver.
PE2	Input or Output		**Port E 2**—The default configuration following reset is GPIO input PE2. When configured as PE2, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal SCLK through the Port E Control Register.

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

1.11 Timers

The DSP56311 has three identical and independent timers. Each timer can use internal or external clocking and can either interrupt the DSP56311 after a specified number of events (clocks) or signal an external device after counting a specific number of internal events.

Table 1-15. Triple Timer Signals

Signal Name	Type	State During Reset[1,2]	Signal Description
TIO0	Input or Output	Ignored Input	**Timer 0 Schmitt-Trigger Input/Output**— When Timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When Timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output. The default mode after reset is GPIO input. TIO0 can be changed to output or configured as a timer I/O through the Timer 0 Control/Status Register (TCSR0).
TIO1	Input or Output	Ignored Input	**Timer 1 Schmitt-Trigger Input/Output**— When Timer 1 functions as an external event counter or in measurement mode, TIO1 is used as input. When Timer 1 functions in watchdog, timer, or pulse modulation mode, TIO1 is used as output. The default mode after reset is GPIO input. TIO1 can be changed to output or configured as a timer I/O through the Timer 1 Control/Status Register (TCSR1).
TIO2	Input or Output	Ignored Input	**Timer 2 Schmitt-Trigger Input/Output**— When Timer 2 functions as an external event counter or in measurement mode, TIO2 is used as input. When Timer 2 functions in watchdog, timer, or pulse modulation mode, TIO2 is used as output. The default mode after reset is GPIO input. TIO2 can be changed to output or configured as a timer I/O through the Timer 2 Control/Status Register (TCSR2).

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

2.2 Thermal Characteristics

Table 2-2. Thermal Characteristics

Thermal Resistance Characteristic	Symbol	MAP-BGA Value	Unit
Junction-to-ambient, natural convection, single-layer board (1s)[1,2]	$R_{\theta JA}$	49	°C/W
Junction-to-ambient, natural convection, four-layer board (2s2p)[1,3]	$R_{\theta JMA}$	26	°C/W
Junction-to-ambient, @200 ft/min air flow, single layer board (1s)[1,3]	$R_{\theta JMA}$	39	°C/W
Junction-to-ambient, @200 ft/min air flow, four-layer board (2s2p)[1,3]	$R_{\theta JMA}$	22	°C/W
Junction-to-board[4]	$R_{\theta JB}$	14	°C/W
Junction-to-case thermal resistance[5]	$R_{\theta JC}$	5	°C/W
Junction-to-package-top, natural convection[6]	Ψ_{JT}	2	°C/W
Junction-to-package-top, @200 ft/min air flow[6]	Ψ_{JT}	2	°C/W

Notes:
1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

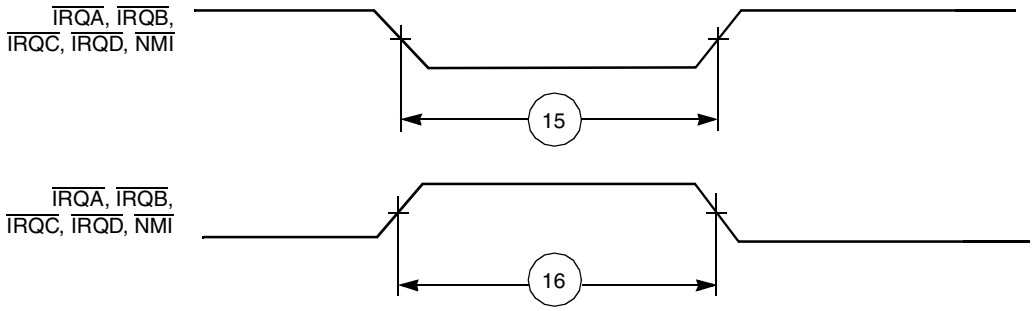


Figure 2-5. External Interrupt Timing (Negative Edge-Triggered)

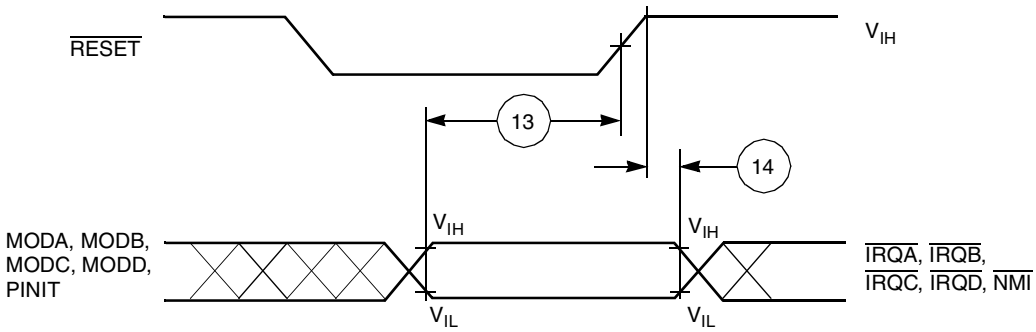


Figure 2-6. Operating Mode Select Timing

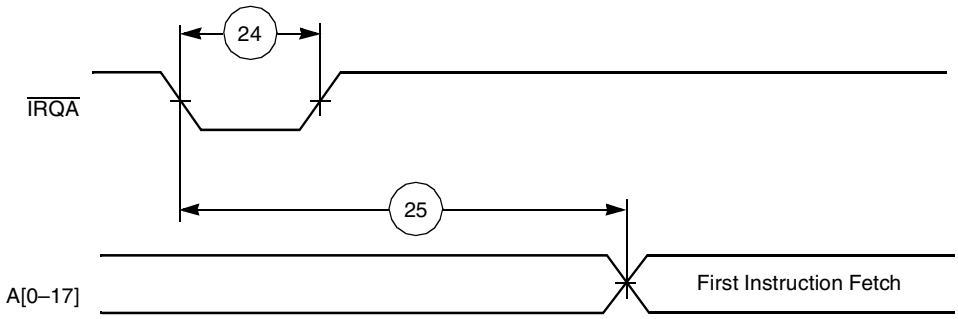


Figure 2-7. Recovery from Stop State Using IRQA

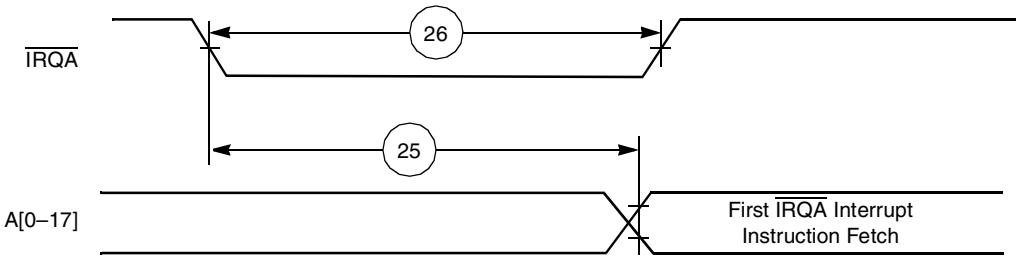
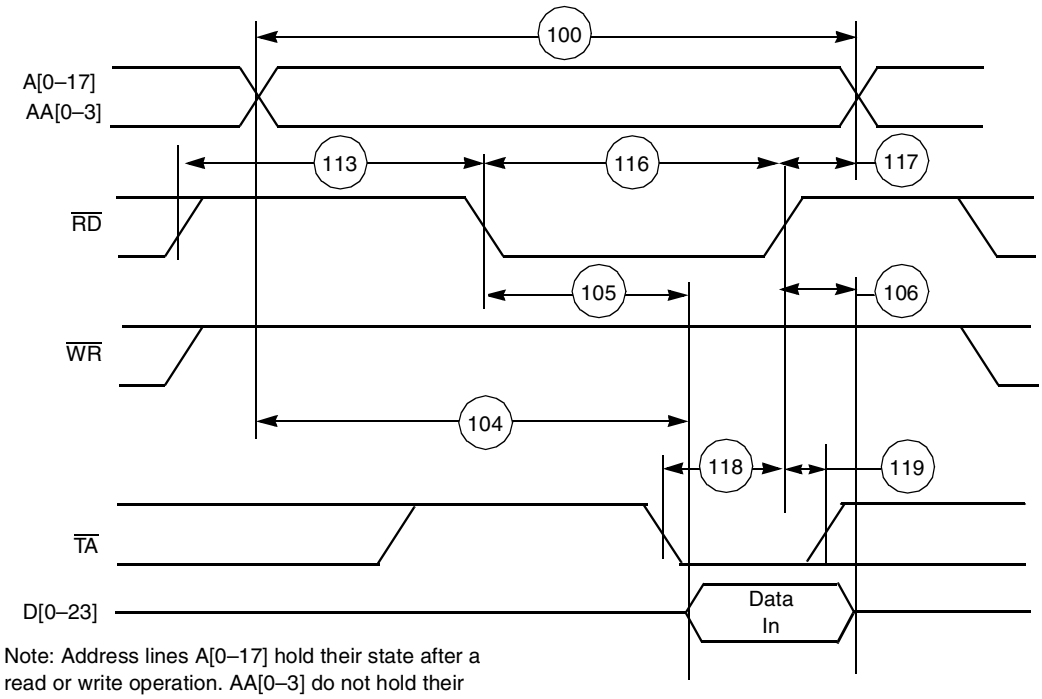
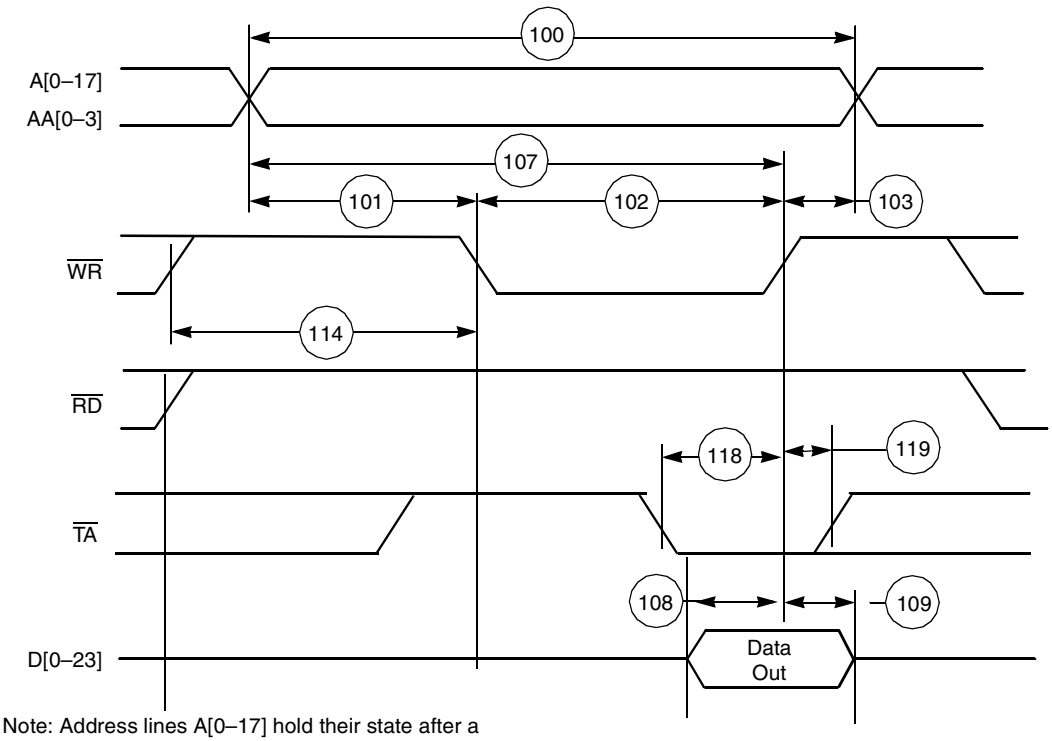


Figure 2-8. Recovery from Stop State Using IRQA Interrupt Service



Note: Address lines A[0–17] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-10. SRAM Read Access



Note: Address lines A[0–17] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-11. SRAM Write Access

Table 2-9. DRAM Page Mode Timings, Three Wait States[1,2,3] (Continued)

No.	Characteristics	Symbol	Expression[4]	100 MHz		Unit
				Min	Max	
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$2.5 \times T_C - 4.0$	21.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$4.5 \times T_C - 4.0$	41.0	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2 \times T_C - 4.0$	16.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ assertion[5] • BRW[1–0] = 00, 01—not applicable • BRW[1–0] = 10 • BRW[1–0] = 11	t_{CRP}	 — $4.75 \times T_C - 6.0$ $6.75 \times T_C - 6.0$	 — 41.5 61.5	 — — —	 — ns ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.5 \times T_C - 4.0$	11.0	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	6.0	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$2.5 \times T_C - 4.0$	21.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$4 \times T_C - 4.0$	36.0	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 4.0$	8.5	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.75 \times T_C - 4.0$	3.5	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$2.25 \times T_C - 4.2$	18.3	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$3.5 \times T_C - 4.5$	30.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$3.75 \times T_C - 4.3$	33.2	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$3.25 \times T_C - 4.3$	28.2	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.5$	0.5	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$2.5 \times T_C - 4.0$	21.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$1.25 \times T_C - 4.3$	8.2	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$3.5 \times T_C - 4.0$	31.0	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$2.5 \times T_C - 5.7$	—	19.3	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 1.5$	6.0	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	ns

Notes:
1. The number of wait states for Page mode access is specified in the DRAM Control Register.
2. The refresh period is specified in the DRAM Control Register.
3. The asynchronous delays specified in the expressions are valid for the DSP56311.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (for example, t_{PC} equals $4 \times T_C$ for read-after-read or write-after-write sequences). An expression is used to compute the number listed as the minimum or maximum value listed, as appropriate.
5. BRW[1–0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of page-access.
6. $\overline{RD}$ deassertion always occurs after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 2-10. DRAM Page Mode Timings, Four Wait States[1,2,3]

No.	Characteristics	Symbol	Expression[4]	100 MHz		Unit
				Min	Max	
131	Page mode cycle time for two consecutive accesses of the same direction Page mode cycle time for mixed (read and write) accesses	 t_{PC}	$5 \times T_C$ $4.5 \times T_C$	50.0 45.0	— —	ns ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$2.75 \times T_C - 5.7$	—	21.8	ns
133	Column address valid to data valid (read)	t_{AA}	$3.75 \times T_C - 5.7$	—	31.8	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$3.5 \times T_C - 4.0$	31.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$6 \times T_C - 4.0$	56.0	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2.5 \times T_C - 4.0$	21.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ assertion[5] • BRW[1–0] = 00, 01—Not applicable • BRW[1–0] = 10 • BRW[1–0] = 11	t_{CRP}	 — $5.25 \times T_C - 6.0$ $7.25 \times T_C - 6.0$	 — 46.5 66.5	 — — —	 — ns ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$2 \times T_C - 4.0$	16.0	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	6.0	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$3.5 \times T_C - 4.0$	31.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$5 \times T_C - 4.0$	46.0	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 4.0$	8.5	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$1.25 \times T_C - 3.7$	8.8	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$3.25 \times T_C - 4.2$	28.3	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$4.5 \times T_C - 4.5$	40.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$4.75 \times T_C - 4.3$	43.2	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$3.75 \times T_C - 4.3$	33.2	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.5$	0.5	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$3.5 \times T_C - 4.0$	31.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$1.25 \times T_C - 4.3$	8.2	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$4.5 \times T_C - 4.0$	41.0	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$3.25 \times T_C - 5.7$	—	26.8	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 1.5$	6.0	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	ns

Notes:
1. The number of wait states for Page mode access is specified in the DRAM Control Register.
2. The refresh period is specified in the DRAM Control Register.
3. The asynchronous delays specified in the expressions are valid for the DSP56311.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (for example, t_{PC} equals $3 \times T_C$ for read-after-read or write-after-write sequences). An expressions is used to calculate the maximum or minimum value listed, as appropriate.
5. BRW[1–0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
6. $\overline{RD}$ deassertion always occurs after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

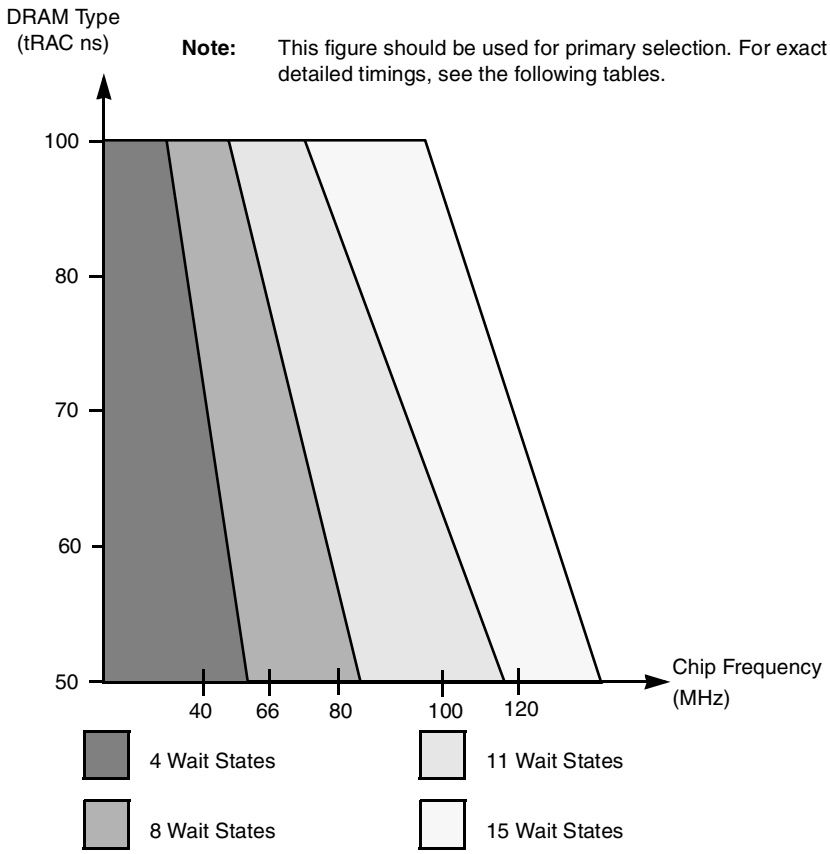


Figure 2-15. DRAM Out-of-Page Wait State Selection Guide

Table 2-11. DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1,2]

No.	Characteristics	Symbol	Expression[3]	100 MHz		Unit
				Min	Max	
157	Random read or write cycle time	t_{RC}	$12 \times T_C$	120.0	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	$6.25 \times T_C - 7.0$	—	55.5	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$3.75 \times T_C - 7.0$	—	30.5	ns
160	Column address valid to data valid (read)	t_{AA}	$4.5 \times T_C - 7.0$	—	38.0	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$4.25 \times T_C - 4.0$	38.5	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$7.75 \times T_C - 4.0$	73.5	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$5.25 \times T_C - 4.0$	48.5	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$6.25 \times T_C - 4.0$	58.5	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$3.75 \times T_C - 4.0$	33.5	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$2.5 \times T_C \pm 4.0$	21.0	29.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$1.75 \times T_C \pm 4.0$	13.5	21.5	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$5.75 \times T_C - 4.0$	53.5	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$4.25 \times T_C - 6.0$	36.5	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$4.25 \times T_C - 4.0$	38.5	—	ns

2.4.5.3 Asynchronous Bus Arbitration Timings

Table 2-13. Asynchronous Bus Timings

No.	Characteristics	Expression	150 MHz		Unit
			Min	Max	
250	$\overline{BB}$ assertion window from $\overline{BG}$ input deassertion.	2.5 × Tc + 5	—	22	ns
251	Delay from $\overline{BB}$ assertion to $\overline{BG}$ assertion	2 × Tc + 5	18.3	—	ns

Notes:
1. Bit 13 in the Operating Mode Register must be set to enable Asynchronous Arbitration mode.
2. At 150 MHz, Asynchronous Arbitration mode is recommended.
3. To guarantee timings 250 and 251, it is recommended that you assert non-overlapping $\overline{BG}$ inputs to different DSP56300 devices (on the same bus), as shown in **Figure 2-19**, where $\overline{BG1}$ is the $\overline{BG}$ signal for one DSP56300 device while $\overline{BG2}$ is the $\overline{BG}$ signal for a second DSP56300 device.

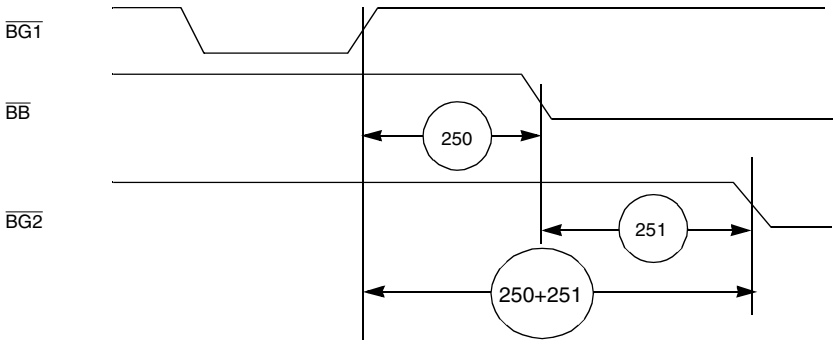


Figure 2-19. Asynchronous Bus Arbitration Timing

The asynchronous bus arbitration is enabled by internal synchronization circuits on $\overline{BG}$ and $\overline{BB}$ inputs. These synchronization circuits add delay from the external signal until it is exposed to internal logic. As a result of this delay, a DSP56300 part may assume mastership and assert $\overline{BB}$, for some time after $\overline{BG}$ is deasserted. This is the reason for timing 250.

Once $\overline{BB}$ is asserted, there is a synchronization delay from $\overline{BB}$ assertion to the time this assertion is exposed to other DSP56300 components that are potential masters on the same bus. If $\overline{BG}$ input is asserted before that time, and $\overline{BG}$ is asserted and $\overline{BB}$ is deasserted, another DSP56300 component may assume mastership at the same time. Therefore, some non-overlap period between one $\overline{BG}$ input active to another $\overline{BG}$ input active is required. Timing 251 ensures that overlaps are avoided.

Table 2-16. ESSI Timings (Continued)

No.	Characteristics[4, 6]	Symbol	Expression	150 MHz		Cond-ition[5]	Unit
				Min	Max		
451	TXC rising edge to FST out (word-length) low			— —	31.0 17.0	x ck i ck	ns
452	TXC rising edge to data out enable from high impedance			— —	31.0 17.0	x ck i ck	ns
453	TXC rising edge to transmitter 0 drive enable assertion			— —	34.0 20.0	x ck i ck	ns
454	TXC rising edge to data out valid		$35 + 0.5 \times T_C$	— —	38.4 21.0	x ck i ck	ns
455	TXC rising edge to data out high impedance[3]			— —	31.0 16.0	x ck i ck	ns
456	TXC rising edge to transmitter 0 drive enable deassertion[3]			— —	34.0 20.0	x ck i ck	ns
457	FST input (bl, wr)[6] set-up time before TXC falling edge[2]			2.0 21.0	— —	x ck i ck	ns
458	FST input (wl)[6] to data out enable from high impedance			—	27.0	—	ns
459	FST input (wl) to transmitter 0 drive enable assertion			—	31.0	—	ns
460	FST input (wl)[6] set-up time before TXC falling edge			2.5 21.0	— —	x ck i ck	ns
461	FST input hold time after TXC falling edge			4.0 0.0	— —	x ck i ck	ns
462	Flag output valid after TXC rising edge			— —	32.0 18.0	x ck i ck	ns

Notes:
1. For the internal clock, the external clock cycle is defined by the instruction cycle time (timing 7 in **Table 2-5** on page 2-6) and the ESSI Control Register.
2. The word-length-relative frame sync signal waveform operates the same way as the bit-length frame sync signal waveform, but spreads from one serial clock before the first bit clock (same as the Bit Length Frame Sync signal) until the one before last bit clock of the first word in the frame.
3. Periodically sampled and not 100 percent tested
4. V_{CCQH} = 3.3 V ± 0.3 V, V_{CC} = 1.8 V ± 0.1 V; T_J = –40°C to +100 °C, C_L = 50 pF.
5. TXC (SCK Pin) = transmit clock
   RXC (SC0 or SCK pin) = receive clock
   FST (SC2 pin) = transmit frame sync
   FSR (SC1 or SC2 pin) receive frame sync
6. i ck = Internal Clock; x ck = external clock
   i ck a = internal clock, Asynchronous mode (asynchronous implies that TXC and RXC are two different clocks)
   i ck s = internal clock, Synchronous mode (synchronous implies that TXC and RXC are the same clock)
   bl = bit length
   wl = word length
   wr = word length relative

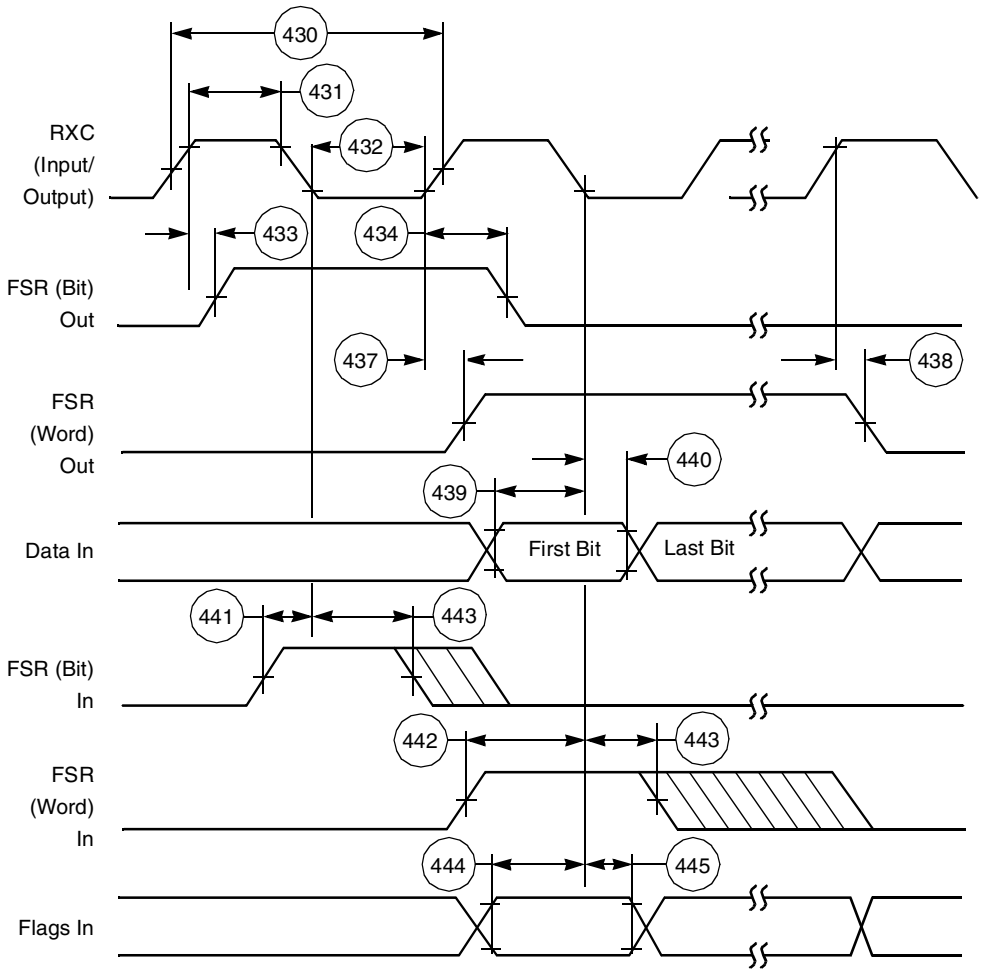


Figure 2-32. ESSI Receiver Timing

2.4.9 Timer Timing

Table 2-17. Timer Timing

No.	Characteristics	Expression	150 MHz		Unit
			Min	Max	
480	TIO Low	$2 \times T_C + 2.0$	15.4	—	ns
481	TIO High	$2 \times T_C + 2.0$	15.4	—	ns
Note:	V_{CCQH} = 3.3 V ± 0.3 V, V_{CC} = 1.8 V ± 0.1 V; T_J = –40°C to +100 °C, C_L = 50 pF				

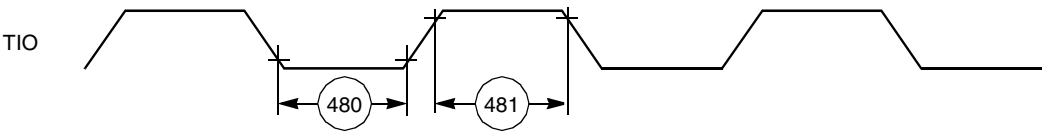


Figure 2-33. TIO Timer Event Input Restrictions

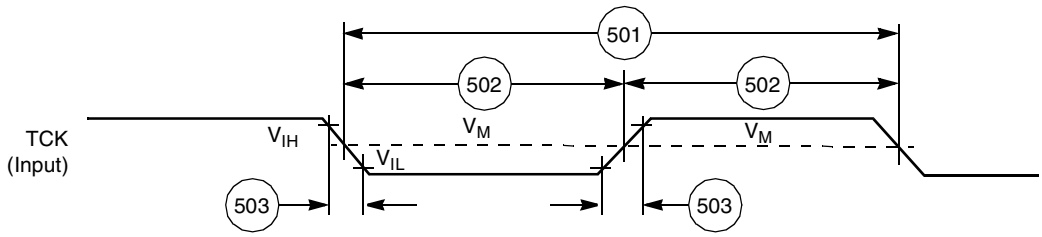


Figure 2-35. Test Clock Input Timing Diagram

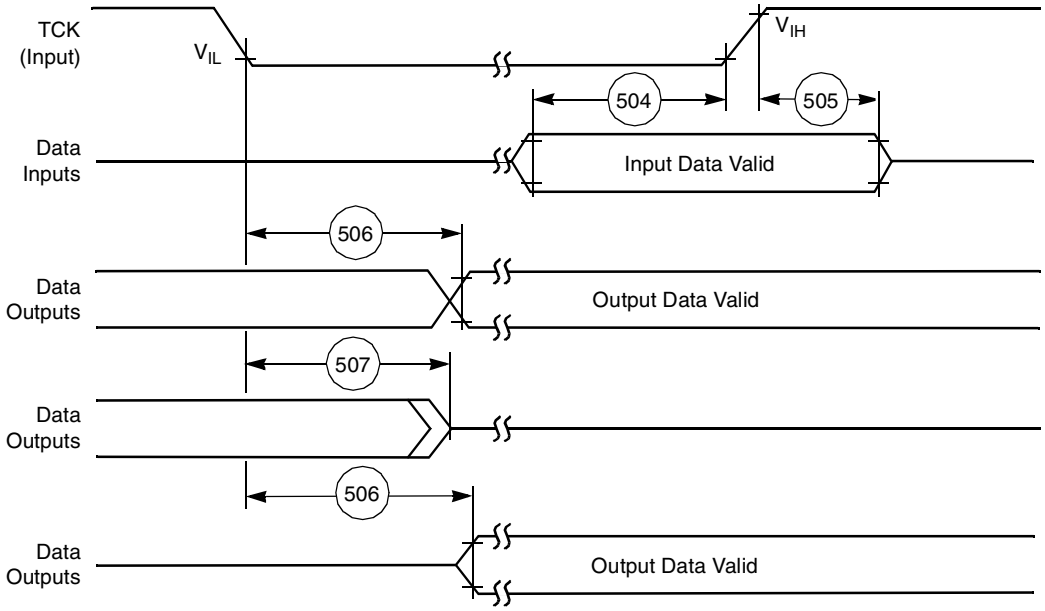


Figure 2-36. Boundary Scan (JTAG) Timing Diagram

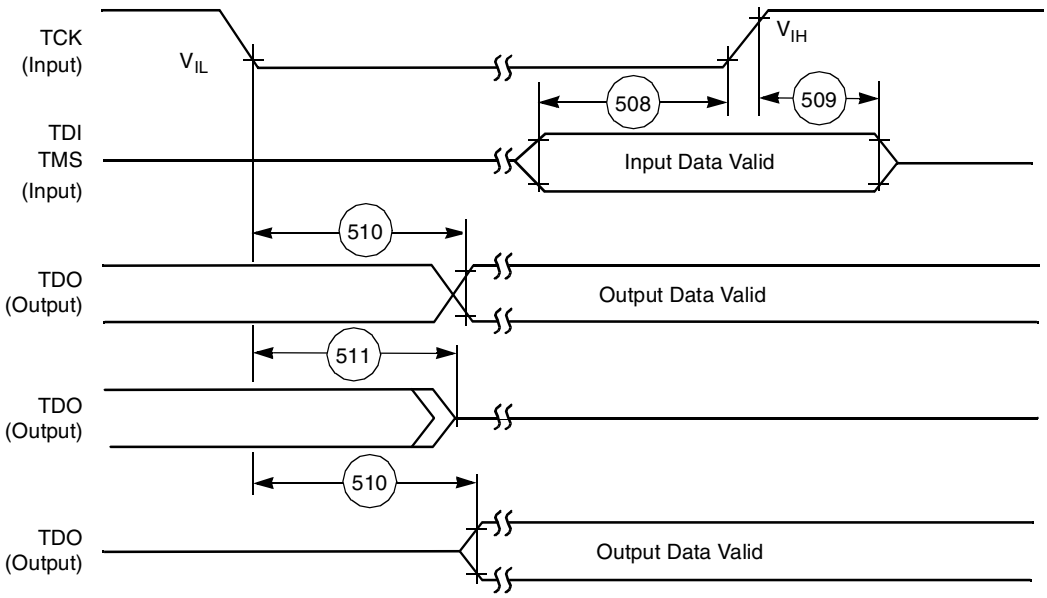


Figure 2-37. Test Access Port Timing Diagram

Equation 4: $I = 50 \times 10^{-12} \times 3.3 \times 33 \times 10^{6} = 5.48\ mA$

The maximum internal current (I_{CCI}max) value reflects the typical possible switching of the internal buses on best-case operation conditions—not necessarily a real application case. The typical internal current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions. Perform the following steps for applications that require very low current consumption:

1. Set the EBD bit when you are not accessing external memory.
2. Minimize external memory accesses, and use internal memory accesses.
3. Minimize the number of pins that are switching.
4. Minimize the capacitive load on the pins.
5. Connect the unused inputs to pull-up or pull-down resistors.
6. Disable unused peripherals.
7. Disable unused pin activity (for example, CLKOUT, XTAL).

One way to evaluate power consumption is to use a current-per-MIPS measurement methodology to minimize specific board effects (that is, to compensate for measured board current not caused by the DSP). A benchmark power consumption test algorithm is listed in **Appendix A**. Use the test algorithm, specific test current measurements, and the following equation to derive the current-per-MIPS value.

Equation 5: $\text{MIPS} = I / \text{MHz} = (I_{typF2} - I_{typF1}) / (F2 - F1)$

Where:

I_{typF2}	=	current at F2
I_{typF1}	=	current at F1
F2	=	high frequency (any specified operating frequency)
F1	=	low frequency (any specified operating frequency lower than F2)

Note: F1 should be significantly less than F2. For example, F2 could be 66 MHz and F1 could be 33 MHz. The degree of difference between F1 and F2 determines the amount of precision with which the current rating can be determined for an application.

4.4 PLL Performance Issues

The following explanations should be considered as general observations on expected PLL behavior. There is no test that replicates these exact numbers. These observations were measured on a limited number of parts and were not verified over the entire temperature and voltage ranges.

4.4.1 Phase Skew Performance

The phase skew of the PLL is defined as the time difference between the falling edges of EXTAL and CLKOUT for a given capacitive load on CLKOUT, over the entire process, temperature and voltage ranges. As defined in **Figure 2-2**, *External Clock Timing*, on page 2-5 for input frequencies greater than 15 MHz and the MF ≤4, this skew is greater than or equal to 0.0 ns and less than 1.8 ns; otherwise, this skew is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this skew is between −1.4 ns and +3.2 ns.

```
        dc      $A43E00
        dc      $C2B639
        dc      $85A47E
        dc      $ABFDDF
        dc      $F3A2C
        dc      $2D7CF5
        dc      $E16A8A
        dc      $ECB8FB
        dc      $4BED18
        dc      $43F371
        dc      $83A556
        dc      $E1E9D7
        dc      $ACA2C4
        dc      $8135AD
        dc      $2CE0E2
        dc      $8F2C73
        dc      $432730
        dc      $A87FA9
        dc      $4A292E
        dc      $A63CCF
        dc      $6BA65C
        dc      $E06D65
        dc      $1AA3A
        dc      $A1B6EB
        dc      $48AC48
        dc      $EF7AE1
        dc      $6E3006
        dc      $62F6C7
        dc      $6064F4
        dc      $87E41D
        dc      $CB2692
        dc      $2C3863
        dc      $C6BC60
        dc      $43A519
        dc      $6139DE
        dc      $ADF7BF
        dc      $4B3E8C
        dc      $6079D5
        dc      $E0F5EA
        dc      $8230DB
        dc      $A3B778
        dc      $2BFE51
        dc      $E0A6B6
        dc      $68FFB7
        dc      $28F324
        dc      $8F2E8D
        dc      $667842
        dc      $83E053
        dc      $A1FD90
        dc      $6B2689
        dc      $85B68E
        dc      $622EAF
        dc      $6162BC
        dc      $E4A245
YDAT_END

;************************************************************************
;
;     EQUATES for DSP56311 I/O registers and ports
;
;     Last update: June 11 1995
;
;************************************************************************
```

```
M_HREN EQU $4                          ; Host Request Enable
M_HAEN EQU $5                          ; Host Acknowledge Enable
M_HEN EQU $6                           ; Host Enable
M_HOD EQU $8                           ; Host Request Open Drain mode
M_HDSP EQU $9                          ; Host Data Strobe Polarity
M_HASP EQU $A                          ; Host Address Strobe Polarity
M_HMUX EQU $B                          ; Host Multiplexed bus select
M_HD_HS EQU $C                         ; Host Double/Single Strobe select
M_HCSP EQU $D                          ; Host Chip Select Polarity
M_HRP EQU $E                           ; Host Request Polarity
M_HAP EQU $F                           ; Host Acknowledge Polarity


;------------------------------------------------------------------------
;
;       EQUATES for Serial Communications Interface (SCI)
;
;------------------------------------------------------------------------

;       Register Addresses

M_STXH EQU $FFFF97                     ; SCI Transmit Data Register (high)
M_STXM EQU $FFFF96                     ; SCI Transmit Data Register (middle)
M_STXL EQU $FFFF95                     ; SCI Transmit Data Register (low)
M_SRXH EQU $FFFF9A                     ; SCI Receive Data Register (high)
M_SRXM EQU $FFFF99                     ; SCI Receive Data Register (middle)
M_SRXL EQU $FFFF98                     ; SCI Receive Data Register (low)
M_STXA EQU $FFFF94                     ; SCI Transmit Address Register
M_SCR EQU $FFFF9C                      ; SCI Control Register
M_SSR EQU $FFFF93                      ; SCI Status Register
M_SCCR EQU $FFFF9B                     ; SCI Clock Control Register

;       SCI Control Register Bit Flags

M_WDS EQU $7                           ; Word Select Mask (WDS0-WDS3)
M_WDS0 EQU 0                           ; Word Select 0
M_WDS1 EQU 1                           ; Word Select 1
M_WDS2 EQU 2                           ; Word Select 2
M_SSFTD EQU 3                          ; SCI Shift Direction
M_SBK EQU 4                            ; Send Break
M_WAKE EQU 5                           ; Wakeup Mode Select
M_RWU EQU 6                            ; Receiver Wakeup Enable
M_WOMS EQU 7                           ; Wired-OR Mode Select
M_SCRE EQU 8                           ; SCI Receiver Enable
M_SCTE EQU 9                           ; SCI Transmitter Enable
M_ILIE EQU 10                          ; Idle Line Interrupt Enable
M_SCRIE EQU 11                         ; SCI Receive Interrupt Enable
M_SCTIE EQU 12                         ; SCI Transmit Interrupt Enable
M_TMIE EQU 13                          ; Timer Interrupt Enable
M_TIR EQU 14                           ; Timer Interrupt Rate
M_SCKP EQU 15                          ; SCI Clock Polarity
M_REIE EQU 16                          ; SCI Error Interrupt Enable (REIE)

;       SCI Status Register Bit Flags

M_TRNE EQU 0                           ; Transmitter Empty
M_TDRE EQU 1                           ; Transmit Data Register Empty
M_RDRF EQU 2                           ; Receive Data Register Full
M_IDLE EQU 3                           ; Idle Line Flag
M_OR EQU 4                             ; Overrun Error Flag
M_PE EQU 5                             ; Parity Error
M_FE EQU 6                             ; Framing Error Flag
M_R8 EQU 7                             ; Received Bit 8 (R8) Address
```

```
;       SCI Clock Control Register

M_CD EQU $FFF                          ; Clock Divider Mask (CD0-CD11)
M_COD EQU 12                           ; Clock Out Divider
M_SCP EQU 13                           ; Clock Prescaler
M_RCM EQU 14                           ; Receive Clock Mode Source Bit
M_TCM EQU 15                           ; Transmit Clock Source Bit

;------------------------------------------------------------------------
;
;       EQUATES for Synchronous Serial Interface (SSI)
;
;------------------------------------------------------------------------

;
;       Register Addresses Of SSI0
M_TX00 EQU $FFFFBC                     ; SSI0 Transmit Data Register 0
M_TX01 EQU $FFFFBB                     ; SSIO Transmit Data Register 1
M_TX02 EQU $FFFFBA                     ; SSIO Transmit Data Register 2
M_TSR0 EQU $FFFFB9                     ; SSI0 Time Slot Register
M_RX0 EQU $FFFFB8                      ; SSI0 Receive Data Register
M_SSISR0 EQU $FFFFB7                   ; SSI0 Status Register
M_CRB0 EQU $FFFFB6                     ; SSI0 Control Register B
M_CRA0 EQU $FFFFB5                     ; SSI0 Control Register A
M_TSMA0 EQU $FFFFB4                    ; SSI0 Transmit Slot Mask Register A
M_TSMB0 EQU $FFFFB3                    ; SSI0 Transmit Slot Mask Register B
M_RSMA0 EQU $FFFFB2                    ; SSI0 Receive Slot Mask Register A
M_RSMB0 EQU $FFFFB1                    ; SSI0 Receive Slot Mask Register B

;       Register Addresses Of SSI1
M_TX10 EQU $FFFFAC                     ; SSI1 Transmit Data Register 0
M_TX11 EQU $FFFFAB                     ; SSI1 Transmit Data Register 1
M_TX12 EQU $FFFFAA                     ; SSI1 Transmit Data Register 2
M_TSR1 EQU $FFFFA9                     ; SSI1 Time Slot Register
M_RX1 EQU $FFFFA8                      ; SSI1 Receive Data Register
M_SSISR1 EQU $FFFFA7                   ; SSI1 Status Register
M_CRB1 EQU $FFFFA6                     ; SSI1 Control Register B
M_CRA1 EQU $FFFFA5                     ; SSI1 Control Register A
M_TSMA1 EQU $FFFFA4                    ; SSI1 Transmit Slot Mask Register A
M_TSMB1 EQU $FFFFA3                    ; SSI1 Transmit Slot Mask Register B
M_RSMA1 EQU $FFFFA2                    ; SSI1 Receive Slot Mask Register A
M_RSMB1 EQU $FFFFA1                    ; SSI1 Receive Slot Mask Register B

;       SSI Control Register A Bit Flags

M_PM EQU $FF                           ; Prescale Modulus Select Mask (PM0-PM7)
M_PSR EQU 11                           ; Prescaler Range
M_DC EQU $1F000                        ; Frame Rate Divider Control Mask (DC0-DC7)
M_ALC EQU 18                           ; Alignment Control (ALC)
M_WL EQU $380000                       ; Word Length Control Mask (WL0-WL7)
M_SSC1 EQU 22                          ; Select SC1 as TR #0 drive enable (SSC1)

;       SSI Control Register B Bit Flags

M_OF EQU $3                            ; Serial Output Flag Mask
M_OF0 EQU 0                            ; Serial Output Flag 0
M_OF1 EQU 1                            ; Serial Output Flag 1
M_SCD EQU $1C                          ; Serial Control Direction Mask
M_SCD0 EQU 2                           ; Serial Control 0 Direction
M_SCD1 EQU 3                           ; Serial Control 1 Direction
M_SCD2 EQU 4                           ; Serial Control 2 Direction
M_SCKD EQU 5                           ; Clock Source Direction
```

```
M_SHFD EQU 6                          ; Shift Direction
M_FSL EQU $180                        ; Frame Sync Length Mask (FSL0-FSL1)
M_FSL0 EQU 7                          ; Frame Sync Length 0
M_FSL1 EQU 8                          ; Frame Sync Length 1
M_FSR EQU 9                           ; Frame Sync Relative Timing
M_FSP EQU 10                          ; Frame Sync Polarity
M_CKP EQU 11                          ; Clock Polarity
M_SYN EQU 12                          ; Sync/Async Control
M_MOD EQU 13                          ; SSI Mode Select
M_SSTE EQU $1C000                     ; SSI Transmit enable Mask
M_SSTE2 EQU 14                        ; SSI Transmit #2 Enable
M_SSTE1 EQU 15                        ; SSI Transmit #1 Enable
M_SSTE0 EQU 16                        ; SSI Transmit #0 Enable
M_SSRE EQU 17                         ; SSI Receive Enable
M_SSTIE EQU 18                        ; SSI Transmit Interrupt Enable
M_SSRIE EQU 19                        ; SSI Receive Interrupt Enable
M_STLIE EQU 20                        ; SSI Transmit Last Slot Interrupt Enable
M_SRLIE EQU 21                        ; SSI Receive Last Slot Interrupt Enable
M_STEIE EQU 22                        ; SSI Transmit Error Interrupt Enable
M_SREIE EQU 23                        ; SI Receive Error Interrupt Enable

;       SSI Status Register Bit Flags

M_IF EQU $3                           ; Serial Input Flag Mask
M_IF0 EQU 0                           ; Serial Input Flag 0
M_IF1 EQU 1                           ; Serial Input Flag 1
M_TFS EQU 2                           ; Transmit Frame Sync Flag
M_RFS EQU 3                           ; Receive Frame Sync Flag
M_TUE EQU 4                           ; Transmitter Underrun Error FLag
M_ROE EQU 5                           ; Receiver Overrun Error Flag
M_TDE EQU 6                           ; Transmit Data Register Empty
M_RDF EQU 7                           ; Receive Data Register Full

;       SSI Transmit Slot Mask Register A

M_SSTSA EQU $FFFF                     ; SSI Transmit Slot Bits Mask A (TS0-TS15)

;       SSI Transmit Slot Mask Register B

M_SSTSB EQU $FFFF                     ; SSI Transmit Slot Bits Mask B (TS16-TS31)

;       SSI Receive Slot Mask Register A

M_SSRSA EQU $FFFF                     ; SSI Receive Slot Bits Mask A (RS0-RS15)

;       SSI Receive Slot Mask Register B

M_SSRSB EQU $FFFF                     ; SSI Receive Slot Bits Mask B (RS16-RS31)



;------------------------------------------------------------------------
;
;       EQUATES for Exception Processing
;
;------------------------------------------------------------------------


;       Register Addresses

M_IPRC EQU $FFFFFF                    ; Interrupt Priority Register Core
M_IPRP EQU $FFFFFE                    ; Interrupt Priority Register Peripheral
```

```
I_VEC EQU $0
       endif

;------------------------------------------------------------------------
; Non-Maskable interrupts
;------------------------------------------------------------------------
I_RESET EQU I_VEC+$00               ; Hardware RESET
I_STACK EQU I_VEC+$02               ; Stack Error
I_ILL EQU I_VEC+$04                 ; Illegal Instruction
I_DBG EQU I_VEC+$06                 ; Debug Request
I_TRAP EQU I_VEC+$08                ; Trap
I_NMI EQU I_VEC+$0A                 ; Non Maskable Interrupt

;------------------------------------------------------------------------
; Interrupt Request Pins
;------------------------------------------------------------------------
I_IRQA EQU I_VEC+$10                ; IRQA
I_IRQB EQU I_VEC+$12                ; IRQB
I_IRQC EQU I_VEC+$14                ; IRQC
I_IRQD EQU I_VEC+$16                ; IRQD

;------------------------------------------------------------------------
; DMA Interrupts
;------------------------------------------------------------------------
I_DMA0 EQU I_VEC+$18                ; DMA Channel 0
I_DMA1 EQU I_VEC+$1A                ; DMA Channel 1
I_DMA2 EQU I_VEC+$1C                ; DMA Channel 2
I_DMA3 EQU I_VEC+$1E                ; DMA Channel 3
I_DMA4 EQU I_VEC+$20                ; DMA Channel 4
I_DMA5 EQU I_VEC+$22                ; DMA Channel 5

;------------------------------------------------------------------------
; Timer Interrupts
;------------------------------------------------------------------------
I_TIM0C EQU I_VEC+$24               ; TIMER 0 compare
I_TIM0OF EQU I_VEC+$26              ; TIMER 0 overflow
I_TIM1C EQU I_VEC+$28               ; TIMER 1 compare
I_TIM1OF EQU I_VEC+$2A              ; TIMER 1 overflow
I_TIM2C EQU I_VEC+$2C               ; TIMER 2 compare
I_TIM2OF EQU I_VEC+$2E              ; TIMER 2 overflow

;------------------------------------------------------------------------
; ESSI Interrupts
;------------------------------------------------------------------------
I_SI0RD EQU I_VEC+$30               ; ESSI0 Receive Data
I_SI0RDE EQU I_VEC+$32              ; ESSI0 Receive Data w/ exception Status
I_SI0RLS EQU I_VEC+$34              ; ESSI0 Receive last slot
I_SI0TD EQU I_VEC+$36               ; ESSI0 Transmit data
I_SI0TDE EQU I_VEC+$38              ; ESSI0 Transmit Data w/ exception Status
I_SI0TLS EQU I_VEC+$3A              ; ESSI0 Transmit last slot
I_SI1RD EQU I_VEC+$40               ; ESSI1 Receive Data
I_SI1RDE EQU I_VEC+$42              ; ESSI1 Receive Data w/ exception Status
I_SI1RLS EQU I_VEC+$44              ; ESSI1 Receive last slot
I_SI1TD EQU I_VEC+$46               ; ESSI1 Transmit data
I_SI1TDE EQU I_VEC+$48              ; ESSI1 Transmit Data w/ exception Status
I_SI1TLS EQU I_VEC+$4A              ; ESSI1 Transmit last slot

;------------------------------------------------------------------------
; SCI Interrupts
;------------------------------------------------------------------------
I_SCIRD EQU I_VEC+$50               ; SCI Receive Data
I_SCIRDE EQU I_VEC+$52              ; SCI Receive Data With Exception Status
I_SCITD EQU I_VEC+$54               ; SCI Transmit Data
```