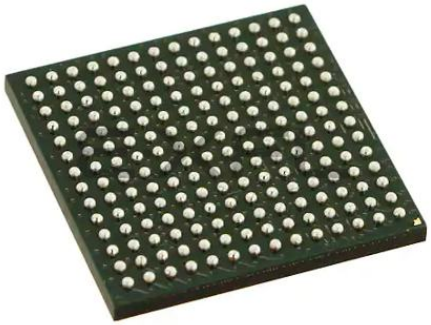

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	150MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56311vf150b1

Table 1. DSP56311 Features (Continued)

Feature	Description
External Memory Expansion	• Data memory expansion to two 256 K × 24-bit word memory spaces using the standard external address lines • Program memory expansion to one 256 K × 24-bit words memory space using the standard external address lines • External memory expansion port • Chip select logic for glueless interface to static random access memory (SRAMs) • Internal DRAM controller for glueless interface to dynamic random access memory (DRAMs) up to 100 MHz operating frequency
Power Dissipation	• Very low-power CMOS design • Wait and Stop low-power standby modes • Fully static design specified to operate down to 0 Hz (dc) • Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)
Packaging	• Molded array plastic-ball grid array (MAP-BGA) package in lead-free or lead-bearing versions.

Target Applications

DSP56311 applications require high performance, low power, small packaging, and a large amount of internal memory. The EFCOP can accelerate general filtering applications. Examples include:

- Wireless and wireline infrastructure applications
- Multi-channel wireless local loop systems
- DSP resource boards
- High-speed modem banks
- IP telephony

Product Documentation

The documents listed in **Table 2** are required for a complete description of the DSP56311 device and are necessary to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, or a Freescale Semiconductor Literature Distribution Center. For documentation updates, visit the Freescale DSP website. See the contact information on the back cover of this document.

Table 2. DSP56311 Documentation

Name	Description	Order Number
DSP56311 User's Manual	Detailed functional description of the DSP56311 memory configuration, operation, and register programming	DSP56311UM
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM
Application Notes	Documents describing specific applications or optimized device operation including code examples	See the DSP56311 product website

Table 1-12. Enhanced Synchronous Serial Interface 0 (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
STD0	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the Serial Transmit Shift Register. STD0 is an output when data is transmitted.
PC5	Input or Output		**Port C 5**—The default configuration following reset is GPIO input PC5. When configured as PC5, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal STD0 through the Port C Control Register.

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

1.9 Enhanced Synchronous Serial Interface 1 (ESSI1)

Table 1-13. Enhanced Serial Synchronous Interface 1

Signal Name	Type	State During Reset[1,2]	Signal Description
SC10	Input or Output	Ignored Input	**Serial Control 0**—For asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For synchronous mode, this signal is used either for transmitter 1 output or for serial I/O flag 0.
PD0	Input or Output		**Port D 0**—The default configuration following reset is GPIO input PD0. When configured as PD0, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC10 through the Port D Control Register.
SC11	Input/Output	Ignored Input	**Serial Control 1**—For asynchronous mode, this signal is the receiver frame sync I/O. For synchronous mode, this signal is used either for Transmitter 2 output or for Serial I/O Flag 1.
PD1	Input or Output		**Port D 1**—The default configuration following reset is GPIO input PD1. When configured as PD1, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC11 through the Port D Control Register.
SC12	Input/Output	Ignored Input	**Serial Control Signal 2**—The frame sync for both the transmitter and receiver in synchronous mode and for the transmitter only in asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
PD2	Input or Output		**Port D 2**—The default configuration following reset is GPIO input PD2. When configured as PD2, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC12 through the Port D Control Register.

Table 1-13. Enhanced Serial Synchronous Interface 1 (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
SCK1	Input/Output	Ignored Input	**Serial Clock**—Provides the serial bit rate clock for the ESSI. The SCK1 is a clock input or output used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PD3	Input or Output		**Port D 3**—The default configuration following reset is GPIO input PD3. When configured as PD3, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SCK1 through the Port D Control Register.
SRD1	Input	Ignored Input	**Serial Receive Data**—Receives serial data and transfers the data to the ESSI Receive Shift Register. SRD1 is an input when data is being received.
PD4	Input or Output		**Port D 4**—The default configuration following reset is GPIO input PD4. When configured as PD4, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SRD1 through the Port D Control Register.
STD1	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the Serial Transmit Shift Register. STD1 is an output when data is being transmitted.
PD5	Input or Output		**Port D 5**—The default configuration following reset is GPIO input PD5. When configured as PD5, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal STD1 through the Port D Control Register.

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

1.10 Serial Communication Interface (SCI)

The SCI provides a full duplex port for serial communication with other DSPs, microprocessors, or peripherals such as modems.

Table 1-14. Serial Communication Interface

Signal Name	Type	State During Reset[1,2]	Signal Description
RXD	Input	Ignored Input	**Serial Receive Data**—Receives byte-oriented serial data and transfers it to the SCI Receive Shift Register.
PE0	Input or Output		**Port E 0**—The default configuration following reset is GPIO input PE0. When configured as PE0, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal RXD through the Port E Control Register.
TXD	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the SCI Transmit Data Register.
PE1	Input or Output		**Port E 1**—The default configuration following reset is GPIO input PE1. When configured as PE1, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal TXD through the Port E Control Register.

1.12 JTAG and OnCE Interface

The DSP56300 family and in particular the DSP56311 support circuit-board test strategies based on the **IEEE® Std.** 1149.1™ test access port and boundary scan architecture, the industry standard developed under the sponsorship of the Test Technology Committee of IEEE and the JTAG. The OnCE module provides a means to interface nonintrusively with the DSP56300 core and its peripherals so that you can examine registers, memory, or on-chip peripherals. Functions of the OnCE module are provided through the JTAG TAP signals. For programming models, see the chapter on debugging support in the *DSP56300 Family Manual*.

Table 1-16. JTAG/OnCE Interface

Signal Name	Type	State During Reset	Signal Description
TCK	Input	Input	**Test Clock**—A test clock input signal to synchronize the JTAG test logic.
TDI	Input	Input	**Test Data Input**—A test data serial input signal for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor.
TDO	Output	Tri-stated	**Test Data Output**—A test data serial output signal for test instructions and data. TDO is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.
TMS	Input	Input	**Test Mode Select**—Sequences the test controller's state machine. TMS is sampled on the rising edge of TCK and has an internal pull-up resistor.
$\overline{\text{TRST}}$	Input	Input	**Test Reset**—Initializes the test controller asynchronously. $\overline{\text{TRST}}$ has an internal pull-up resistor. $\overline{\text{TRST}}$ must be asserted during and after power-up (see EB610/D for details).
$\overline{\text{DE}}$	Input/ Output	Input	**Debug Event**—As an input, initiates Debug mode from an external command controller, and, as an open-drain output, acknowledges that the chip has entered Debug mode. As an input, $\overline{\text{DE}}$ causes the DSP56300 core to finish executing the current instruction, save the instruction pipeline information, enter Debug mode, and wait for commands to be entered from the debug serial input line. This signal is asserted as an output for three clock cycles when the chip enters Debug mode as a result of a debug request or as a result of meeting a breakpoint condition. The $\overline{\text{DE}}$ has an internal pull-up resistor. This signal is not a standard part of the JTAG TAP controller. The signal connects directly to the OnCE module to initiate debug mode directly or to provide a direct external indication that the chip has entered Debug mode. All other interface with the OnCE module must occur through the JTAG port.

Specifications 2

The DSP56311 is fabricated in high-density CMOS with transistor-transistor logic (TTL) compatible inputs and outputs.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}).

In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device that has a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2-1. Absolute Maximum Ratings

Rating[1]	Symbol	Value[1, 2]	Unit
Supply Voltage	V_{CC}	–0.1 to 2.0	V
Input/Output Supply Voltage	V_{CCQH}	–0.3 to 4.0	V
All input voltages	V_{IN}	GND – 0.3 to V_{CCQH} + 0.3	V
Current drain per pin excluding V_{CC} and GND	I	10	mA
Operating temperature range	T_J	–40 to +100	°C
Storage temperature	T_{STG}	–55 to +150	°C

Notes:
1. GND = 0 V, V_{CC} = 1.8 V ± 0.1 V, V_{CCQH} = 3.3 V ± 0.3 V, T_J = –40°C to +100°C, CL = 50 pF
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.
3. Power-up sequence: During power-up, and throughout the DSP56311 operation, V_{CCQH} voltage must always be higher or equal to V_{CC} voltage.

2.3 DC Electrical Characteristics

Table 2-3. DC Electrical Characteristics[7]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage: • Core (V_{CCQL}) and PLL (V_{CCP}) • I/O (V_{CCQH}, V_{CCA}, V_{CCD}, V_{CCC}, V_{CCH}, and V_{CCS})		 1.7 3.0	 1.8 3.3	 1.9 3.6	 V V
Input high voltage • D[0–23], $\overline{BG}$, $\overline{BB}$, $\overline{TA}$ • MOD/$\overline{IRQ}$[1], $\overline{RESET}$, PINIT/$\overline{NMI}$ and all JTAG/ESSI/SCI/Timer/HI08 pins • EXTAL[8]	 V_{IH} V_{IHP} V_{IHX}	 2.0 2.0 0.8 × V_{CCQH}	 — — —	 V_{CCQH} + 0.3 V_{CCQH} + 0.3 V_{CCQH}	 V V V
Input low voltage • D[0–23], $\overline{BG}$, $\overline{BB}$, $\overline{TA}$, MOD/$\overline{IRQ}$[1], $\overline{RESET}$, PINIT • All JTAG/ESSI/SCI/Timer/HI08 pins • EXTAL[8]	 V_{IL} V_{ILP} V_{ILX}	 –0.3 –0.3 –0.3	 — — —	 0.8 0.8 0.2 × V_{CCQH}	 V V V
Input leakage current	I_{IN}	–10	—	10	µA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	µA
Output high voltage • TTL (I_{OH} = –0.4 mA)[5,7] • CMOS (I_{OH} = –10 µA)[5]	V_{OH}	 2.4 V_{CC} – 0.01	 — —	 — —	 V V
Output low voltage • TTL (I_{OL} = 3.0 mA, open-drain pins I_{OL} = 6.7 mA)[5,7] • CMOS (I_{OL} = 10 µA)[5]	V_{OL}	 — —	 — —	 0.4 0.01	 V V
Internal supply current[2]: • In Normal mode • In Wait mode[3] • In Stop mode[4]	 I_{CCI} I_{CCW} I_{CCS}	 — — —	 150 7. 5 100	 — — —	 mA mA µA
PLL supply current		—	1	2.5	mA
Input capacitance[5]	C_{IN}	—	—	10	pF

Notes:
1. Refers to MODA/$\overline{IRQA}$, MODB/$\overline{IRQB}$, MODC/$\overline{IRQC}$, and MODD/$\overline{IRQD}$ pins.
2. **Section 4.3** provides a formula to compute the estimated current requirements in Normal mode. To obtain these results, all inputs must be terminated (that is, not allowed to float). Measurements are based on synthetic intensive DSP benchmarks (see *Appendix A*). The power consumption numbers in this specification are 90 percent of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CCQP} = 3.3 V, V_{CC} = 1.8 V at T_J = 100°C.
3. To obtain these results, all inputs must be terminated (that is, not allowed to float). PLL and XTAL signals are disabled during Stop state.
4. DC current in Stop mode is evaluated based on measurements. To obtain these results, all inputs not disconnected at Stop mode must be terminated (that is, not allowed to float).
5. Periodically sampled and not 100 percent tested.
6. V_{CCQH} = 3.3 V ±0.3 V, V_{CC} = 1.8 V ±0.1 V; T_J = –40°C to +100 °C, C_L = 50 pF
7. This characteristic does not apply to XTAL and PCAP.
8. Driving EXTAL to the low V_{IHX} or the high V_{ILX} value may cause additional power consumption (DC current). To minimize power consumption, the minimum V_{IHX} should be no lower than 0.9 × V_{CCQH} and the maximum V_{ILX} should be no higher than 0.1 × V_{CCQH}.

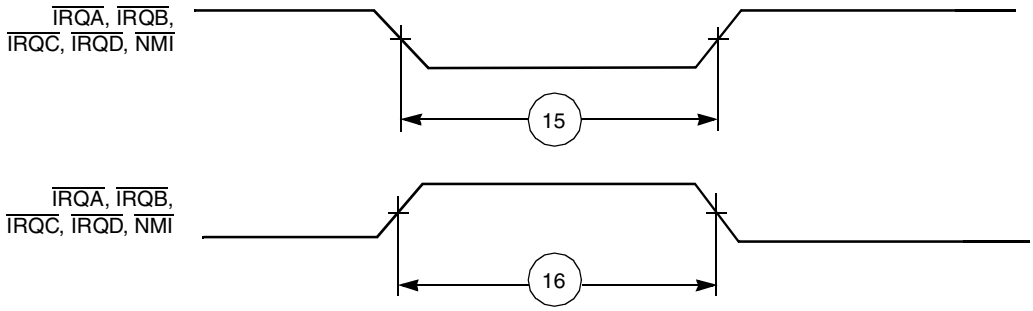


Figure 2-5. External Interrupt Timing (Negative Edge-Triggered)

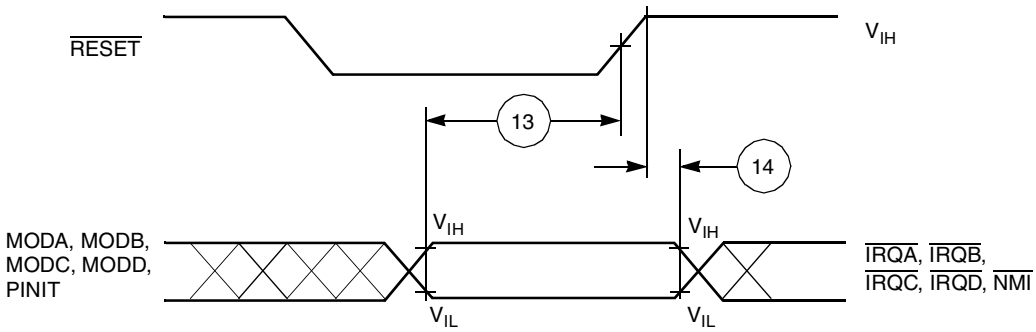


Figure 2-6. Operating Mode Select Timing

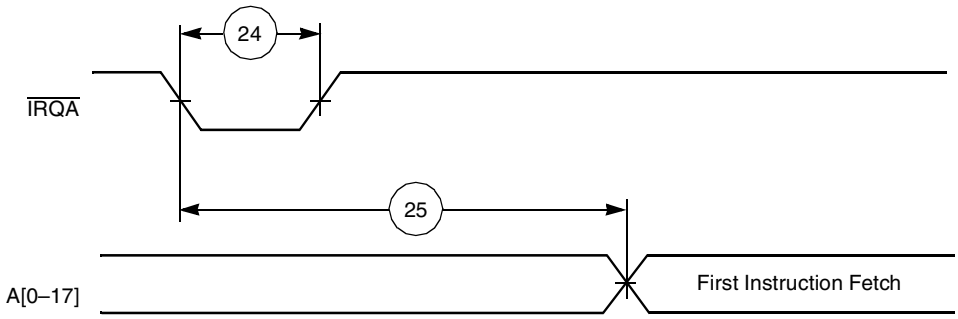


Figure 2-7. Recovery from Stop State Using IRQA

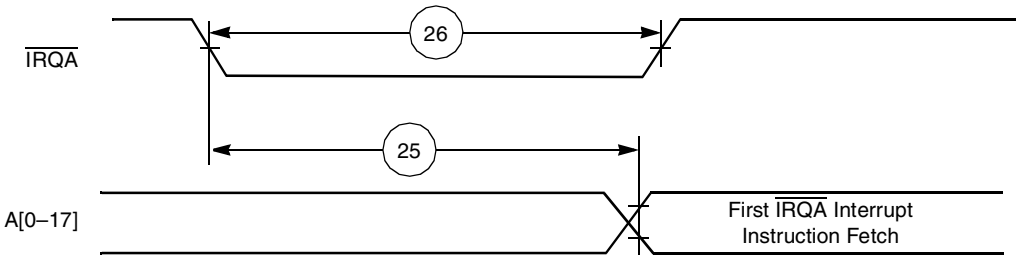


Figure 2-8. Recovery from Stop State Using IRQA Interrupt Service

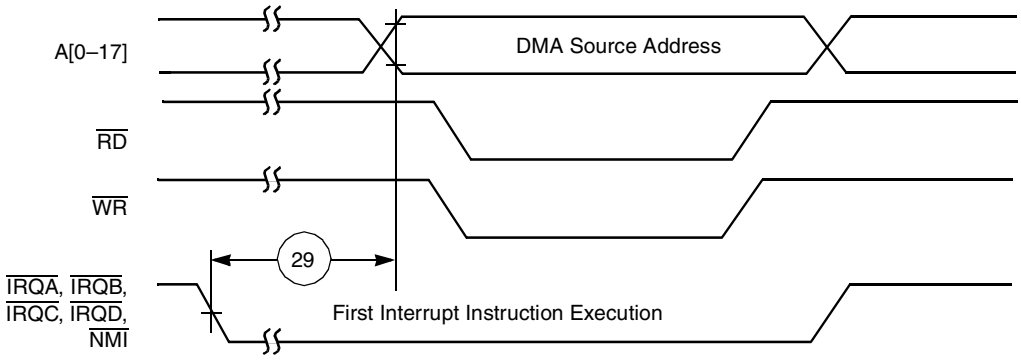


Figure 2-9. External Memory Access (DMA Source) Timing

2.4.5 External Memory Expansion Port (Port A)

2.4.5.1 SRAM Timing

Table 2-8. SRAM Timing

No.	Characteristics	Symbol	Expression[1]	150 MHz		Unit
				Min	Max	
100	Address valid and AA assertion pulse width[2]	t_{RC}, t_{WC}	(WS + 2) × T_C –4.0 [2 ≤WS ≤7] (WS + 3) × T_C –4.0 [WS ≥ 8]	22.7 69.3	— —	ns ns
101	Address and AA valid to $\overline{WR}$ assertion	t_{AS}	0.75 × T_C – 3.0 [2 ≤WS ≤3] 1.25 × T_C – 3.0 [WS ≥ 4]	2.0 5.3	— —	ns ns
102	$\overline{WR}$ assertion pulse width	t_{WP}	WS × T_C –4.0 [2 ≤WS ≤3] (WS –0.5) × T_C –4.0 [WS ≥ 4]	9.3 19.3	— —	ns ns
103	$\overline{WR}$ deassertion to address not valid	t_{WR}	1.25 × T_C –4.0 [2 ≤WS ≤7] 2.25 × T_C –4.0 [WS ≥ 8]	4.3 11.0	— —	ns ns
104	Address and AA valid to input data valid	t_{AA}, t_{AC}	(WS + 0.75) × T_C –6.5 [WS ≥ 2]	—	11.8	ns
105	$\overline{RD}$ assertion to input data valid	t_{OE}	(WS + 0.25) × T_C –6.5 [WS ≥ 2]	—	8.5	ns
106	$\overline{RD}$ deassertion to data not valid (data hold time)	t_{OHZ}		0.0	—	ns
107	Address valid to $\overline{WR}$ deassertion[2]	t_{AW}	(WS + 0.75) × T_C –4.0 [WS ≥ 2]	14.3	—	ns
108	Data valid to $\overline{WR}$ deassertion (data set-up time)	t_{DS} (t_{DW})	(WS –0.25) × T_C –5.4 [WS ≥ 2]	6.3	—	ns
109	Data hold time from $\overline{WR}$ deassertion	t_{DH}	1.25 × T_C –4.0 [2 ≤WS ≤7] 2.25 × T_C –4.0 [WS ≥ 8]	4.3 11.0	— —	ns ns
110	$\overline{WR}$ assertion to data active	—	0.25 × T_C –4.0 [2 ≤WS ≤3] –0.25 × T_C –4.0 [WS ≥ 4]	–2.4 –5.7	— —	ns ns

Table 2-8. SRAM Timing (Continued)

No.	Characteristics	Symbol	Expression[1]	150 MHz		Unit
				Min	Max	
111	$\overline{WR}$ deassertion to data high impedance	—	$1.25 \times T_C$ [2 ≤WS ≤7] $2.25 \times T_C$ [WS ≥ 8]	— —	8.3 15.0	ns ns
112	Previous $\overline{RD}$ deassertion to data active (write)	—	$2.25 \times T_C - 4.0$ [2 ≤WS ≤7] $3.25 \times T_C - 4.0$ [WS ≥ 8]	11.0 17.7	— —	ns ns
113	$\overline{RD}$ deassertion time	—	$1.75 \times T_C - 4.0$ [2 ≤WS ≤7] $2.75 \times T_C - 4.0$ [WS ≥ 8]	7.6 14.3	— —	ns ns
114	$\overline{WR}$ deassertion time[4]	—	$1.5 \times T_C - 4.0$ [2 ≤WS ≤7] $2.5 \times T_C - 4.0$ [WS ≥ 8]	6.0 12.7	— —	ns ns
115	Address valid to $\overline{RD}$ assertion	—	$0.5 \times T_C - 2.8$	0.5	—	ns
116	$\overline{RD}$ assertion pulse width	—	$(WS + 0.25) \times T_C - 4.0$	11.0	—	ns
117	$\overline{RD}$ deassertion to address not valid	—	$1.25 \times T_C - 4.0$ [2 ≤WS ≤7] $2.25 \times T_C - 4.0$ [WS ≥ 8]	4.3 11.0	— —	ns ns
118	$\overline{TA}$ set-up before $\overline{RD}$ or $\overline{WR}$ deassertion[5]	—	$0.25 \times T_C + 1.5$	3.2	—	ns
119	$\overline{TA}$ hold after $\overline{RD}$ or $\overline{WR}$ deassertion	—		0	—	ns

Notes:
1. WS is the number of wait states specified in the BCR. The value is given for the minimum for a given category. (For example, for a category of [2 ≤WS ≤7] timing is specified for 2 wait states.) Two wait states is the minimum otherwise.
2. Timings 100 and107 are guaranteed by design, not tested.
3. All timings for 150 MHz are measured from $0.5 \times V_{CCQH}$ to $0.5 \times V_{CCQH}$.
4. The WS number applies to the access in which the deassertion of $\overline{WR}$ occurs and assumes the next access uses a minimal number of wait states.
5. Timing 118 is relative to the deassertion edge of $\overline{RD}$ or $\overline{WR}$ even if $\overline{TA}$ remains asserted.

2.4.5.2 DRAM Timing

The selection guides in **Figure 2-12** and **Figure 2-15** are for primary selection only. Final selection should be based on the timing in the following tables. For example, the selection guide suggests that four wait states must be used for 100 MHz operation with Page Mode DRAM. However, consulting the appropriate table, a designer can evaluate whether fewer wait states might suffice by determining which timing prevents operation at 100 MHz, running the chip at a slightly lower frequency (for example, 95 MHz), using faster DRAM (if it becomes available), and manipulating control factors such as capacitive and resistive load to improve overall system performance.

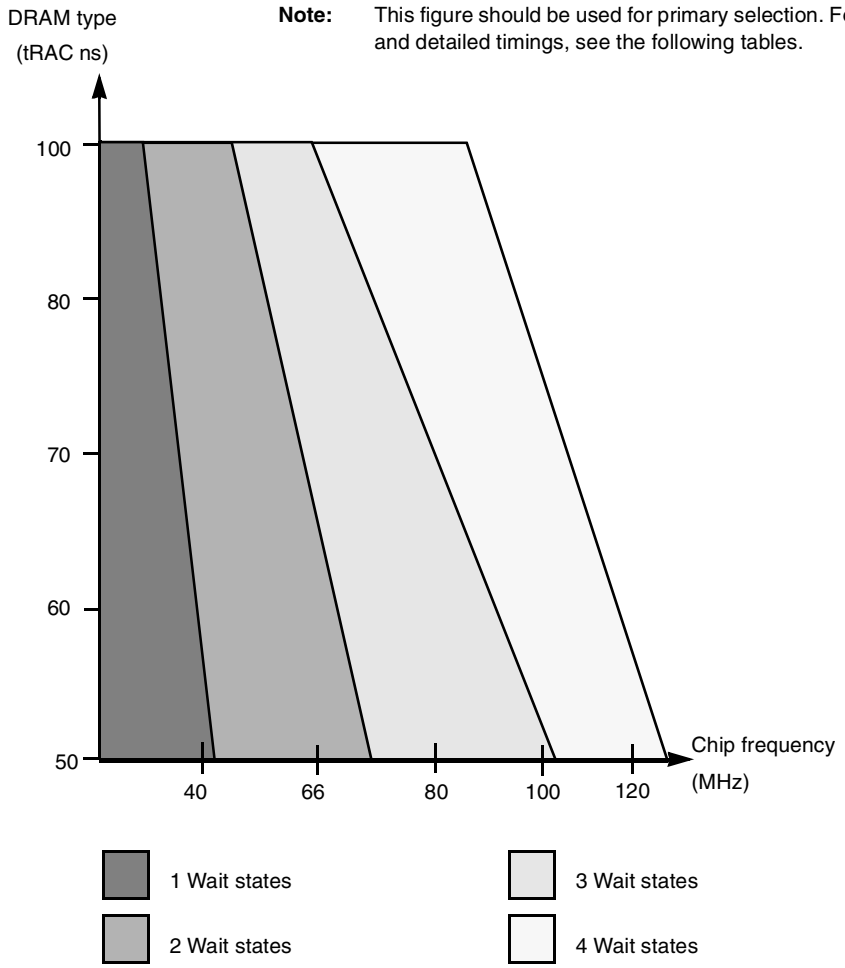


Figure 2-12. DRAM Page Mode Wait State Selection Guide

Table 2-9. DRAM Page Mode Timings, Three Wait States[1,2,3]

No.	Characteristics	Symbol	Expression[4]	100 MHz		Unit
				Min	Max	
131	Page mode cycle time for two consecutive accesses of the same direction		$4 \times T_C$	40.0	—	ns
	Page mode cycle time for mixed (read and write) accesses	t_{PC}	$3.5 \times T_C$	35.0	—	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$2 \times T_C - 5.7$	—	14.3	ns
133	Column address valid to data valid (read)	t_{AA}	$3 \times T_C - 5.7$	—	24.3	ns

Table 2-11. DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1,2] (Continued)

No.	Characteristics	Symbol	Expression[3]	100 MHz		Unit
				Min	Max	
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$1.75 \times T_C - 4.0$	13.5	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	3.5	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$5.25 \times T_C - 4.0$	48.5	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$7.75 \times T_C - 4.0$	73.5	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$6 \times T_C - 4.0$	56.0	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$3.0 \times T_C - 4.0$	26.0	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[4] assertion	t_{RCH}	$1.75 \times T_C - 3.7$	13.8	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[4] assertion	t_{RRH}	$0.25 \times T_C - 2.0$	0.5	—	ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$5 \times T_C - 4.2$	45.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$7.5 \times T_C - 4.2$	70.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$11.5 \times T_C - 4.5$	110.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$11.75 \times T_C - 4.3$	113.2	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$10.25 \times T_C - 4.3$	98.2	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$5.75 \times T_C - 4.0$	53.5	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$5.25 \times T_C - 4.0$	48.5	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$7.75 \times T_C - 4.0$	73.5	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$6.5 \times T_C - 4.3$	60.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	11.0	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$2.75 \times T_C - 4.0$	23.5	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$11.5 \times T_C - 4.0$	111.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	$10 \times T_C - 7.0$	—	93.0	ns
193	$\overline{RD}$ deassertion to data not valid[5]	t_{GZ}		0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 1.5$	6.0	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	ns

Notes:
1. The number of wait states for an out-of-page access is specified in the DRAM Control Register.
2. The refresh period is specified in the DRAM Control Register.
3. Use the expression to compute the maximum or minimum value listed (or both if the expression includes ±).
4. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.
5. $\overline{RD}$ deassertion always occurs after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

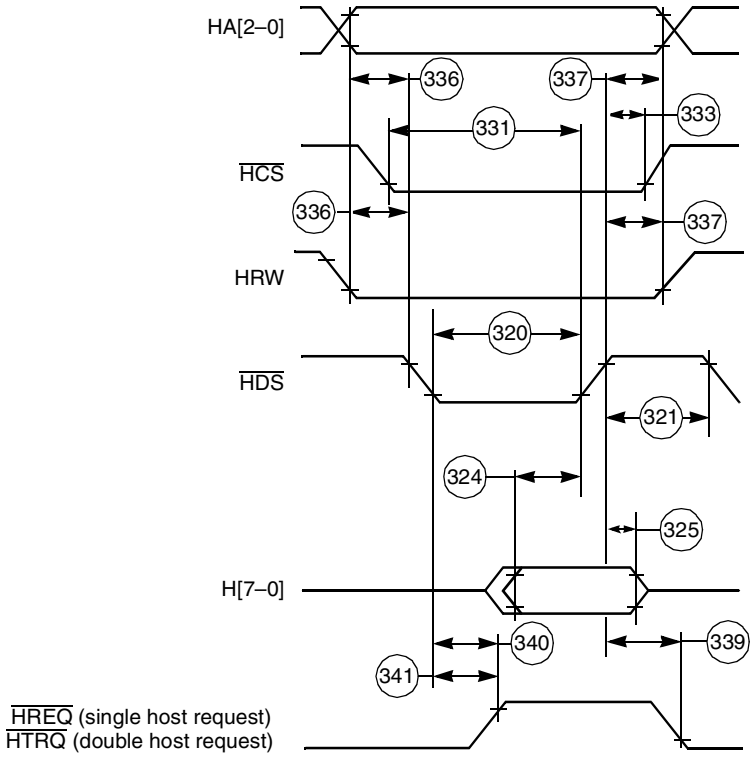


Figure 2-23. Write Timing Diagram, Non-Multiplexed Bus, Single Data Strobe

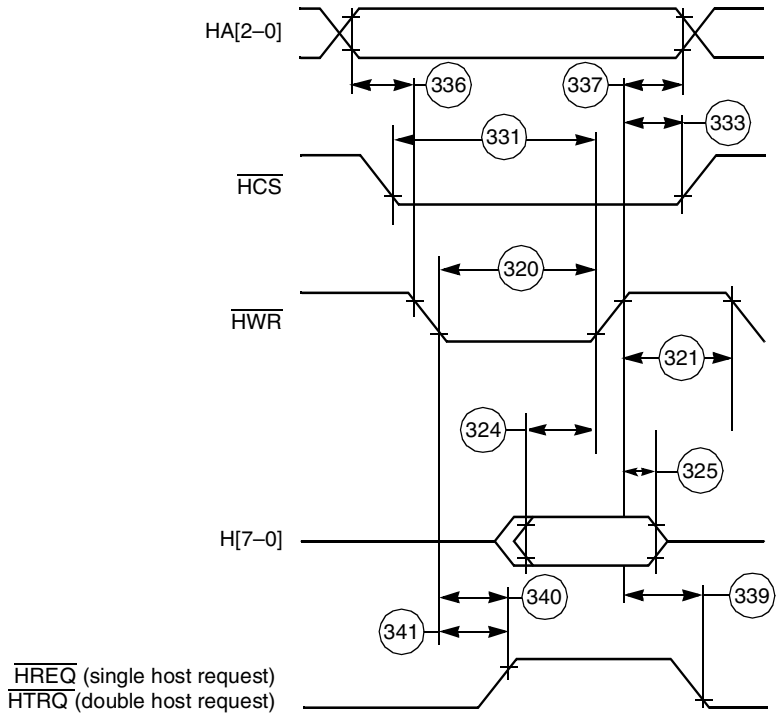


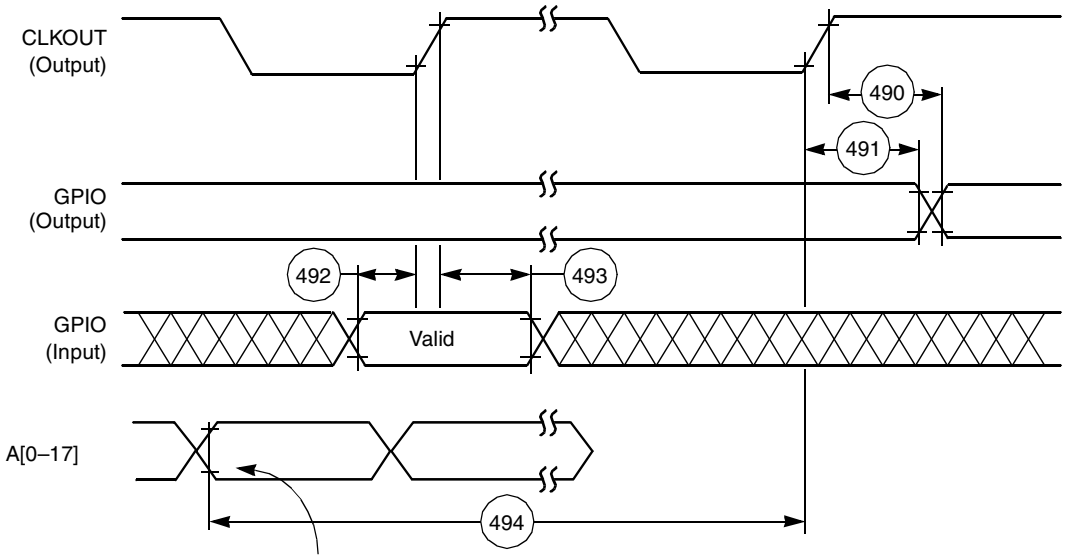
Figure 2-24. Write Timing Diagram, Non-Multiplexed Bus, Double Data Strobe

2.4.10 Considerations For GPIO Use

2.4.10.1 Operating Frequency of 100 MHz or Less

Table 2-18. GPIO Timing

No.	Characteristics	Expression	100 MHz		Unit
			Min	Max	
490	CLKOUT edge to GPIO out valid (GPIO out delay time)		—	8.5	ns
491	CLKOUT edge to GPIO out not valid (GPIO out hold time)		0.0	—	ns
492	GPIO In valid to CLKOUT edge (GPIO in set-up time)		8.5	—	ns
493	CLKOUT edge to GPIO in not valid (GPIO in hold time)		0.0	—	ns
494	Fetch to CLKOUT edge before GPIO change	Minimum: 6.75 × T_C	67.5	—	ns
Note:	V_{CC} = 3.3 V ± 0.3 V; T_J = -40°C to +100 °C, C_L = 50 pF.				



Fetch the instruction MOVE X0,X:(R0); X0 contains the new value of GPIO and R0 contains the address of the GPIO data register.

Figure 2-34. GPIO Timing

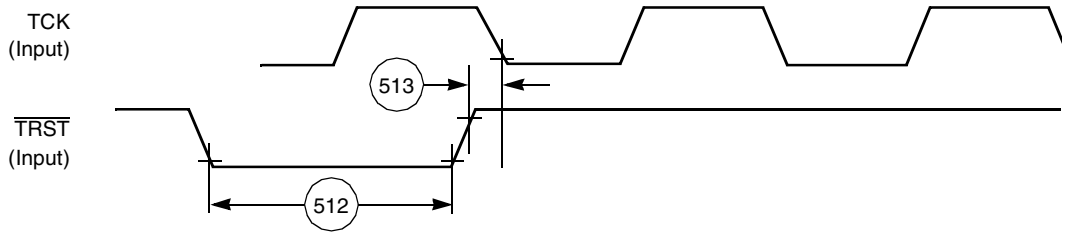


Figure 2-38. $\overline{\text{TRST}}$ Timing Diagram

2.4.12 OnCE Module TimIng

Table 2-20. OnCE Module Timing

No.	Characteristics	Expression	150 MHz		Unit
			Min	Max	
500	TCK frequency of operation	Max 22.0 MHz	0.0	22.0	MHz
514	$\overline{\text{DE}}$ assertion time in order to enter Debug mode	$1.5 \times T_C + 10.0$	20.0	—	ns
515	Response time when DSP56311 is executing NOP instructions from internal memory	$5.5 \times T_C + 30.0$	—	67.0	ns
516	Debug acknowledge assertion time	$3 \times T_C + 5.0$	25.0	—	ns
Note:	$V_{CCQH} = 3.3\ V \pm 0.3\ V$, $V_{CC} = 1.8\ V \pm 0.1\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF$				

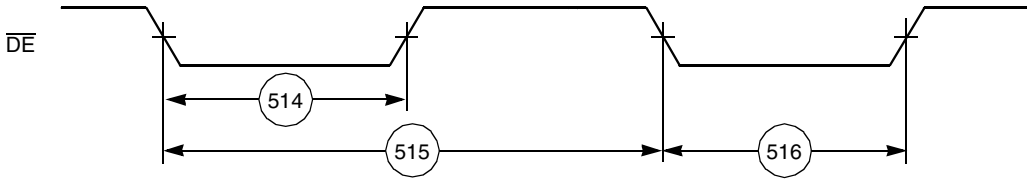


Figure 2-39. OnCE—Debug Request

Table 3-1. Signal List by Ball Number (Continued)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
L11	GND	M13	A1	P1	NC
L12	V_{CCA}	M14	A2	P2	H5, HAD5, or PB5
L13	A3	N1	H6, HAD6, or PB6	P3	H3, HAD3, or PB3
L14	A4	N2	H7, HAD7, or PB7	P4	H1, HAD1, or PB1
M1	HA1, HA8, or PB9	N3	H4, HAD4, or PB4	P5	PCAP
M2	HA2, HA9, or PB10	N4	H2, HAD2, or PB2	P6	GND_{P1}
M3	HA0, $\overline{HAS}$/HAS, or PB8	N5	$\overline{RESET}$	P7	AA2/$\overline{RAS2}$
M4	V_{CCH}	N6	GND_P	P8	XTAL
M5	H0, HAD0, or PB0	N7	AA3/$\overline{RAS3}$	P9	V_{CCC}
M6	V_{CCP}	N8	CAS	P10	$\overline{TA}$
M7	V_{CCQH}	N9	V_{CCQL}	P11	$\overline{BB}$
M8	EXTAL	N10	BCLK[2]	P12	AA1/$\overline{RAS1}$
M9	CLKOUT[2]	N11	$\overline{BR}$	P13	$\overline{BG}$
M10	$\overline{BCLK}$[2]	N12	V_{CCC}	P14	NC
M11	$\overline{WR}$	N13	AA0/$\overline{RAS0}$		
M12	$\overline{RD}$	N14	A0		

Notes:
1. Signal names are based on configured functionality. Most connections supply a single signal. Some connections provide a signal with dual functionality, such as the MODx/$\overline{IRQx}$ pins that select an operating mode after $\overline{RESET}$ is deasserted but act as interrupt lines during operation. Some signals have configurable polarity; these names are shown with and without overbars, such as $\overline{HAS}$/HAS. Some connections have two or more configurable functions; names assigned to these connections indicate the function for a specific configuration. For example, connection N2 is data line H7 in non-multiplexed bus mode, data/address line HAD7 in multiplexed bus mode, or GPIO line PB7 when the GPIO function is enabled for this pin. Unlike in the TQFP package, most of the GND pins are connected internally in the center of the connection array and act as heat sink for the chip. Therefore, except for GND_P and GND_{P1} that support the PLL, other GND signals do not support individual subsystems in the chip.
2. CLKOUT, $\overline{BCLK}$, and BCLK are available only if the operating frequency is ≤100 MHz.

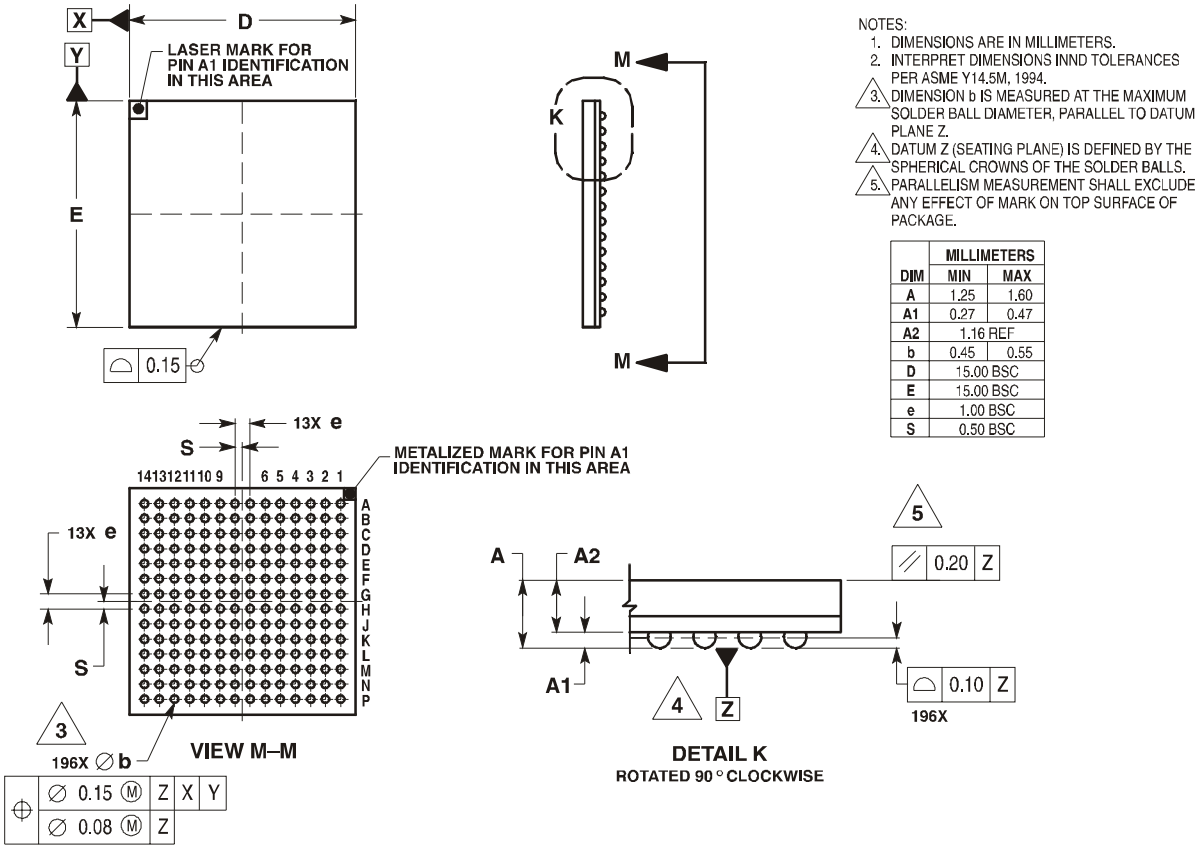
Table 3-2. Signal List by Signal Name (Continued)

Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.
GND	F11	GND	K4	H7	N2
GND	G4	GND	K5	HA0	M3
GND	G5	GND	K6	HA1	M1
GND	G6	GND	K7	HA10	L1
GND	G7	GND	K8	HA2	M2
GND	G8	GND	K9	HA8	M1
GND	G9	GND	K10	HA9	M2
GND	G10	GND	K11	$\overline{\text{HACK}}$/HACK	J1
GND	G11	GND	L4	HAD0	M5
GND	H4	GND	L5	HAD1	P4
GND	H5	GND	L6	HAD2	N4
GND	H6	GND	L7	HAD3	P3
GND	H7	GND	L8	HAD4	N3
GND	H8	GND	L9	HAD5	P2
GND	H9	GND	L10	HAD6	N1
GND	H10	GND	L11	HAD7	N2
GND	H11	GND_P	N6	$\overline{\text{HAS}}$/HAS	M3
GND	J4	GND_{P1}	P6	$\overline{\text{HCS}}$/HCS	L1
GND	J5	H0	M5	$\overline{\text{HDS}}$/HDS	J3
GND	J6	H1	P4	$\overline{\text{HRD}}$/HRD	J2
GND	J7	H2	N4	$\overline{\text{HREQ}}$/HREQ	K2
GND	J8	H3	P3	$\overline{\text{HRRQ}}$/HRRQ	J1
GND	J9	H4	N3	HRW	J2
GND	J10	H5	P2	$\overline{\text{HTRQ}}$/HTRQ	K2
GND	J11	H6	N2	$\overline{\text{HWR}}$/HWR	J3

Table 3-2. Signal List by Signal Name (Continued)

Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.
$\overline{\text{IRQA}}$	C4	PC3	H3	STD1	C2
$\overline{\text{IRQB}}$	A5	PC4	E3	$\overline{\text{TA}}$	P10
$\overline{\text{IRQC}}$	C5	PC5	E1	TCK	C3
$\overline{\text{IRQD}}$	B5	PCAP	P5	TDI	B3
MODA	C4	PD0	F2	TDO	A4
MODB	A5	PD1	A2	TIO0	L3
MODC	C5	PD2	B2	TIO1	L2
MODD	B5	PD3	G1	TIO2	K3
NC	A1	PD4	B1	TMS	A3
NC	A14	PD5	C2	$\overline{\text{TRST}}$	B4
NC	B14	PE0	F1	TXD	G3
NC	P1	PE1	G3	V_{CCA}	H12
NC	P14	PE2	G2	V_{CCA}	K12
$\overline{\text{NMI}}$	D1	PINIT	D1	V_{CCA}	L12
PB0	M5	$\overline{\text{RAS0}}$	N13	V_{CCC}	N12
PB1	P4	$\overline{\text{RAS1}}$	P12	V_{CCC}	P9
PB10	M2	$\overline{\text{RAS2}}$	P7	V_{CCD}	A7
PB11	J2	$\overline{\text{RAS3}}$	N7	V_{CCD}	C9
PB12	J3	$\overline{\text{RD}}$	M12	V_{CCD}	C11
PB13	L1	$\overline{\text{RESET}}$	N5	V_{CCD}	D14
PB14	K2	RXD	F1	V_{CCH}	M4
PB15	J1	SC00	F3	V_{CCP}	M6
PB2	N4	SC01	D2	V_{CCQH}	F12
PB3	P3	SC02	C1	V_{CCQH}	H1
PB4	N3	SC10	F2	V_{CCQH}	M7
PB5	P2	SC11	A2	V_{CCQL}	C7
PB6	N1	SC12	B2	V_{CCQL}	G13
PB7	N2	SCK0	H3	V_{CCQL}	H2
PB8	M3	SCK1	G1	V_{CCQL}	N9
PB9	M1	SCLK	G2	V_{CCS}	E2
PC0	F3	SRD0	E3	V_{CCS}	K1
PC1	D2	SRD1	B1	$\overline{\text{WR}}$	M11
PC2	C1	STD0	E1	XTAL	P8

3.2 MAP-BGA Package Mechanical Drawing



CASE 1128C–01
ISSUE O

DATE 07/28/98

Figure 3-3. DSP56311 Mechanical Information, 196-pin MAP-BGA Package

```
;       Interrupt Priority Register Core (IPRC)

M_IAL EQU $7                        ; IRQA Mode Mask
M_IAL0 EQU 0                        ; IRQA Mode Interrupt Priority Level (low)
M_IAL1 EQU 1                        ; IRQA Mode Interrupt Priority Level (high)
M_IAL2 EQU 2                        ; IRQA Mode Trigger Mode
M_IBL EQU $38                       ; IRQB Mode Mask
M_IBL0 EQU 3                        ; IRQB Mode Interrupt Priority Level (low)
M_IBL1 EQU 4                        ; IRQB Mode Interrupt Priority Level (high)
M_IBL2 EQU 5                        ; IRQB Mode Trigger Mode
M_ICL EQU $1C0                      ; IRQC Mode Mask
M_ICL0 EQU 6                        ; IRQC Mode Interrupt Priority Level (low)
M_ICL1 EQU 7                        ; IRQC Mode Interrupt Priority Level (high)
M_ICL2 EQU 8                        ; IRQC Mode Trigger Mode
M_IDL EQU $E00                      ; IRQD Mode Mask
M_IDL0 EQU 9                        ; IRQD Mode Interrupt Priority Level (low)
M_IDL1 EQU 10                       ; IRQD Mode Interrupt Priority Level (high)
M_IDL2 EQU 11                       ; IRQD Mode Trigger Mode
M_D0L EQU $3000                     ; DMA0 Interrupt priority Level Mask
M_D0L0 EQU 12                       ; DMA0 Interrupt Priority Level (low)
M_D0L1 EQU 13                       ; DMA0 Interrupt Priority Level (high)
M_D1L EQU $C000                     ; DMA1 Interrupt Priority Level Mask
M_D1L0 EQU 14                       ; DMA1 Interrupt Priority Level (low)
M_D1L1 EQU 15                       ; DMA1 Interrupt Priority Level (high)
M_D2L EQU $30000                    ; DMA2 Interrupt priority Level Mask
M_D2L0 EQU 16                       ; DMA2 Interrupt Priority Level (low)
M_D2L1 EQU 17                       ; DMA2 Interrupt Priority Level (high)
M_D3L EQU $C0000                    ; DMA3 Interrupt Priority Level Mask
M_D3L0 EQU 18                       ; DMA3 Interrupt Priority Level (low)
M_D3L1 EQU 19                       ; DMA3 Interrupt Priority Level (high)
M_D4L EQU $300000                   ; DMA4 Interrupt priority Level Mask
M_D4L0 EQU 20                       ; DMA4 Interrupt Priority Level (low)
M_D4L1 EQU 21                       ; DMA4 Interrupt Priority Level (high)
M_D5L EQU $C00000                   ; DMA5 Interrupt priority Level Mask
M_D5L0 EQU 22                       ; DMA5 Interrupt Priority Level (low)
M_D5L1 EQU 23                       ; DMA5 Interrupt Priority Level (high)


;       Interrupt Priority Register Peripheral (IPRP)

M_HPL EQU $3                        ; Host Interrupt Priority Level Mask
M_HPL0 EQU 0                        ; Host Interrupt Priority Level (low)
M_HPL1 EQU 1                        ; Host Interrupt Priority Level (high)
M_S0L EQU $C                        ; SSI0 Interrupt Priority Level Mask
M_S0L0 EQU 2                        ; SSI0 Interrupt Priority Level (low)
M_S0L1 EQU 3                        ; SSI0 Interrupt Priority Level (high)
M_S1L EQU $30                       ; SSI1 Interrupt Priority Level Mask
M_S1L0 EQU 4                        ; SSI1 Interrupt Priority Level (low)
M_S1L1 EQU 5                        ; SSI1 Interrupt Priority Level (high)
M_SCL EQU $C0                       ; SCI  Interrupt Priority Level  Mask
M_SCL0 EQU 6                        ; SCI  Interrupt Priority Level  (low)
M_SCL1 EQU 7                        ; SCI  Interrupt Priority Level  (high)
M_T0L EQU $300                      ; TIMER Interrupt Priority Level Mask
M_T0L0 EQU 8                        ; TIMER Interrupt Priority Level (low)
M_T0L1 EQU 9                        ; TIMER Interrupt Priority Level (high)


;---------------------------------------------------------------------
;
;       EQUATES for TIMER
;
;---------------------------------------------------------------------
```

Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Supply Voltage	Package Type	Pin Count	Core Frequency (MHz)	Solder Spheres	Order Number
DSP56311	1.8 V core 3.3 V I/O	Molded Array Process-Ball Grid Array (MAP-BGA)	196	150	Lead-free	DSP56311VL150
					Lead-bearing	DSP56311VF150

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