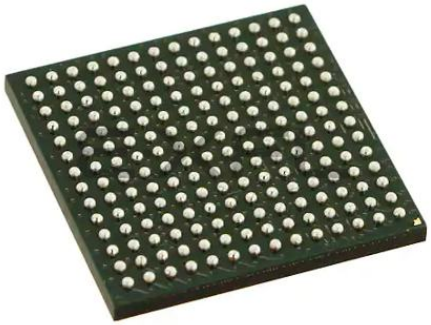

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	150MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56311vf150r2

Signals/Connections 1

The DSP56311 input and output signals are organized into functional groups as shown in **Table 1-1**. **Figure 1-1** diagrams the DSP56311 signals by functional group. The remainder of this chapter describes the signal pins in each functional group.

Table 1-1. DSP56311 Functional Signal Groupings

Functional Group		Number of Signals
Power (V_{CC})		20
Ground (GND)		66
Clock		2
PLL		3
Address bus	Port A[1]	18
Data bus		24
Bus control		13
Interrupt and mode control		5
Host interface (HI08)	Port B[2]	16
Enhanced synchronous serial interface (ESSI)	Ports C and D[3]	12
Serial communication interface (SCI)	Port E[4]	3
Timer		3
OnCE/JTAG Port		6

Notes:
1. Port A signals define the external memory interface port, including the external address bus, data bus, and control signals.
2. Port B signals are the HI08 port signals multiplexed with the GPIO signals.
3. Port C and D signals are the two ESSI port signals multiplexed with the GPIO signals.
4. Port E signals are the SCI port signals multiplexed with the GPIO signals.
5. There are 5 signal connections that are not used. These are designated as no connect (NC) in the package description (see **Chapter 3**).

Note: The Clock Output (CLKOUT), BCLK, $\overline{\text{BCLK}}$, $\overline{\text{CAS}}$, and $\overline{\text{RAS[0–3]}}$ signals used by other DSP56300 family members are supported by the DSP56311 at operating frequencies up to 100 MHz. Therefore, above 100 MHz, you must enable bus arbitration by setting the Asynchronous Bus Arbitration Enable Bit (ABE) in the operating mode register. When set, the ABE bit eliminates the required set-up and hold times for $\overline{\text{BB}}$ and $\overline{\text{BG}}$ with respect to $\overline{\text{CLKOUT}}$. In addition, DRAM access is not supported above 100 MHz.

1.7 Host Interface (HI08)

The HI08 provides a fast, 8-bit, parallel data port that connects directly to the host bus. The HI08 supports a variety of standard buses and connects directly to a number of industry-standard microcomputers, microprocessors, DSPs, and DMA hardware.

1.7.1 Host Port Usage Considerations

Careful synchronization is required when the system reads multiple-bit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected (as they are in the Host port). The considerations for proper operation are discussed in **Table 1-10**.

Table 1-10. Host Port Usage Considerations

Action	Description
Asynchronous read of receive byte registers	When reading the receive byte registers, Receive register High (RXH), Receive register Middle (RXM), or Receive register Low (RXL), the host interface programmer should use interrupts or poll the Receive register Data Full (RXDF) flag that indicates data is available. This assures that the data in the receive byte registers is valid.
Asynchronous write to transmit byte registers	The host interface programmer should not write to the transmit byte registers, Transmit register High (TXH), Transmit register Middle (TXM), or Transmit register Low (TXL), unless the Transmit register Data Empty (TXDE) bit is set indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers transfer valid data to the Host Receive (HRX) register.
Asynchronous write to host vector	The host interface programmer must change the Host Vector (HV) register only when the Host Command bit (HC) is clear. This practice guarantees that the DSP interrupt control logic receives a stable vector.

1.7.2 Host Port Configuration

HI08 signal functions vary according to the programmed configuration of the interface as determined by the 16 bits in the HI08 Port Control Register.

Table 1-11. Host Interface

Signal Name	Type	State During Reset[1,2]	Signal Description
H[0–7]	Input/Output	Ignored Input	**Host Data—**When the HI08 is programmed to interface with a non-multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the bidirectional Data bus.
HAD[0–7]	Input/Output		**Host Address—**When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the bidirectional multiplexed Address/Data bus.
PB[0–7]	Input or Output		**Port B 0–7—**When the HI08 is configured as GPIO through the HI08 Port Control Register, these signals are individually programmed as inputs or outputs through the HI08 Data Direction Register.

Table 1-13. Enhanced Serial Synchronous Interface 1 (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
SCK1	Input/Output	Ignored Input	**Serial Clock**—Provides the serial bit rate clock for the ESSI. The SCK1 is a clock input or output used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PD3	Input or Output		**Port D 3**—The default configuration following reset is GPIO input PD3. When configured as PD3, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SCK1 through the Port D Control Register.
SRD1	Input	Ignored Input	**Serial Receive Data**—Receives serial data and transfers the data to the ESSI Receive Shift Register. SRD1 is an input when data is being received.
PD4	Input or Output		**Port D 4**—The default configuration following reset is GPIO input PD4. When configured as PD4, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SRD1 through the Port D Control Register.
STD1	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the Serial Transmit Shift Register. STD1 is an output when data is being transmitted.
PD5	Input or Output		**Port D 5**—The default configuration following reset is GPIO input PD5. When configured as PD5, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal STD1 through the Port D Control Register.

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

1.10 Serial Communication Interface (SCI)

The SCI provides a full duplex port for serial communication with other DSPs, microprocessors, or peripherals such as modems.

Table 1-14. Serial Communication Interface

Signal Name	Type	State During Reset[1,2]	Signal Description
RXD	Input	Ignored Input	**Serial Receive Data**—Receives byte-oriented serial data and transfers it to the SCI Receive Shift Register.
PE0	Input or Output		**Port E 0**—The default configuration following reset is GPIO input PE0. When configured as PE0, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal RXD through the Port E Control Register.
TXD	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the SCI Transmit Data Register.
PE1	Input or Output		**Port E 1**—The default configuration following reset is GPIO input PE1. When configured as PE1, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal TXD through the Port E Control Register.

Table 1-14. Serial Communication Interface (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
SCLK	Input/Output	Ignored Input	**Serial Clock**—Provides the input or output clock used by the transmitter and/or the receiver.
PE2	Input or Output		**Port E 2**—The default configuration following reset is GPIO input PE2. When configured as PE2, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal SCLK through the Port E Control Register.

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

1.11 Timers

The DSP56311 has three identical and independent timers. Each timer can use internal or external clocking and can either interrupt the DSP56311 after a specified number of events (clocks) or signal an external device after counting a specific number of internal events.

Table 1-15. Triple Timer Signals

Signal Name	Type	State During Reset[1,2]	Signal Description
TIO0	Input or Output	Ignored Input	**Timer 0 Schmitt-Trigger Input/Output**— When Timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When Timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output. The default mode after reset is GPIO input. TIO0 can be changed to output or configured as a timer I/O through the Timer 0 Control/Status Register (TCSR0).
TIO1	Input or Output	Ignored Input	**Timer 1 Schmitt-Trigger Input/Output**— When Timer 1 functions as an external event counter or in measurement mode, TIO1 is used as input. When Timer 1 functions in watchdog, timer, or pulse modulation mode, TIO1 is used as output. The default mode after reset is GPIO input. TIO1 can be changed to output or configured as a timer I/O through the Timer 1 Control/Status Register (TCSR1).
TIO2	Input or Output	Ignored Input	**Timer 2 Schmitt-Trigger Input/Output**— When Timer 2 functions as an external event counter or in measurement mode, TIO2 is used as input. When Timer 2 functions in watchdog, timer, or pulse modulation mode, TIO2 is used as output. The default mode after reset is GPIO input. TIO2 can be changed to output or configured as a timer I/O through the Timer 2 Control/Status Register (TCSR2).

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

2.2 Thermal Characteristics

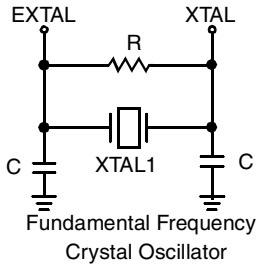
Table 2-2. Thermal Characteristics

Thermal Resistance Characteristic	Symbol	MAP-BGA Value	Unit
Junction-to-ambient, natural convection, single-layer board (1s)[1,2]	$R_{\theta JA}$	49	°C/W
Junction-to-ambient, natural convection, four-layer board (2s2p)[1,3]	$R_{\theta JMA}$	26	°C/W
Junction-to-ambient, @200 ft/min air flow, single layer board (1s)[1,3]	$R_{\theta JMA}$	39	°C/W
Junction-to-ambient, @200 ft/min air flow, four-layer board (2s2p)[1,3]	$R_{\theta JMA}$	22	°C/W
Junction-to-board[4]	$R_{\theta JB}$	14	°C/W
Junction-to-case thermal resistance[5]	$R_{\theta JC}$	5	°C/W
Junction-to-package-top, natural convection[6]	Ψ_{JT}	2	°C/W
Junction-to-package-top, @200 ft/min air flow[6]	Ψ_{JT}	2	°C/W

Notes:
1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

2.4.2 External Clock Operation

The DSP56311 system clock is derived from the on-chip oscillator or is externally supplied. To use the on-chip oscillator, connect a crystal and associated resistor/capacitor components to EXTAL and XTAL; examples are shown in **Figure 2-1**.



Note: Make sure that in the PCTL Register:
- XTLD (bit 16) = 0
- If f_{OSC} > 200 kHz, XTLR (bit 15) = 0

Suggested Component Values:

f_{OSC} = 4 MHz	f_{OSC} = 20 MHz
R = 680 kΩ±10%	R = 680 kΩ±10%
C = 56 pF ±20%	C = 22 pF ±20%

Calculations were done for a 4/20 MHz crystal with the following parameters:
- C_L of 30/20 pF,
- C_0 of 7/6 pF,
- series resistance of 100/20 Ω, and
- drive level of 2 mW.

Figure 2-1. Crystal Oscillator Circuits

If an externally-supplied square wave voltage source is used, disable the internal oscillator circuit during bootup by setting XTLD (PCTL Register bit 16 = 1—see the *DSP56311 User's Manual*). The external square wave source connects to EXTAL; XTAL is not physically connected to the board or socket. **Figure 2-2** shows the relationship between the EXTAL input and the internal clock and CLKOUT.

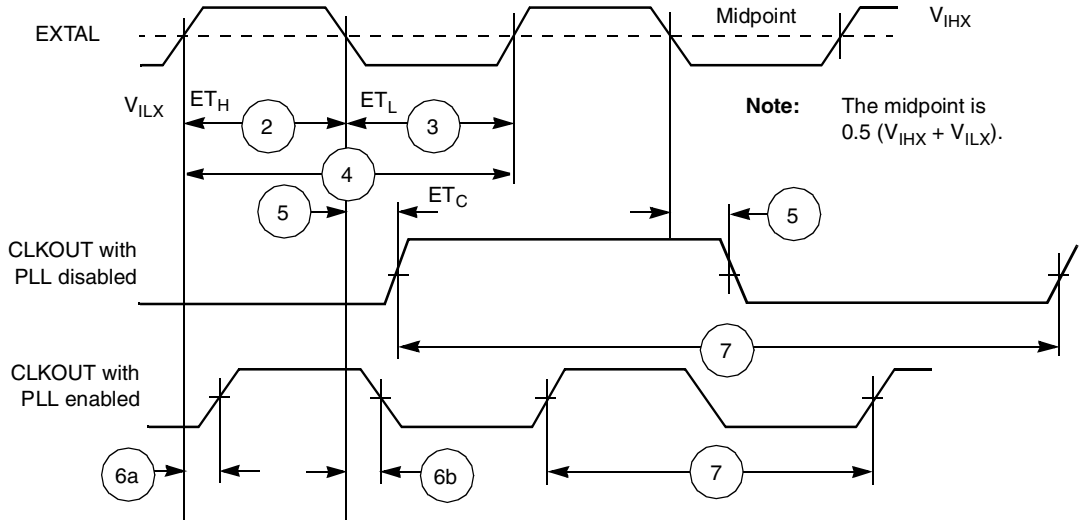


Figure 2-2. External Clock Timing

2.4.4 Reset, Stop, Mode Select, and Interrupt Timing

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[6]

No.	Characteristics	Expression	150 MHz		Unit
			Min	Max	
8	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[3]	—	—	26.0	ns
9	Required $\overline{\text{RESET}}$ duration[4]	Minimum:			
	• Power on, external clock generator, PLL disabled	$50 \times ET_C$	333.3	—	ns
	• Power on, external clock generator, PLL enabled	$1000 \times ET_C$	6.67	—	µs
	• Power on, internal oscillator	$75000 \times ET_C$	0.50	—	ms
	• During STOP, XTAL disabled (PCTL Bit 16 = 0)	$75000 \times ET_C$	0.50	—	ms
	• During STOP, XTAL enabled (PCTL Bit 16 = 1)	$2.5 \times T_C$	16.7	—	ns
	• During normal operation	$2.5 \times T_C$	16.7	—	ns
10	Delay from asynchronous $\overline{\text{RESET}}$ deassertion to first external address output (internal reset deassertion)[5]				
	• Minimum	$3.25 \times T_C + 2.0$	23.7	—	ns
	• Maximum	$20.25 \times T_C + 10$	—	145.0	ns
13	Mode select set-up time		30.0	—	ns
14	Mode select hold time		0.0	—	ns
15	Minimum edge-triggered interrupt request assertion width		6.6	—	ns
16	Minimum edge-triggered interrupt request deassertion width		6.6	—	ns
17	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory access address out valid	Minimum:			
	• Caused by first interrupt instruction fetch	$4.25 \times T_C + 2.0$	30.4	—	ns
	• Caused by first interrupt instruction execution	$7.25 \times T_C + 2.0$	51.0	—	ns
18	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution	Minimum: $10 \times T_C + 5.0$	72.0	—	ns
19	Delay from address output valid caused by first interrupt instruction execute to interrupt request deassertion for level sensitive fast interrupts[1, 7, 8]	Maximum: $(WS + 3.75) \times T_C - 10.94$	—	Note 8	ns
20	Delay from $\overline{\text{RD}}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1, 7, 8]	Maximum: $(WS + 3.25) \times T_C - 10.94$	—	Note 8	ns
21	Delay from $\overline{\text{WR}}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1, 7, 8]	Maximum:			
	• DRAM for all WS	$(WS + 3.5) \times T_C - 10.94$	—	Note 8	ns
	• SRAM WS = 1	$(WS + 3.5) \times T_C - 10.94$	—	Note 8	ns
	• SRAM WS = 2, 3	$(WS + 3) \times T_C - 10.94$	—	Note 8	ns
	• SRAM WS ≥ 4	$(WS + 2.5) \times T_C - 10.94$	—	Note 8	ns
24	Duration for $\overline{\text{IRQA}}$ assertion to recover from Stop state		5.9	—	ns
25	Delay from $\overline{\text{IRQA}}$ assertion to fetch of first instruction (when exiting Stop)[2, 3]				
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (Operating Mode Register Bit 6 = 0)	$PLC \times ET_C \times PDF + (128\text{ K} - PLC/2) \times T_C$	1.3	9.1	ms
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (Operating Mode Register Bit 6 = 1)	$PLC \times ET_C \times PDF + (23.75 \pm 0.5) \times T_C$	232.5 ns	12.3 ms	
	• PLL is active during Stop (PCTL Bit 17 = 1) (Implies No Stop Delay)	$(8.25 \pm 0.5) \times T_C$	51.7	58.3	ns

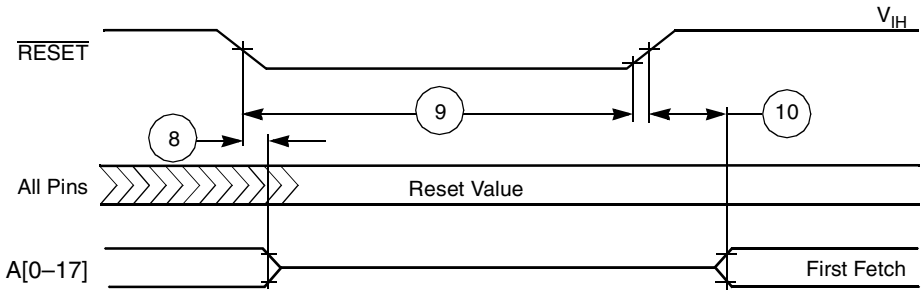
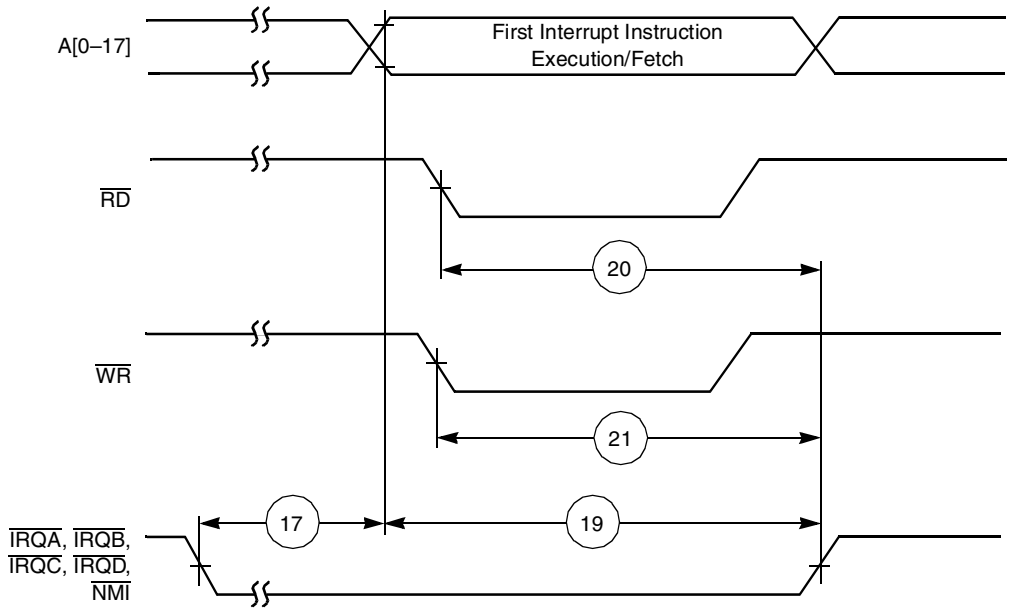
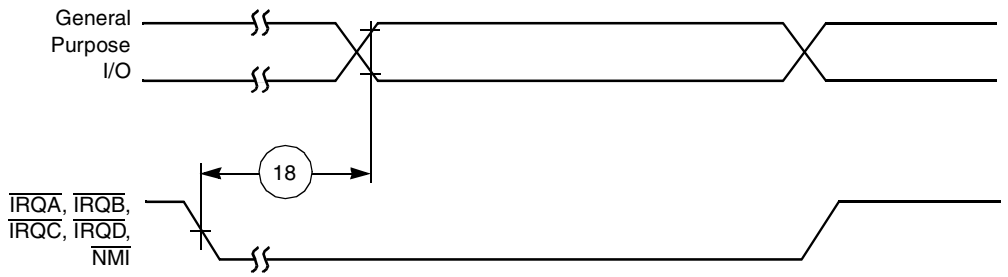


Figure 2-3. Reset Timing



a) First Interrupt Instruction Execution



b) General-Purpose I/O

Figure 2-4. External Fast Interrupt Timing

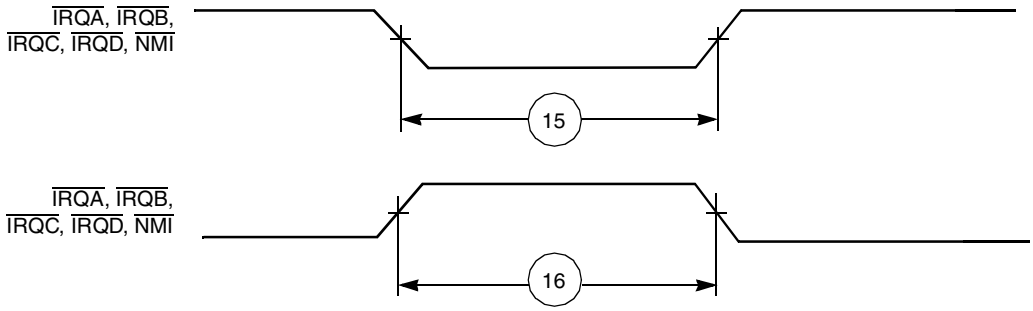


Figure 2-5. External Interrupt Timing (Negative Edge-Triggered)

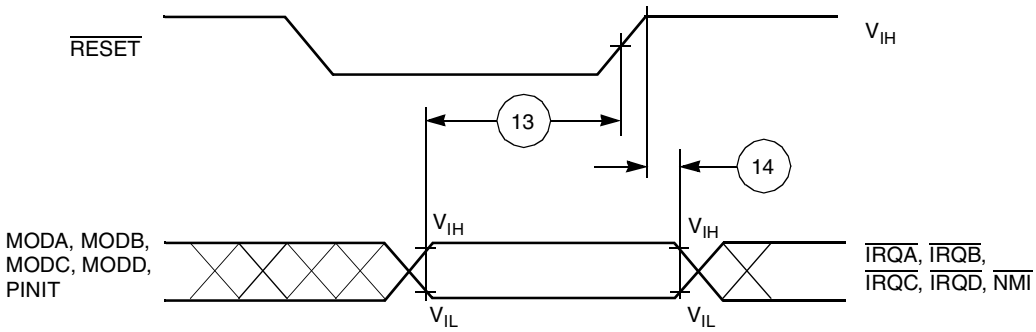


Figure 2-6. Operating Mode Select Timing

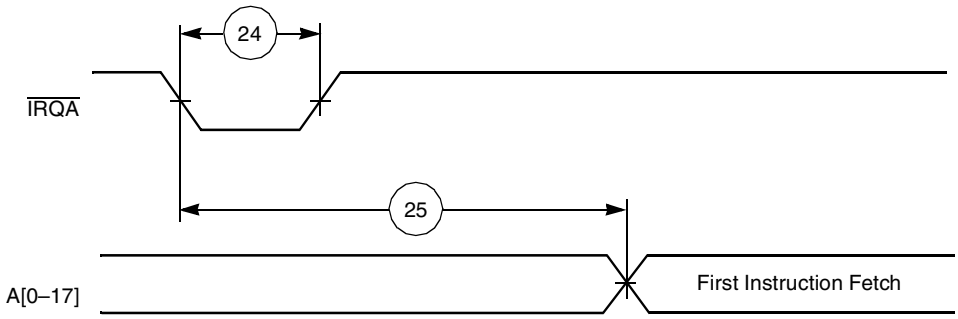


Figure 2-7. Recovery from Stop State Using IRQA

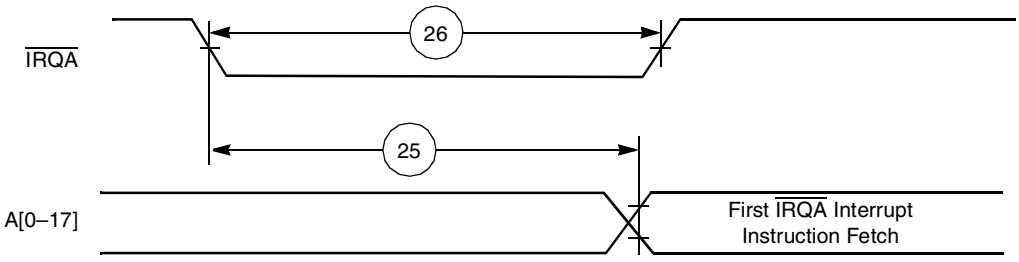


Figure 2-8. Recovery from Stop State Using IRQA Interrupt Service

Table 2-9. DRAM Page Mode Timings, Three Wait States[1,2,3] (Continued)

No.	Characteristics	Symbol	Expression[4]	100 MHz		Unit
				Min	Max	
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$2.5 \times T_C - 4.0$	21.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$4.5 \times T_C - 4.0$	41.0	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2 \times T_C - 4.0$	16.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ assertion[5] • BRW[1–0] = 00, 01—not applicable • BRW[1–0] = 10 • BRW[1–0] = 11	t_{CRP}	 — $4.75 \times T_C - 6.0$ $6.75 \times T_C - 6.0$	 — 41.5 61.5	 — — —	 — ns ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.5 \times T_C - 4.0$	11.0	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	6.0	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$2.5 \times T_C - 4.0$	21.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$4 \times T_C - 4.0$	36.0	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 4.0$	8.5	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.75 \times T_C - 4.0$	3.5	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$2.25 \times T_C - 4.2$	18.3	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$3.5 \times T_C - 4.5$	30.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$3.75 \times T_C - 4.3$	33.2	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$3.25 \times T_C - 4.3$	28.2	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.5$	0.5	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$2.5 \times T_C - 4.0$	21.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$1.25 \times T_C - 4.3$	8.2	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$3.5 \times T_C - 4.0$	31.0	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$2.5 \times T_C - 5.7$	—	19.3	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 1.5$	6.0	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	ns

Notes:
1. The number of wait states for Page mode access is specified in the DRAM Control Register.
2. The refresh period is specified in the DRAM Control Register.
3. The asynchronous delays specified in the expressions are valid for the DSP56311.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (for example, t_{PC} equals $4 \times T_C$ for read-after-read or write-after-write sequences). An expression is used to compute the number listed as the minimum or maximum value listed, as appropriate.
5. BRW[1–0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of page-access.
6. $\overline{RD}$ deassertion always occurs after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

2.4.5.3 Asynchronous Bus Arbitration Timings

Table 2-13. Asynchronous Bus Timings

No.	Characteristics	Expression	150 MHz		Unit
			Min	Max	
250	$\overline{BB}$ assertion window from $\overline{BG}$ input deassertion.	2.5 × Tc + 5	—	22	ns
251	Delay from $\overline{BB}$ assertion to $\overline{BG}$ assertion	2 × Tc + 5	18.3	—	ns

Notes:
1. Bit 13 in the Operating Mode Register must be set to enable Asynchronous Arbitration mode.
2. At 150 MHz, Asynchronous Arbitration mode is recommended.
3. To guarantee timings 250 and 251, it is recommended that you assert non-overlapping $\overline{BG}$ inputs to different DSP56300 devices (on the same bus), as shown in **Figure 2-19**, where $\overline{BG1}$ is the $\overline{BG}$ signal for one DSP56300 device while $\overline{BG2}$ is the $\overline{BG}$ signal for a second DSP56300 device.

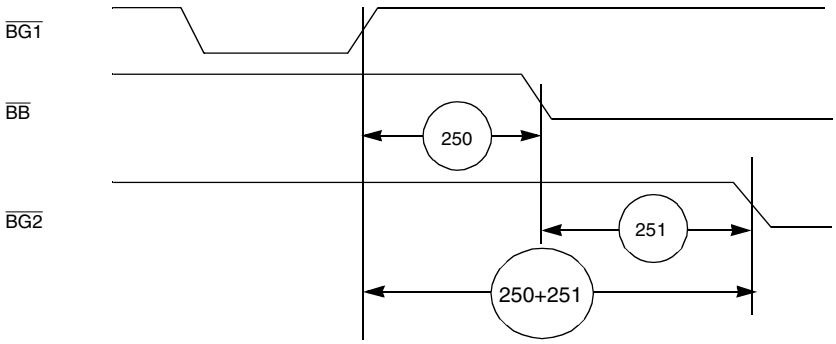


Figure 2-19. Asynchronous Bus Arbitration Timing

The asynchronous bus arbitration is enabled by internal synchronization circuits on $\overline{BG}$ and $\overline{BB}$ inputs. These synchronization circuits add delay from the external signal until it is exposed to internal logic. As a result of this delay, a DSP56300 part may assume mastership and assert $\overline{BB}$, for some time after $\overline{BG}$ is deasserted. This is the reason for timing 250.

Once $\overline{BB}$ is asserted, there is a synchronization delay from $\overline{BB}$ assertion to the time this assertion is exposed to other DSP56300 components that are potential masters on the same bus. If $\overline{BG}$ input is asserted before that time, and $\overline{BG}$ is asserted and $\overline{BB}$ is deasserted, another DSP56300 component may assume mastership at the same time. Therefore, some non-overlap period between one $\overline{BG}$ input active to another $\overline{BG}$ input active is required. Timing 251 ensures that overlaps are avoided.

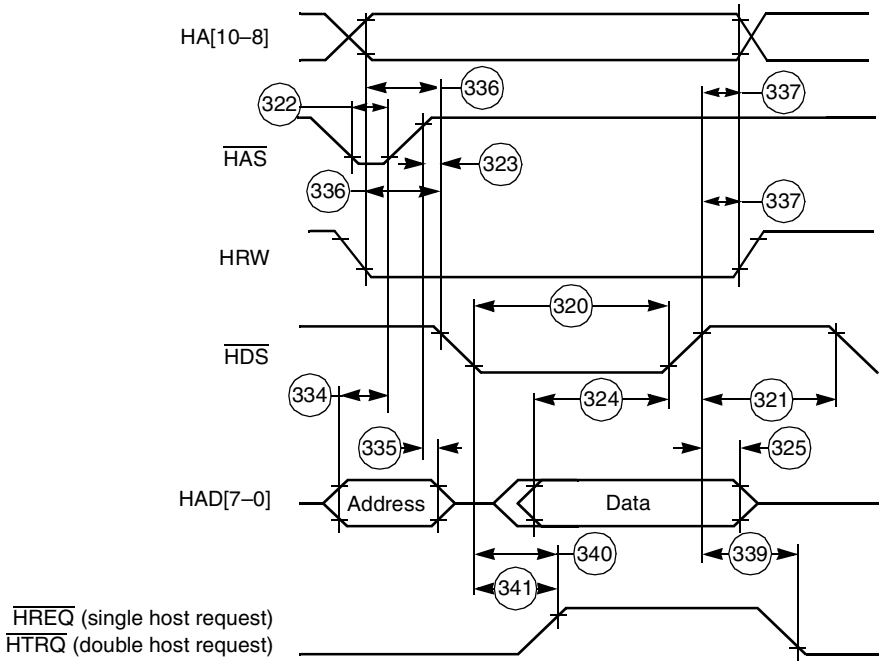


Figure 2-27. Write Timing Diagram, Multiplexed Bus, Single Data Strobe

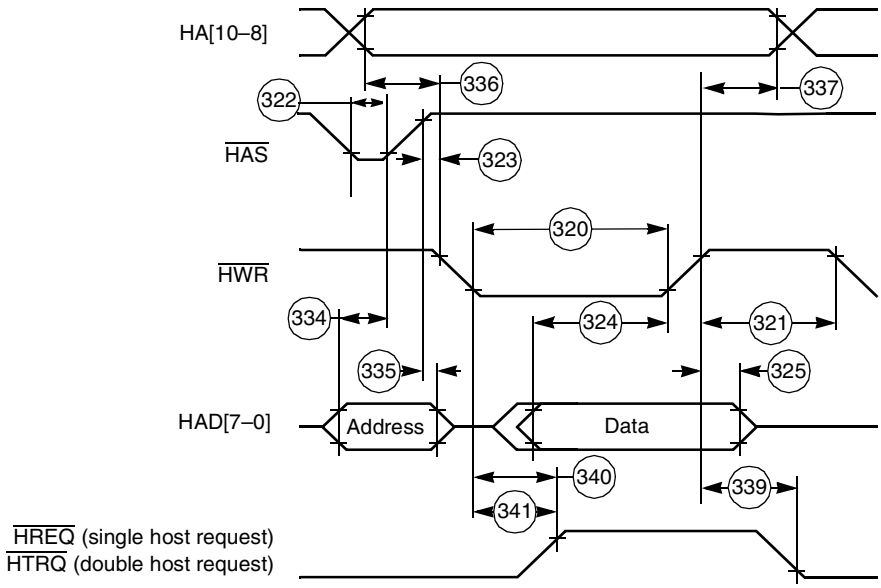
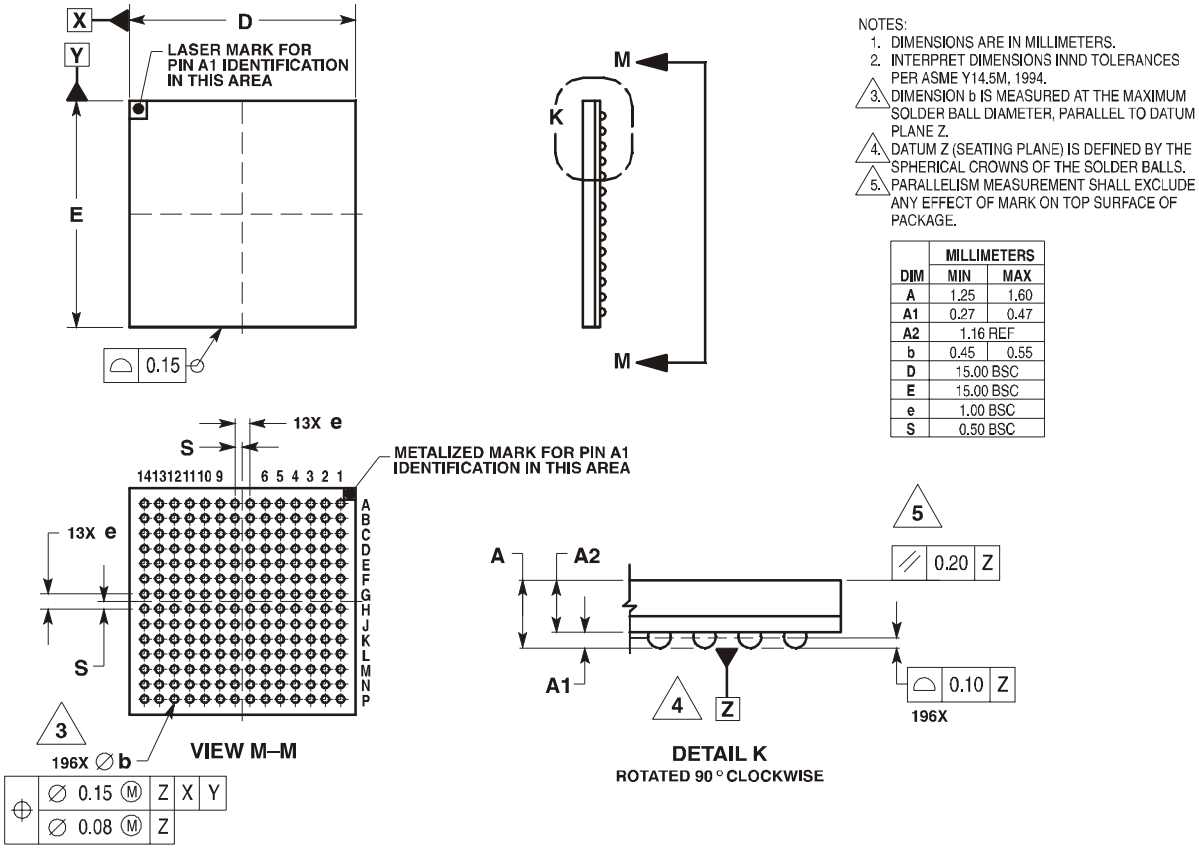


Figure 2-28. Write Timing Diagram, Multiplexed Bus, Double Data Strobe

3.2 MAP-BGA Package Mechanical Drawing



CASE 1128C–01
ISSUE O

DATE 07/28/98

Figure 3-3. DSP56311 Mechanical Information, 196-pin MAP-BGA Package

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to the point at which the leads attach to the case.
- If the temperature of the package case (T_T) is determined by a thermocouple, thermal resistance is computed from the value obtained by the equation $(T_J - T_T)/P_D$.

As noted earlier, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable to determine the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, the use of the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will yield an estimate of a junction temperature slightly higher than actual temperature. Hence, the new thermal metric, thermal characterization parameter or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when the surface temperature of the package is used. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

4.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}).

Use the following list of recommendations to ensure correct DSP operation.

- Provide a low-impedance path from the board power supply to each V_{CC} pin on the DSP and from the board ground to each GND pin.
- Use at least four 0.01–0.1 µF bypass capacitors for the core and PLL power and six 0.01–0.1 µF bypass capacitors for I/O power positioned as closely as possible to the four sides of the package to connect the V_{CC} power source to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{CC} and GND pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer PCB with two inner layers for V_{CC} and GND.

4.4.2 Phase Jitter Performance

The phase jitter of the PLL is defined as the variations in the skew between the falling edges of EXTAL and CLKOUT for a given device in specific temperature, voltage, input frequency, MF, and capacitive load on CLKOUT. These variations are a result of the PLL locking mechanism. For input frequencies greater than 15 MHz and MF ≤4, this jitter is less than ±0.6 ns; otherwise, this jitter is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this jitter is less than ±2 ns.

4.4.3 Frequency Jitter Performance

The frequency jitter of the PLL is defined as the variation of the frequency of CLKOUT. For small MF (MF < 10) this jitter is smaller than 0.5 percent. For mid-range MF (10 < MF < 500) this jitter is between 0.5 percent and approximately 2 percent. For large MF (MF > 500), the frequency jitter is 2–3 percent.

4.5 Input (EXTAL) Jitter Requirements

The allowed jitter on the frequency of EXTAL is 0.5 percent. If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time), then the allowed jitter can be 2 percent. The phase and frequency jitter performance results are valid only if the input jitter is less than the prescribed values.

```
;       SCI Clock Control Register

M_CD EQU $FFF                          ; Clock Divider Mask (CD0-CD11)
M_COD EQU 12                           ; Clock Out Divider
M_SCP EQU 13                           ; Clock Prescaler
M_RCM EQU 14                           ; Receive Clock Mode Source Bit
M_TCM EQU 15                           ; Transmit Clock Source Bit

;------------------------------------------------------------------------
;
;       EQUATES for Synchronous Serial Interface (SSI)
;
;------------------------------------------------------------------------

;
;       Register Addresses Of SSI0
M_TX00 EQU $FFFFBC                     ; SSI0 Transmit Data Register 0
M_TX01 EQU $FFFFBB                     ; SSIO Transmit Data Register 1
M_TX02 EQU $FFFFBA                     ; SSIO Transmit Data Register 2
M_TSR0 EQU $FFFFB9                     ; SSI0 Time Slot Register
M_RX0 EQU $FFFFB8                      ; SSI0 Receive Data Register
M_SSISR0 EQU $FFFFB7                   ; SSI0 Status Register
M_CRB0 EQU $FFFFB6                     ; SSI0 Control Register B
M_CRA0 EQU $FFFFB5                     ; SSI0 Control Register A
M_TSMA0 EQU $FFFFB4                    ; SSI0 Transmit Slot Mask Register A
M_TSMB0 EQU $FFFFB3                    ; SSI0 Transmit Slot Mask Register B
M_RSMA0 EQU $FFFFB2                    ; SSI0 Receive Slot Mask Register A
M_RSMB0 EQU $FFFFB1                    ; SSI0 Receive Slot Mask Register B

;       Register Addresses Of SSI1
M_TX10 EQU $FFFFAC                     ; SSI1 Transmit Data Register 0
M_TX11 EQU $FFFFAB                     ; SSI1 Transmit Data Register 1
M_TX12 EQU $FFFFAA                     ; SSI1 Transmit Data Register 2
M_TSR1 EQU $FFFFA9                     ; SSI1 Time Slot Register
M_RX1 EQU $FFFFA8                      ; SSI1 Receive Data Register
M_SSISR1 EQU $FFFFA7                   ; SSI1 Status Register
M_CRB1 EQU $FFFFA6                     ; SSI1 Control Register B
M_CRA1 EQU $FFFFA5                     ; SSI1 Control Register A
M_TSMA1 EQU $FFFFA4                    ; SSI1 Transmit Slot Mask Register A
M_TSMB1 EQU $FFFFA3                    ; SSI1 Transmit Slot Mask Register B
M_RSMA1 EQU $FFFFA2                    ; SSI1 Receive Slot Mask Register A
M_RSMB1 EQU $FFFFA1                    ; SSI1 Receive Slot Mask Register B

;       SSI Control Register A Bit Flags

M_PM EQU $FF                           ; Prescale Modulus Select Mask (PM0-PM7)
M_PSR EQU 11                           ; Prescaler Range
M_DC EQU $1F000                        ; Frame Rate Divider Control Mask (DC0-DC7)
M_ALC EQU 18                           ; Alignment Control (ALC)
M_WL EQU $380000                       ; Word Length Control Mask (WL0-WL7)
M_SSC1 EQU 22                          ; Select SC1 as TR #0 drive enable (SSC1)

;       SSI Control Register B Bit Flags

M_OF EQU $3                            ; Serial Output Flag Mask
M_OF0 EQU 0                            ; Serial Output Flag 0
M_OF1 EQU 1                            ; Serial Output Flag 1
M_SCD EQU $1C                          ; Serial Control Direction Mask
M_SCD0 EQU 2                           ; Serial Control 0 Direction
M_SCD1 EQU 3                           ; Serial Control 1 Direction
M_SCD2 EQU 4                           ; Serial Control 2 Direction
M_SCKD EQU 5                           ; Clock Source Direction
```

```
I_VEC EQU $0
       endif

;------------------------------------------------------------------------
; Non-Maskable interrupts
;------------------------------------------------------------------------
I_RESET EQU I_VEC+$00               ; Hardware RESET
I_STACK EQU I_VEC+$02               ; Stack Error
I_ILL EQU I_VEC+$04                 ; Illegal Instruction
I_DBG EQU I_VEC+$06                 ; Debug Request
I_TRAP EQU I_VEC+$08                ; Trap
I_NMI EQU I_VEC+$0A                 ; Non Maskable Interrupt

;------------------------------------------------------------------------
; Interrupt Request Pins
;------------------------------------------------------------------------
I_IRQA EQU I_VEC+$10                ; IRQA
I_IRQB EQU I_VEC+$12                ; IRQB
I_IRQC EQU I_VEC+$14                ; IRQC
I_IRQD EQU I_VEC+$16                ; IRQD

;------------------------------------------------------------------------
; DMA Interrupts
;------------------------------------------------------------------------
I_DMA0 EQU I_VEC+$18                ; DMA Channel 0
I_DMA1 EQU I_VEC+$1A                ; DMA Channel 1
I_DMA2 EQU I_VEC+$1C                ; DMA Channel 2
I_DMA3 EQU I_VEC+$1E                ; DMA Channel 3
I_DMA4 EQU I_VEC+$20                ; DMA Channel 4
I_DMA5 EQU I_VEC+$22                ; DMA Channel 5

;------------------------------------------------------------------------
; Timer Interrupts
;------------------------------------------------------------------------
I_TIM0C EQU I_VEC+$24               ; TIMER 0 compare
I_TIM0OF EQU I_VEC+$26              ; TIMER 0 overflow
I_TIM1C EQU I_VEC+$28               ; TIMER 1 compare
I_TIM1OF EQU I_VEC+$2A              ; TIMER 1 overflow
I_TIM2C EQU I_VEC+$2C               ; TIMER 2 compare
I_TIM2OF EQU I_VEC+$2E              ; TIMER 2 overflow

;------------------------------------------------------------------------
; ESSI Interrupts
;------------------------------------------------------------------------
I_SI0RD EQU I_VEC+$30               ; ESSI0 Receive Data
I_SI0RDE EQU I_VEC+$32              ; ESSI0 Receive Data w/ exception Status
I_SI0RLS EQU I_VEC+$34              ; ESSI0 Receive last slot
I_SI0TD EQU I_VEC+$36               ; ESSI0 Transmit data
I_SI0TDE EQU I_VEC+$38              ; ESSI0 Transmit Data w/ exception Status
I_SI0TLS EQU I_VEC+$3A              ; ESSI0 Transmit last slot
I_SI1RD EQU I_VEC+$40               ; ESSI1 Receive Data
I_SI1RDE EQU I_VEC+$42              ; ESSI1 Receive Data w/ exception Status
I_SI1RLS EQU I_VEC+$44              ; ESSI1 Receive last slot
I_SI1TD EQU I_VEC+$46               ; ESSI1 Transmit data
I_SI1TDE EQU I_VEC+$48              ; ESSI1 Transmit Data w/ exception Status
I_SI1TLS EQU I_VEC+$4A              ; ESSI1 Transmit last slot

;------------------------------------------------------------------------
; SCI Interrupts
;------------------------------------------------------------------------
I_SCIRD EQU I_VEC+$50               ; SCI Receive Data
I_SCIRDE EQU I_VEC+$52              ; SCI Receive Data With Exception Status
I_SCITD EQU I_VEC+$54               ; SCI Transmit Data
```