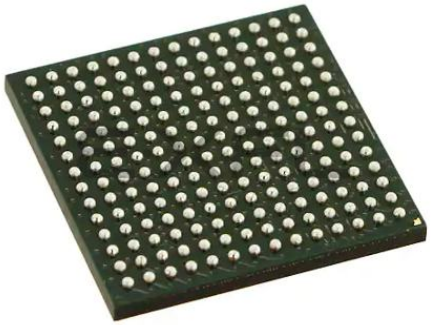

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	150MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56311vl150r2

1.7 Host Interface (HI08)

The HI08 provides a fast, 8-bit, parallel data port that connects directly to the host bus. The HI08 supports a variety of standard buses and connects directly to a number of industry-standard microcomputers, microprocessors, DSPs, and DMA hardware.

1.7.1 Host Port Usage Considerations

Careful synchronization is required when the system reads multiple-bit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected (as they are in the Host port). The considerations for proper operation are discussed in **Table 1-10**.

Table 1-10. Host Port Usage Considerations

Action	Description
Asynchronous read of receive byte registers	When reading the receive byte registers, Receive register High (RXH), Receive register Middle (RXM), or Receive register Low (RXL), the host interface programmer should use interrupts or poll the Receive register Data Full (RXDF) flag that indicates data is available. This assures that the data in the receive byte registers is valid.
Asynchronous write to transmit byte registers	The host interface programmer should not write to the transmit byte registers, Transmit register High (TXH), Transmit register Middle (TXM), or Transmit register Low (TXL), unless the Transmit register Data Empty (TXDE) bit is set indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers transfer valid data to the Host Receive (HRX) register.
Asynchronous write to host vector	The host interface programmer must change the Host Vector (HV) register only when the Host Command bit (HC) is clear. This practice guarantees that the DSP interrupt control logic receives a stable vector.

1.7.2 Host Port Configuration

HI08 signal functions vary according to the programmed configuration of the interface as determined by the 16 bits in the HI08 Port Control Register.

Table 1-11. Host Interface

Signal Name	Type	State During Reset[1,2]	Signal Description
H[0–7]	Input/Output	Ignored Input	**Host Data—**When the HI08 is programmed to interface with a non-multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the bidirectional Data bus.
HAD[0–7]	Input/Output		**Host Address—**When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the bidirectional multiplexed Address/Data bus.
PB[0–7]	Input or Output		**Port B 0–7—**When the HI08 is configured as GPIO through the HI08 Port Control Register, these signals are individually programmed as inputs or outputs through the HI08 Data Direction Register.

2.2 Thermal Characteristics

Table 2-2. Thermal Characteristics

Thermal Resistance Characteristic	Symbol	MAP-BGA Value	Unit
Junction-to-ambient, natural convection, single-layer board (1s)[1,2]	$R_{\theta JA}$	49	°C/W
Junction-to-ambient, natural convection, four-layer board (2s2p)[1,3]	$R_{\theta JMA}$	26	°C/W
Junction-to-ambient, @200 ft/min air flow, single layer board (1s)[1,3]	$R_{\theta JMA}$	39	°C/W
Junction-to-ambient, @200 ft/min air flow, four-layer board (2s2p)[1,3]	$R_{\theta JMA}$	22	°C/W
Junction-to-board[4]	$R_{\theta JB}$	14	°C/W
Junction-to-case thermal resistance[5]	$R_{\theta JC}$	5	°C/W
Junction-to-package-top, natural convection[6]	Ψ_{JT}	2	°C/W
Junction-to-package-top, @200 ft/min air flow[6]	Ψ_{JT}	2	°C/W

Notes:
1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Table 2-5. Clock Operation

No.	Characteristics	Symbol	150 MHz	
			Min	Max
1	Frequency of EXTAL (EXTAL Pin Frequency) The rise and fall time of this external clock should be 3 ns maximum.	Ef	0	150.0
2	EXTAL input high[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[6]) • With PLL enabled (42.5%–57.5% duty cycle[6])	ET_H	 3.11 ns 2.83 ns	 ∞ 157.0 µs
3	EXTAL input low[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[6]) • With PLL enabled (42.5%–57.5% duty cycle[6])	ET_L	 3.11 ns 2.83 ns	 ∞ 157.0 µs
4	EXTAL cycle time[2] • With PLL disabled • With PLL enabled	ET_C	 6.67 ns 6.67 ns	 ∞ 273.1 µs
5	Internal clock change from EXTAL fall with PLL disabled		4.3 ns	11.0 ns
6	a.Internal clock rising edge from EXTAL rising edge with PLL enabled (MF = 1 or 2 or 4, PDF = 1, Ef > 15 MHz)[3,5] b. Internal clock falling edge from EXTAL falling edge with PLL enabled (MF ≤4, PDF ≠ 1, Ef / PDF > 15 MHz)[3,5]		0.0 ns 0.0 ns	1.8 ns 1.8 ns
7	Instruction cycle time = I_{CYC} = T_C[4] (see **Figure 2-4**) (46.7%–53.3% duty cycle) • With PLL disabled • With PLL enabled	I_{CYC}	 13.33 ns 6.7 ns	 ∞ 8.53 µs

Notes:
1. Measured at 50 percent of the input transition.
2. The maximum value for PLL enabled is given for minimum VCO frequency (see **Table 2-4**) and maximum MF.
3. Periodically sampled and not 100 percent tested.
4. The maximum value for PLL enabled is given for minimum VCO frequency and maximum DF.
5. The skew is not guaranteed for any other MF value.
6. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correction operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

2.4.3 Phase Lock Loop (PLL) Characteristics

Table 2-6. PLL Characteristics

Characteristics	150 MHz		Unit
	Min	Max	
Voltage Controlled Oscillator (VCO) frequency when PLL enabled (MF × E_f × 2/PDF)	30	300	MHz
PLL external capacitor (PCAP pin to V_{CCP}) (C_{PCAP}[1]) • @ MF ≤4 • @ MF > 4	 (580 × MF) –100 830 × MF	 (780 × MF) –140 1470 × MF	 pF pF

Note: C_{PCAP} is the value of the PLL capacitor (connected between the PCAP pin and V_{CCP}) computed using the appropriate expression listed above.

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	150 MHz		Unit
			Min	Max	
26	Duration of level sensitive $\overline{\text{IRQA}}$ assertion to ensure interrupt service (when exiting Stop)[2, 3]				
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (Operating Mode Register Bit 6 = 0)	Minimum: $PLC \times ET_C \times PDF + (128K - PLC/2) \times T_C$	13.6	—	ms
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (Operating Mode Register Bit 6 = 1)	$PLC \times ET_C \times PDF + (20.5 \pm 0.5) \times T_C$	12.3	—	ms
	• PLL is active during Stop (PCTL Bit 17 = 1) (implies no Stop delay)	$5.5 \times T_C$	36.7	—	ns
27	Interrupt Request Rate	Maximum:			
	• HI08, ESSI, SCI, Timer	$12 \times T_C$	—	80.0	ns
	• DMA	$8 \times T_C$	—	53.3	ns
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger)	$8 \times T_C$	—	53.3	ns
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (level trigger)	$12 \times T_C$	—	80.0	ns
28	DMA Request Rate	Maximum:			
	• Data read from HI08, ESSI, SCI	$6 \times T_C$	—	40.0	ns
	• Data write to HI08, ESSI, SCI	$7 \times T_C$	—	46.7	ns
	• Timer	$2 \times T_C$	—	13.3	ns
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger)	$3 \times T_C$	—	20.0	ns
29	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory (DMA source) access address out valid	Minimum: $4.25 \times T_C + 2.0$	30.3	—	ns

Notes:

1. When fast interrupts are used and $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, and $\overline{\text{IRQD}}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when fast interrupts are used. Long interrupts are recommended for Level-sensitive mode.
2. This timing depends on several settings:
   • For PLL disable, using internal oscillator (PLL Control Register (PCTL) Bit 16 = 0) and oscillator disabled during Stop (PCTL Bit 17 = 0), a stabilization delay is required to assure that the oscillator is stable before programs are executed. Resetting the Stop delay (Operating Mode Register Bit 6 = 0) provides the proper delay. While Operating Mode Register Bit 6 = 1 can be set, it is not recommended, and these specifications do not guarantee timings for that case.
   • For PLL disable, using internal oscillator (PCTL Bit 16 = 0) and oscillator enabled during Stop (PCTL Bit 17=1), no stabilization delay is required and recovery is minimal (Operating Mode Register Bit 6 setting is ignored).
   • For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time is defined by the PCTL Bit 17 and Operating Mode Register Bit 6 settings.
   • For PLL enable, if PCTL Bit 17 is 0, the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0 to 1000 cycles. This procedure occurs in parallel with the stop delay counter, and stop recovery ends when the last of these two events occurs. The stop delay counter completes count or PLL lock procedure completion.
   • PLC value for PLL disable is 0.
   • The maximum value for ET_C is 4096 (maximum MF) divided by the desired internal frequency (that is, for 66 MHz it is 4096/66 MHz = 62 µs). During the stabilization period, T_C, T_H, and T_L is not constant, and their width may vary, so timing may vary as well.
3. Periodically sampled and not 100 percent tested.
4. Value depends on clock source:
   • For an external clock generator, $\overline{\text{RESET}}$ duration is measured while $\overline{\text{RESET}}$ is asserted, V_{CC} is valid, and the EXTAL input is active and valid.
   • For an internal oscillator, $\overline{\text{RESET}}$ duration is measured while $\overline{\text{RESET}}$ is asserted and V_{CC} is valid. The specified timing reflects the crystal oscillator stabilization time after power-up. This number is affected both by the specifications of the crystal and other components connected to the oscillator and reflects worst case conditions.
   • When the V_{CC} is valid, but the other "required $\overline{\text{RESET}}$ duration" conditions (as specified above) have not been yet met, the device circuitry is in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.
5. If PLL does not lose lock.
6. V_{CCQH} = 3.3 V ±0.3 V, V_{CC} = 1.8 V ±0.1 V; T_J = –40°C to +100°C, C_L = 50 pF.
7. WS = number of wait states (measured in clock cycles, number of T_C).
8. Use expression to compute maximum value.

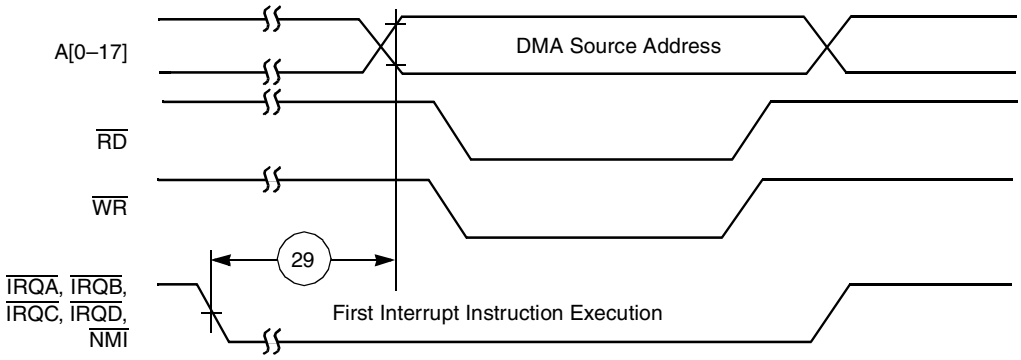

Figure 2-9. External Memory Access (DMA Source) Timing

2.4.5 External Memory Expansion Port (Port A)

2.4.5.1 SRAM Timing

Table 2-8. SRAM Timing

No.	Characteristics	Symbol	Expression[1]	150 MHz		Unit
				Min	Max	
100	Address valid and AA assertion pulse width[2]	t_{RC}, t_{WC}	(WS + 2) × T_C –4.0 [2 ≤WS ≤7] (WS + 3) × T_C –4.0 [WS ≥ 8]	22.7 69.3	— —	ns ns
101	Address and AA valid to $\overline{WR}$ assertion	t_{AS}	0.75 × T_C – 3.0 [2 ≤WS ≤3] 1.25 × T_C – 3.0 [WS ≥ 4]	2.0 5.3	— —	ns ns
102	$\overline{WR}$ assertion pulse width	t_{WP}	WS × T_C –4.0 [2 ≤WS ≤3] (WS –0.5) × T_C –4.0 [WS ≥ 4]	9.3 19.3	— —	ns ns
103	$\overline{WR}$ deassertion to address not valid	t_{WR}	1.25 × T_C –4.0 [2 ≤WS ≤7] 2.25 × T_C –4.0 [WS ≥ 8]	4.3 11.0	— —	ns ns
104	Address and AA valid to input data valid	t_{AA}, t_{AC}	(WS + 0.75) × T_C –6.5 [WS ≥ 2]	—	11.8	ns
105	$\overline{RD}$ assertion to input data valid	t_{OE}	(WS + 0.25) × T_C –6.5 [WS ≥ 2]	—	8.5	ns
106	$\overline{RD}$ deassertion to data not valid (data hold time)	t_{OHZ}		0.0	—	ns
107	Address valid to $\overline{WR}$ deassertion[2]	t_{AW}	(WS + 0.75) × T_C –4.0 [WS ≥ 2]	14.3	—	ns
108	Data valid to $\overline{WR}$ deassertion (data set-up time)	t_{DS} (t_{DW})	(WS –0.25) × T_C –5.4 [WS ≥ 2]	6.3	—	ns
109	Data hold time from $\overline{WR}$ deassertion	t_{DH}	1.25 × T_C –4.0 [2 ≤WS ≤7] 2.25 × T_C –4.0 [WS ≥ 8]	4.3 11.0	— —	ns ns
110	$\overline{WR}$ assertion to data active	—	0.25 × T_C –4.0 [2 ≤WS ≤3] –0.25 × T_C –4.0 [WS ≥ 4]	–2.4 –5.7	— —	ns ns

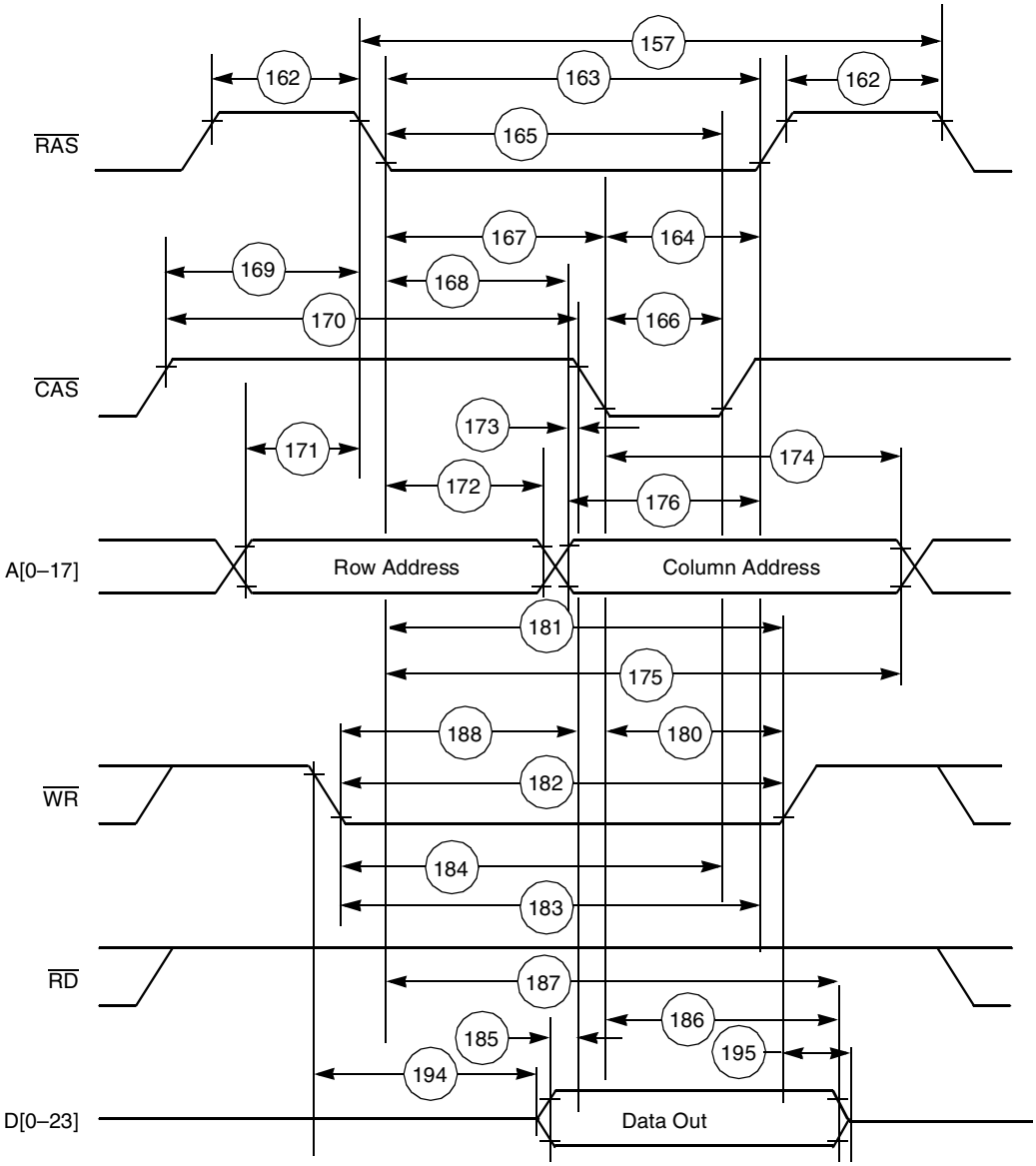

Figure 2-17. DRAM Out-of-Page Write Access

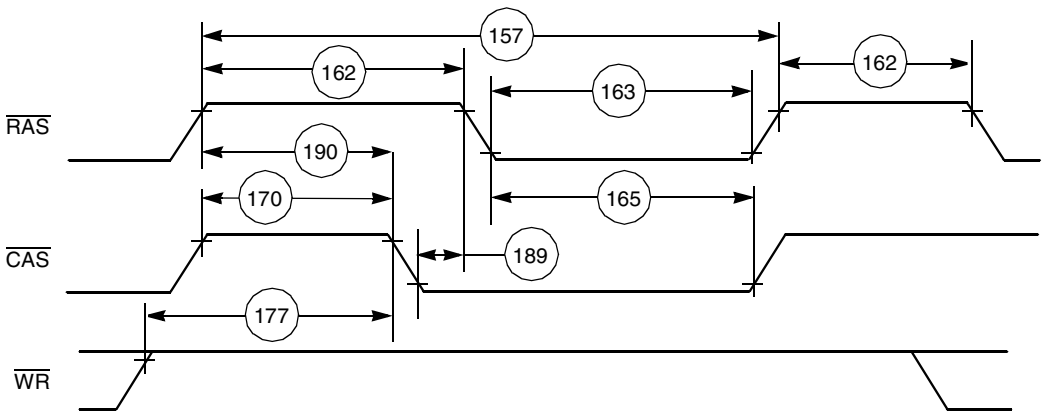

Figure 2-18. DRAM Refresh Access

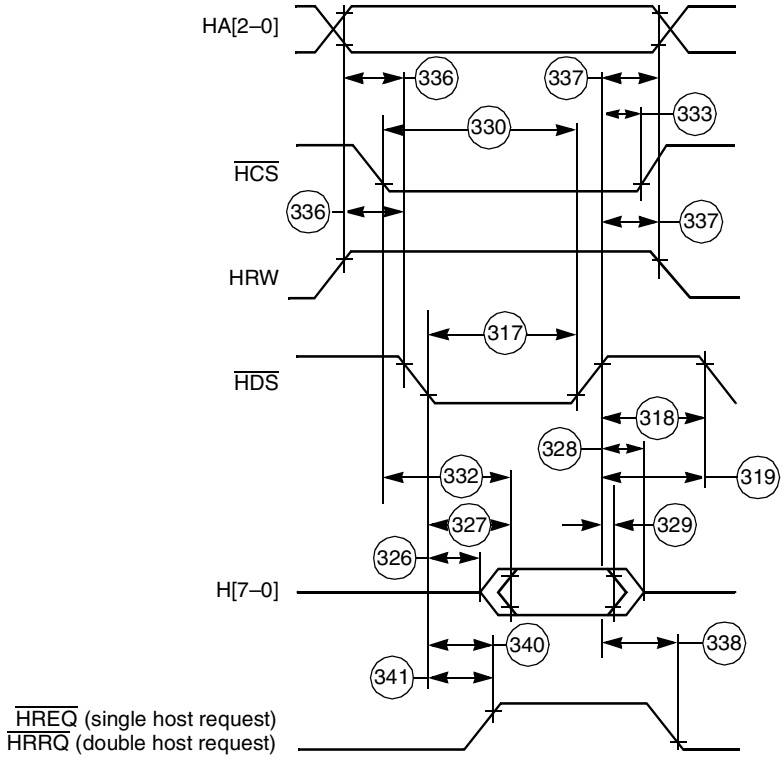

Figure 2-21. Read Timing Diagram, Non-Multiplexed Bus, Single Data Strobe

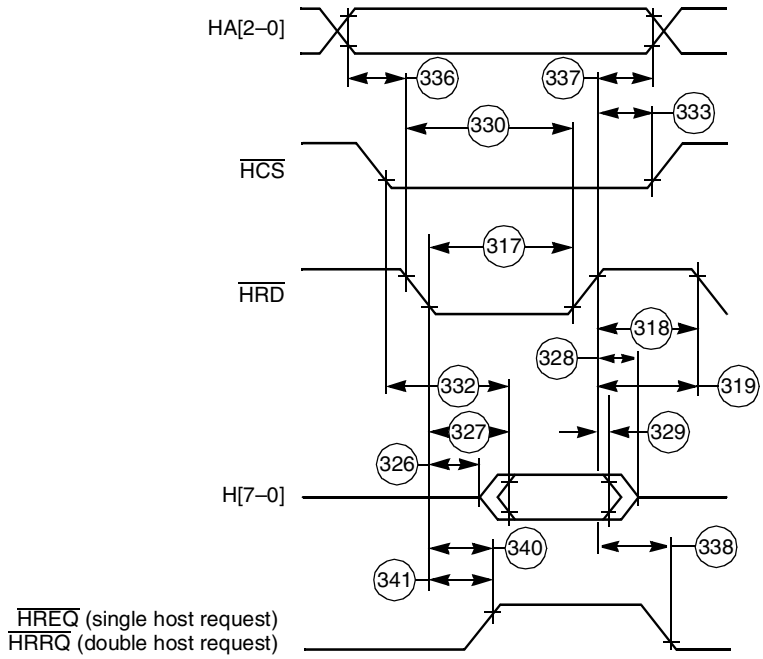

Figure 2-22. Read Timing Diagram, Non-Multiplexed Bus, Double Data Strobe

Table 2-16. ESSI Timings (Continued)

No.	Characteristics[4, 6]	Symbol	Expression	150 MHz		Cond-ition[5]	Unit
				Min	Max		
451	TXC rising edge to FST out (word-length) low			— —	31.0 17.0	x ck i ck	ns
452	TXC rising edge to data out enable from high impedance			— —	31.0 17.0	x ck i ck	ns
453	TXC rising edge to transmitter 0 drive enable assertion			— —	34.0 20.0	x ck i ck	ns
454	TXC rising edge to data out valid		$35 + 0.5 \times T_C$	— —	38.4 21.0	x ck i ck	ns
455	TXC rising edge to data out high impedance[3]			— —	31.0 16.0	x ck i ck	ns
456	TXC rising edge to transmitter 0 drive enable deassertion[3]			— —	34.0 20.0	x ck i ck	ns
457	FST input (bl, wr)[6] set-up time before TXC falling edge[2]			2.0 21.0	— —	x ck i ck	ns
458	FST input (wl)[6] to data out enable from high impedance			—	27.0	—	ns
459	FST input (wl) to transmitter 0 drive enable assertion			—	31.0	—	ns
460	FST input (wl)[6] set-up time before TXC falling edge			2.5 21.0	— —	x ck i ck	ns
461	FST input hold time after TXC falling edge			4.0 0.0	— —	x ck i ck	ns
462	Flag output valid after TXC rising edge			— —	32.0 18.0	x ck i ck	ns

Notes:
1. For the internal clock, the external clock cycle is defined by the instruction cycle time (timing 7 in **Table 2-5** on page 2-6) and the ESSI Control Register.
2. The word-length-relative frame sync signal waveform operates the same way as the bit-length frame sync signal waveform, but spreads from one serial clock before the first bit clock (same as the Bit Length Frame Sync signal) until the one before last bit clock of the first word in the frame.
3. Periodically sampled and not 100 percent tested
4. V_{CCQH} = 3.3 V ± 0.3 V, V_{CC} = 1.8 V ± 0.1 V; T_J = –40°C to +100 °C, C_L = 50 pF.
5. TXC (SCK Pin) = transmit clock
   RXC (SC0 or SCK pin) = receive clock
   FST (SC2 pin) = transmit frame sync
   FSR (SC1 or SC2 pin) receive frame sync
6. i ck = Internal Clock; x ck = external clock
   i ck a = internal clock, Asynchronous mode (asynchronous implies that TXC and RXC are two different clocks)
   i ck s = internal clock, Synchronous mode (synchronous implies that TXC and RXC are the same clock)
   bl = bit length
   wl = word length
   wr = word length relative

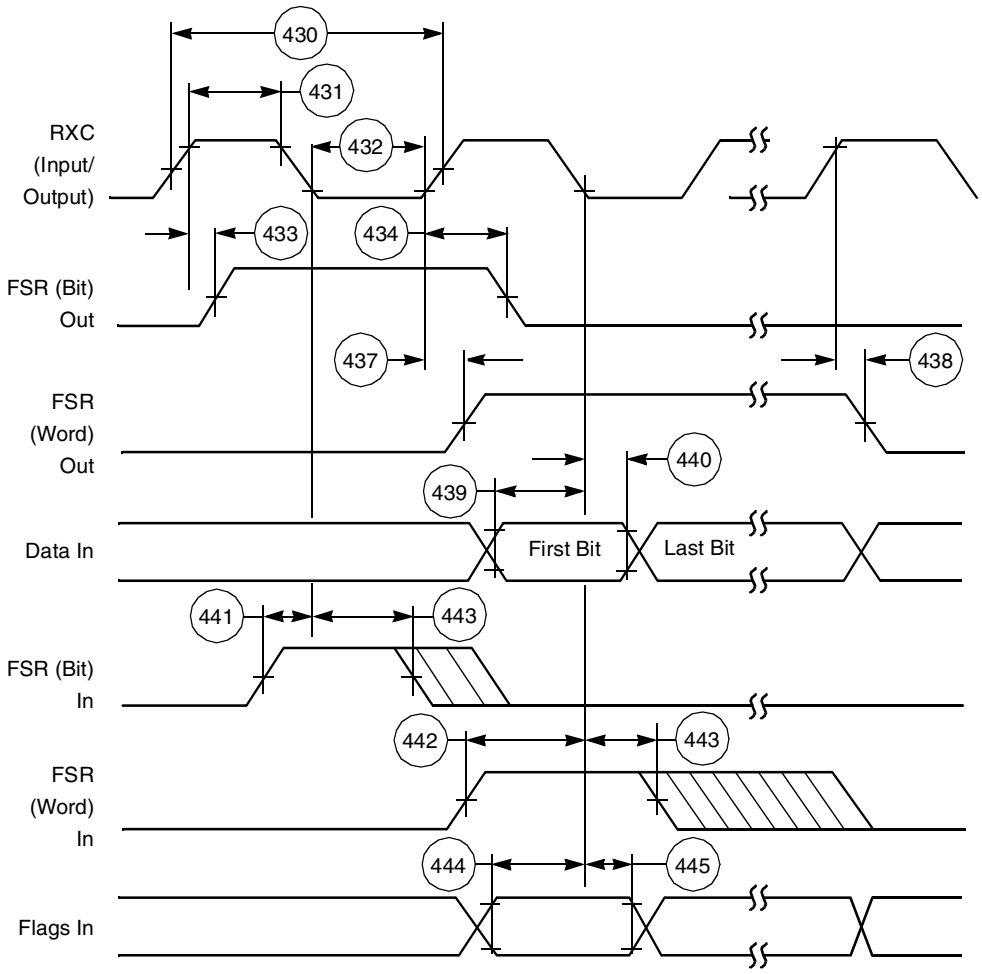

Figure 2-32. ESSI Receiver Timing

2.4.9 Timer Timing

Table 2-17. Timer Timing

No.	Characteristics	Expression	150 MHz		Unit
			Min	Max	
480	TIO Low	$2 \times T_C + 2.0$	15.4	—	ns
481	TIO High	$2 \times T_C + 2.0$	15.4	—	ns
Note:	V_{CCQH} = 3.3 V ± 0.3 V, V_{CC} = 1.8 V ± 0.1 V; T_J = –40°C to +100 °C, C_L = 50 pF				

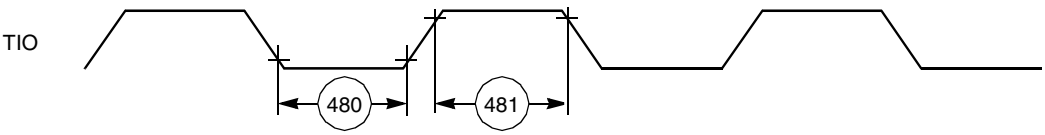

Figure 2-33. TIO Timer Event Input Restrictions

Table 3-1. Signal List by Ball Number

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
A1	Not Connected (NC), reserved	B12	D8	D9	GND
A2	SC11 or PD1	B13	D5	D10	GND
A3	TMS	B14	NC	D11	GND
A4	TDO	C1	SC02 or PC2	D12	D1
A5	MODB/$\overline{\text{IRQB}}$	C2	STD1 or PD5	D13	D2
A6	D23	C3	TCK	D14	V_{CCD}
A7	V_{CCD}	C4	MODA/$\overline{\text{IRQA}}$	E1	STD0 or PC5
A8	D19	C5	MODC/$\overline{\text{IRQC}}$	E2	V_{CCS}
A9	D16	C6	D22	E3	SRD0 or PC4
A10	D14	C7	V_{CCQL}	E4	GND
A11	D11	C8	D18	E5	GND
A12	D9	C9	V_{CCD}	E6	GND
A13	D7	C10	D12	E7	GND
A14	NC	C11	V_{CCD}	E8	GND
B1	SRD1 or PD4	C12	D6	E9	GND
B2	SC12 or PD2	C13	D3	E10	GND
B3	TDI	C14	D4	E11	GND
B4	$\overline{\text{TRST}}$	D1	PINIT/$\overline{\text{NMI}}$	E12	A17
B5	MODD/$\overline{\text{IRQD}}$	D2	SC01 or PC1	E13	A16
B6	D21	D3	DE	E14	D0
B7	D20	D4	GND	F1	RXD or PE0
B8	D17	D5	GND	F2	SC10 or PD0
B9	D15	D6	GND	F3	SC00 or PC0
B10	D13	D7	GND	F4	GND
B11	D10	D8	GND	F5	GND

Table 3-2. Signal List by Signal Name

Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.
A0	N14	$\overline{BR}$	N11	D9	A12
A1	M13	$\overline{CAS}$	N8	$\overline{DE}$	D3
A10	H13	CLKOUT	M9	EXTAL	M8
A11	H14	D0	E14	GND	D4
A12	G14	D1	D12	GND	D5
A13	G12	D10	B11	GND	D6
A14	F13	D11	A11	GND	D7
A15	F14	D12	C10	GND	D8
A16	E13	D13	B10	GND	D9
A17	E12	D14	A10	GND	D10
A2	M14	D15	B9	GND	D11
A3	L13	D16	A9	GND	E4
A4	L14	D17	B8	GND	E5
A5	K13	D18	C8	GND	E6
A6	K14	D19	A8	GND	E7
A7	J13	D2	D13	GND	E8
A8	J12	D20	B7	GND	E9
A9	J14	D21	B6	GND	E10
AA0	N13	D22	C6	GND	E11
AA1	P12	D23	A6	GND	F4
AA2	P7	D3	C13	GND	F5
AA3	N7	D4	C14	GND	F6
$\overline{BB}$	P11	D5	B13	GND	F7
$\overline{BCLK}$	M10	D6	C12	GND	F8
BCLK	N10	D7	A13	GND	F9
$\overline{BG}$	P13	D8	B12	GND	F10

Power Consumption Benchmark A

The following benchmark program evaluates DSP56311 power use in a test situation. It enables the PLL, disables the external clock, and uses repeated multiply-accumulate (MAC) instructions with a set of synthetic DSP application data to emulate intensive sustained DSP operation.

```
;************************************************************************
;************************************************************************
;*                                                                      *
;*                    CHECKS   Typical Power Consumption                *
;*                                                                      *
;************************************************************************

        page    200,55,0,0,0
        nolist

I_VEC EQU $000000                   ; Interrupt vectors for program debug only
START EQU $8000                     ; MAIN (external) program starting address
INT_PROG  EQU $100                  ; INTERNAL program memory starting address
INT_XDAT  EQU $0                    ; INTERNAL X-data memory starting address
INT_YDAT  EQU $0                    ; INTERNAL Y-data memory starting address

        INCLUDE "ioequ.asm"
        INCLUDE "intequ.asm"

        list

        org     P:START
;
        movep #$0243FF,x:M_BCR ;    ; BCR: Area 3 = 2 w.s (SRAM)
                                    ; Default: 2w.s (SRAM)
;
        movep   #$0d0000,x:M_PCTL   ; XTAL disable
                                    ; PLL enable
                                    ; CLKOUT disable
;
                                    ; Load the program
;
        move    #INT_PROG,r0
        move    #PROG_START,r1
        do      #(PROG_END-PROG_START),PLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,p:(r0)+
        nop
PLOAD_LOOP
;
                                    ; Load the X-data
;
        move    #INT_XDAT,r0
        move    #XDAT_START,r1
        do      #(XDAT_END-XDAT_START),XLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,x:(r0)+
```

```
XLOAD_LOOP
;
; Load the Y-data
;
        move    #INT_YDAT,r0
        move    #YDAT_START,r1
        do      #(YDAT_END-YDAT_START),YLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,y:(r0)+
YLOAD_LOOP
;

        jmp     INT_PROG

PROG_START
        move    #$0,r0
        move    #$0,r4
        move    #$3f,m0
        move    #$3f,m4
;
        clr     a
        clr     b
        move    #$0,x0
        move    #$0,x1
        move    #$0,y0
        move    #$0,y1
        bset    #4,omr                  ; ebd
;
sbr     dor     #60,_end
        mac     x0,y0,ax:(r0)+,x1     y:(r4)+,y1
        mac     x1,y1,ax:(r0)+,x0     y:(r4)+,y0
        add     a,b
        mac     x0,y0,ax:(r0)+,x1
        mac     x1,y1,a               y:(r4)+,y0
        move    b1,x:$ff
_end
        bra     sbr
        nop
        nop
        nop
        nop
PROG_END
        nop
        nop


XDAT_START
;       org     x:0
        dc      $262EB9
        dc      $86F2FE
        dc      $E56A5F
        dc      $616CAC
        dc      $8FFD75
        dc      $9210A
        dc      $A06D7B
        dc      $CEA798
        dc      $8DFBF1
        dc      $A063D6
        dc      $6C6657
        dc      $C2A544
        dc      $A3662D
        dc      $A4E762
        dc      $84F0F3
```

```
        dc      $A43E00
        dc      $C2B639
        dc      $85A47E
        dc      $ABFDDF
        dc      $F3A2C
        dc      $2D7CF5
        dc      $E16A8A
        dc      $ECB8FB
        dc      $4BED18
        dc      $43F371
        dc      $83A556
        dc      $E1E9D7
        dc      $ACA2C4
        dc      $8135AD
        dc      $2CE0E2
        dc      $8F2C73
        dc      $432730
        dc      $A87FA9
        dc      $4A292E
        dc      $A63CCF
        dc      $6BA65C
        dc      $E06D65
        dc      $1AA3A
        dc      $A1B6EB
        dc      $48AC48
        dc      $EF7AE1
        dc      $6E3006
        dc      $62F6C7
        dc      $6064F4
        dc      $87E41D
        dc      $CB2692
        dc      $2C3863
        dc      $C6BC60
        dc      $43A519
        dc      $6139DE
        dc      $ADF7BF
        dc      $4B3E8C
        dc      $6079D5
        dc      $E0F5EA
        dc      $8230DB
        dc      $A3B778
        dc      $2BFE51
        dc      $E0A6B6
        dc      $68FFB7
        dc      $28F324
        dc      $8F2E8D
        dc      $667842
        dc      $83E053
        dc      $A1FD90
        dc      $6B2689
        dc      $85B68E
        dc      $622EAF
        dc      $6162BC
        dc      $E4A245
YDAT_END

;************************************************************************
;
;     EQUATES for DSP56311 I/O registers and ports
;
;     Last update: June 11 1995
;
;************************************************************************
```

```
M_Z EQU 2                           ; Zero
M_N EQU 3                           ; Negative
M_U EQU 4                           ; Unnormalized
M_E EQU 5                           ; Extension
M_L EQU 6                           ; Limit
M_S EQU 7                           ; Scaling Bit
M_I0 EQU 8                          ; Interupt Mask Bit 0
M_I1 EQU 9                          ; Interupt Mask Bit 1
M_S0 EQU 10                         ; Scaling Mode Bit 0
M_S1 EQU 11                         ; Scaling Mode Bit 1
M_SC EQU 13                         ; Sixteen_Bit Compatibility
M_DM EQU 14                         ; Double Precision Multiply
M_LF EQU 15                         ; DO-Loop Flag
M_FV EQU 16                         ; DO-Forever Flag
M_SA EQU 17                         ; Sixteen-Bit Arithmetic
M_CE EQU 19                         ; Instruction Cache Enable
M_SM EQU 20                         ; Arithmetic Saturation
M_RM EQU 21                         ; Rounding Mode
M_CP0 EQU 22                        ; bit 0 of priority bits in SR
M_CP1 EQU 23                        ; bit 1 of priority bits in SR

;       control and status bits in OMR
M_CDP EQU $300                      ; mask for CORE-DMA priority bits in OMR
M_MA    equ0                        ; Operating Mode A
M_MB   equ1                         ; Operating Mode B
M_MC    equ2                        ; Operating Mode C
M_MD    equ3                        ; Operating Mode D
M_EBD EQU 4                         ; External Bus Disable bit in OMR
M_SD EQU 6                          ; Stop Delay
M_MS EQU 7                          ; Memory Switch bit in OMR
M_CDP0 EQU 8                        ; bit 0 of priority bits in OMR
M_CDP1 EQU 9                        ; bit 1 of priority bits in OMR
M_BEN   EQU 10                      ; Burst Enable
M_TAS  EQU 11                       ; TA Synchronize Select
M_BRT  EQU 12                       ; Bus Release Timing
M_ATE EQU 15                        ; Address Tracing Enable bit in OMR.
M_XYS EQU 16                        ; Stack Extension space select bit in OMR.
M_EUN EQU 17                        ; Extensed stack UNderflow flag in OMR.
M_EOV EQU 18                        ; Extended stack OVerflow flag in OMR.
M_WRP EQU 19                        ; Extended WRaP flag in OMR.
M_SEN EQU 20                        ; Stack Extension Enable bit in OMR.




;****************************************************************************
;
;     EQUATES for DSP56311 interrupts
;
;     Last update: June 11 1995
;
;****************************************************************************

       page    132,55,0,0,0
       opt     mex

intequ  ident   1,0

       if      @DEF(I_VEC)
                                    ;leave user definition as is.
       else
```

```
I_VEC EQU $0
       endif

;------------------------------------------------------------------------
; Non-Maskable interrupts
;------------------------------------------------------------------------
I_RESET EQU I_VEC+$00               ; Hardware RESET
I_STACK EQU I_VEC+$02               ; Stack Error
I_ILL EQU I_VEC+$04                 ; Illegal Instruction
I_DBG EQU I_VEC+$06                 ; Debug Request
I_TRAP EQU I_VEC+$08                ; Trap
I_NMI EQU I_VEC+$0A                 ; Non Maskable Interrupt

;------------------------------------------------------------------------
; Interrupt Request Pins
;------------------------------------------------------------------------
I_IRQA EQU I_VEC+$10                ; IRQA
I_IRQB EQU I_VEC+$12                ; IRQB
I_IRQC EQU I_VEC+$14                ; IRQC
I_IRQD EQU I_VEC+$16                ; IRQD

;------------------------------------------------------------------------
; DMA Interrupts
;------------------------------------------------------------------------
I_DMA0 EQU I_VEC+$18                ; DMA Channel 0
I_DMA1 EQU I_VEC+$1A                ; DMA Channel 1
I_DMA2 EQU I_VEC+$1C                ; DMA Channel 2
I_DMA3 EQU I_VEC+$1E                ; DMA Channel 3
I_DMA4 EQU I_VEC+$20                ; DMA Channel 4
I_DMA5 EQU I_VEC+$22                ; DMA Channel 5

;------------------------------------------------------------------------
; Timer Interrupts
;------------------------------------------------------------------------
I_TIM0C EQU I_VEC+$24               ; TIMER 0 compare
I_TIM0OF EQU I_VEC+$26              ; TIMER 0 overflow
I_TIM1C EQU I_VEC+$28               ; TIMER 1 compare
I_TIM1OF EQU I_VEC+$2A              ; TIMER 1 overflow
I_TIM2C EQU I_VEC+$2C               ; TIMER 2 compare
I_TIM2OF EQU I_VEC+$2E              ; TIMER 2 overflow

;------------------------------------------------------------------------
; ESSI Interrupts
;------------------------------------------------------------------------
I_SI0RD EQU I_VEC+$30               ; ESSI0 Receive Data
I_SI0RDE EQU I_VEC+$32              ; ESSI0 Receive Data w/ exception Status
I_SI0RLS EQU I_VEC+$34              ; ESSI0 Receive last slot
I_SI0TD EQU I_VEC+$36               ; ESSI0 Transmit data
I_SI0TDE EQU I_VEC+$38              ; ESSI0 Transmit Data w/ exception Status
I_SI0TLS EQU I_VEC+$3A              ; ESSI0 Transmit last slot
I_SI1RD EQU I_VEC+$40               ; ESSI1 Receive Data
I_SI1RDE EQU I_VEC+$42              ; ESSI1 Receive Data w/ exception Status
I_SI1RLS EQU I_VEC+$44              ; ESSI1 Receive last slot
I_SI1TD EQU I_VEC+$46               ; ESSI1 Transmit data
I_SI1TDE EQU I_VEC+$48              ; ESSI1 Transmit Data w/ exception Status
I_SI1TLS EQU I_VEC+$4A              ; ESSI1 Transmit last slot

;------------------------------------------------------------------------
; SCI Interrupts
;------------------------------------------------------------------------
I_SCIRD EQU I_VEC+$50               ; SCI Receive Data
I_SCIRDE EQU I_VEC+$52              ; SCI Receive Data With Exception Status
I_SCITD EQU I_VEC+$54               ; SCI Transmit Data
```

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