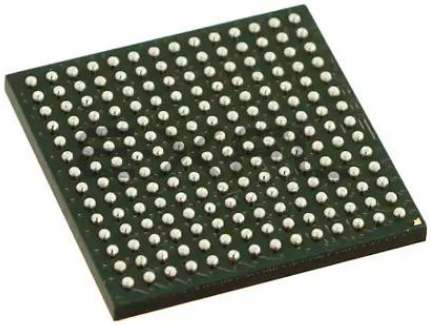

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	150MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spakdsp311vf150

Table 1-11. Host Interface (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
$\overline{\text{HDS}}$/HDS	Input	Ignored Input	**Host Data Strobe**—When the HI08 is programmed to interface with a single-data-strobe host bus and the HI function is selected, this signal is the host data strobe (HDS) Schmitt-trigger input. The polarity of the data strobe is programmable but is configured as active-low ($\overline{\text{HDS}}$) following reset.
$\overline{\text{HWR}}$/HWR	Input		**Host Write Data**—When the HI08 is programmed to interface with a double-data-strobe host bus and the HI function is selected, this signal is the host write data strobe (HWR) Schmitt-trigger input. The polarity of the data strobe is programmable but is configured as active-low ($\overline{\text{HWR}}$) following reset.
PB12	Input or Output		**Port B 12**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
$\overline{\text{HREQ}}$/HREQ	Output	Ignored Input	**Host Request**—When the HI08 is programmed to interface with a single host request host bus and the HI function is selected, this signal is the host request (HREQ) output. The polarity of the host request is programmable but is configured as active-low ($\overline{\text{HREQ}}$) following reset. The host request may be programmed as a driven or open-drain output.
$\overline{\text{HTRQ}}$/HTRQ	Output		**Transmit Host Request**—When the HI08 is programmed to interface with a double host request host bus and the HI function is selected, this signal is the transmit host request (HTRQ) output. The polarity of the host request is programmable but is configured as active-low ($\overline{\text{HTRQ}}$) following reset. The host request may be programmed as a driven or open-drain output.
PB14	Input or Output		**Port B 14**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
$\overline{\text{HACK}}$/HACK	Input	Ignored Input	**Host Acknowledge**—When the HI08 is programmed to interface with a single host request host bus and the HI function is selected, this signal is the host acknowledge (HACK) Schmitt-trigger input. The polarity of the host acknowledge is programmable but is configured as active-low ($\overline{\text{HACK}}$) after reset.
$\overline{\text{HRRQ}}$/HRRQ	Output		**Receive Host Request**—When the HI08 is programmed to interface with a double host request host bus and the HI function is selected, this signal is the receive host request (HRRQ) output. The polarity of the host request is programmable but is configured as active-low ($\overline{\text{HRRQ}}$) after reset. The host request may be programmed as a driven or open-drain output.
PB15	Input or Output		**Port B 15**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

Table 1-12. Enhanced Synchronous Serial Interface 0 (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
STD0	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the Serial Transmit Shift Register. STD0 is an output when data is transmitted.
PC5	Input or Output		**Port C 5**—The default configuration following reset is GPIO input PC5. When configured as PC5, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal STD0 through the Port C Control Register.

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

1.9 Enhanced Synchronous Serial Interface 1 (ESSI1)

Table 1-13. Enhanced Serial Synchronous Interface 1

Signal Name	Type	State During Reset[1,2]	Signal Description
SC10	Input or Output	Ignored Input	**Serial Control 0**—For asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For synchronous mode, this signal is used either for transmitter 1 output or for serial I/O flag 0.
PD0	Input or Output		**Port D 0**—The default configuration following reset is GPIO input PD0. When configured as PD0, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC10 through the Port D Control Register.
SC11	Input/Output	Ignored Input	**Serial Control 1**—For asynchronous mode, this signal is the receiver frame sync I/O. For synchronous mode, this signal is used either for Transmitter 2 output or for Serial I/O Flag 1.
PD1	Input or Output		**Port D 1**—The default configuration following reset is GPIO input PD1. When configured as PD1, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC11 through the Port D Control Register.
SC12	Input/Output	Ignored Input	**Serial Control Signal 2**—The frame sync for both the transmitter and receiver in synchronous mode and for the transmitter only in asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
PD2	Input or Output		**Port D 2**—The default configuration following reset is GPIO input PD2. When configured as PD2, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC12 through the Port D Control Register.

Table 2-5. Clock Operation

No.	Characteristics	Symbol	150 MHz	
			Min	Max
1	Frequency of EXTAL (EXTAL Pin Frequency) The rise and fall time of this external clock should be 3 ns maximum.	Ef	0	150.0
2	EXTAL input high[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[6]) • With PLL enabled (42.5%–57.5% duty cycle[6])	ET_H	 3.11 ns 2.83 ns	 ∞ 157.0 µs
3	EXTAL input low[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[6]) • With PLL enabled (42.5%–57.5% duty cycle[6])	ET_L	 3.11 ns 2.83 ns	 ∞ 157.0 µs
4	EXTAL cycle time[2] • With PLL disabled • With PLL enabled	ET_C	 6.67 ns 6.67 ns	 ∞ 273.1 µs
5	Internal clock change from EXTAL fall with PLL disabled		4.3 ns	11.0 ns
6	a.Internal clock rising edge from EXTAL rising edge with PLL enabled (MF = 1 or 2 or 4, PDF = 1, Ef > 15 MHz)[3,5] b. Internal clock falling edge from EXTAL falling edge with PLL enabled (MF ≤4, PDF ≠ 1, Ef / PDF > 15 MHz)[3,5]		0.0 ns 0.0 ns	1.8 ns 1.8 ns
7	Instruction cycle time = I_{CYC} = T_C[4] (see **Figure 2-4**) (46.7%–53.3% duty cycle) • With PLL disabled • With PLL enabled	I_{CYC}	 13.33 ns 6.7 ns	 ∞ 8.53 µs

Notes:
1. Measured at 50 percent of the input transition.
2. The maximum value for PLL enabled is given for minimum VCO frequency (see **Table 2-4**) and maximum MF.
3. Periodically sampled and not 100 percent tested.
4. The maximum value for PLL enabled is given for minimum VCO frequency and maximum DF.
5. The skew is not guaranteed for any other MF value.
6. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correction operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

2.4.3 Phase Lock Loop (PLL) Characteristics

Table 2-6. PLL Characteristics

Characteristics	150 MHz		Unit
	Min	Max	
Voltage Controlled Oscillator (VCO) frequency when PLL enabled (MF × E_f × 2/PDF)	30	300	MHz
PLL external capacitor (PCAP pin to V_{CCP}) (C_{PCAP}[1]) • @ MF ≤4 • @ MF > 4	 (580 × MF) –100 830 × MF	 (780 × MF) –140 1470 × MF	 pF pF

Note: C_{PCAP} is the value of the PLL capacitor (connected between the PCAP pin and V_{CCP}) computed using the appropriate expression listed above.

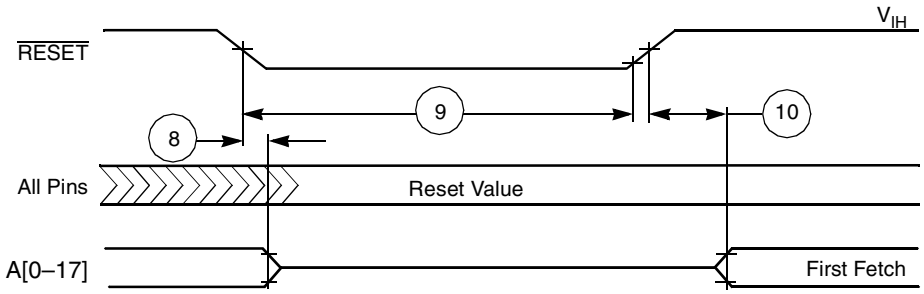
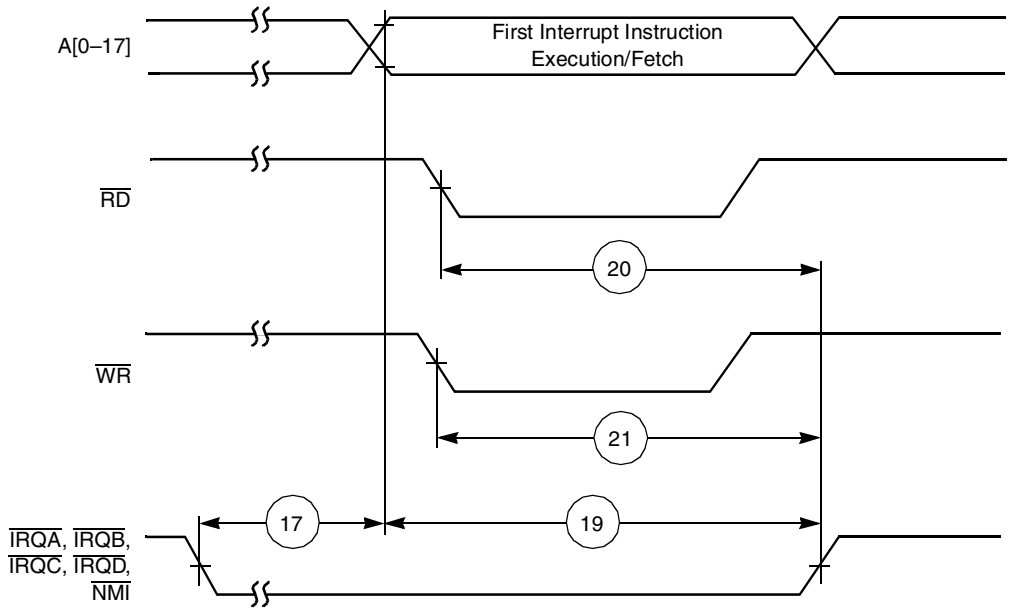
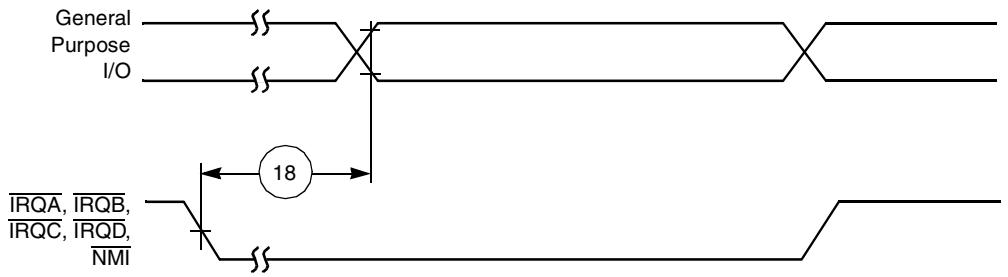


Figure 2-3. Reset Timing



a) First Interrupt Instruction Execution



b) General-Purpose I/O

Figure 2-4. External Fast Interrupt Timing

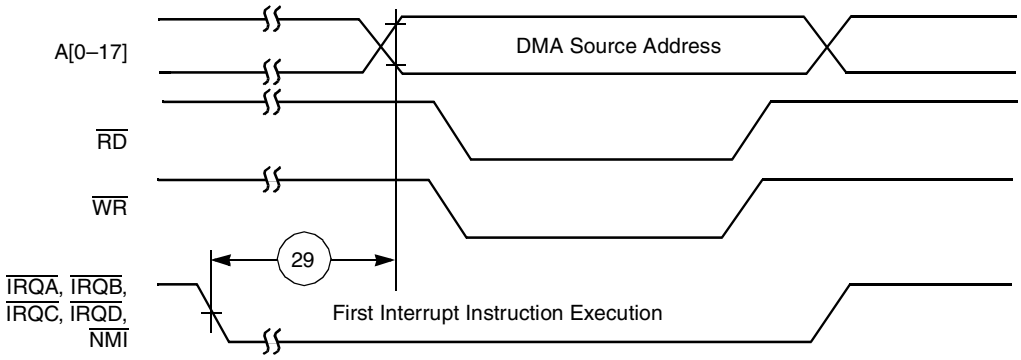


Figure 2-9. External Memory Access (DMA Source) Timing

2.4.5 External Memory Expansion Port (Port A)

2.4.5.1 SRAM Timing

Table 2-8. SRAM Timing

No.	Characteristics	Symbol	Expression[1]	150 MHz		Unit
				Min	Max	
100	Address valid and AA assertion pulse width[2]	t_{RC}, t_{WC}	(WS + 2) × T_C –4.0 [2 ≤WS ≤7] (WS + 3) × T_C –4.0 [WS ≥ 8]	22.7 69.3	— —	ns ns
101	Address and AA valid to $\overline{WR}$ assertion	t_{AS}	0.75 × T_C – 3.0 [2 ≤WS ≤3] 1.25 × T_C – 3.0 [WS ≥ 4]	2.0 5.3	— —	ns ns
102	$\overline{WR}$ assertion pulse width	t_{WP}	WS × T_C –4.0 [2 ≤WS ≤3] (WS –0.5) × T_C –4.0 [WS ≥ 4]	9.3 19.3	— —	ns ns
103	$\overline{WR}$ deassertion to address not valid	t_{WR}	1.25 × T_C –4.0 [2 ≤WS ≤7] 2.25 × T_C –4.0 [WS ≥ 8]	4.3 11.0	— —	ns ns
104	Address and AA valid to input data valid	t_{AA}, t_{AC}	(WS + 0.75) × T_C –6.5 [WS ≥ 2]	—	11.8	ns
105	$\overline{RD}$ assertion to input data valid	t_{OE}	(WS + 0.25) × T_C –6.5 [WS ≥ 2]	—	8.5	ns
106	$\overline{RD}$ deassertion to data not valid (data hold time)	t_{OHZ}		0.0	—	ns
107	Address valid to $\overline{WR}$ deassertion[2]	t_{AW}	(WS + 0.75) × T_C –4.0 [WS ≥ 2]	14.3	—	ns
108	Data valid to $\overline{WR}$ deassertion (data set-up time)	t_{DS} (t_{DW})	(WS –0.25) × T_C –5.4 [WS ≥ 2]	6.3	—	ns
109	Data hold time from $\overline{WR}$ deassertion	t_{DH}	1.25 × T_C –4.0 [2 ≤WS ≤7] 2.25 × T_C –4.0 [WS ≥ 8]	4.3 11.0	— —	ns ns
110	$\overline{WR}$ assertion to data active	—	0.25 × T_C –4.0 [2 ≤WS ≤3] –0.25 × T_C –4.0 [WS ≥ 4]	–2.4 –5.7	— —	ns ns

2.4.5.2 DRAM Timing

The selection guides in **Figure 2-12** and **Figure 2-15** are for primary selection only. Final selection should be based on the timing in the following tables. For example, the selection guide suggests that four wait states must be used for 100 MHz operation with Page Mode DRAM. However, consulting the appropriate table, a designer can evaluate whether fewer wait states might suffice by determining which timing prevents operation at 100 MHz, running the chip at a slightly lower frequency (for example, 95 MHz), using faster DRAM (if it becomes available), and manipulating control factors such as capacitive and resistive load to improve overall system performance.

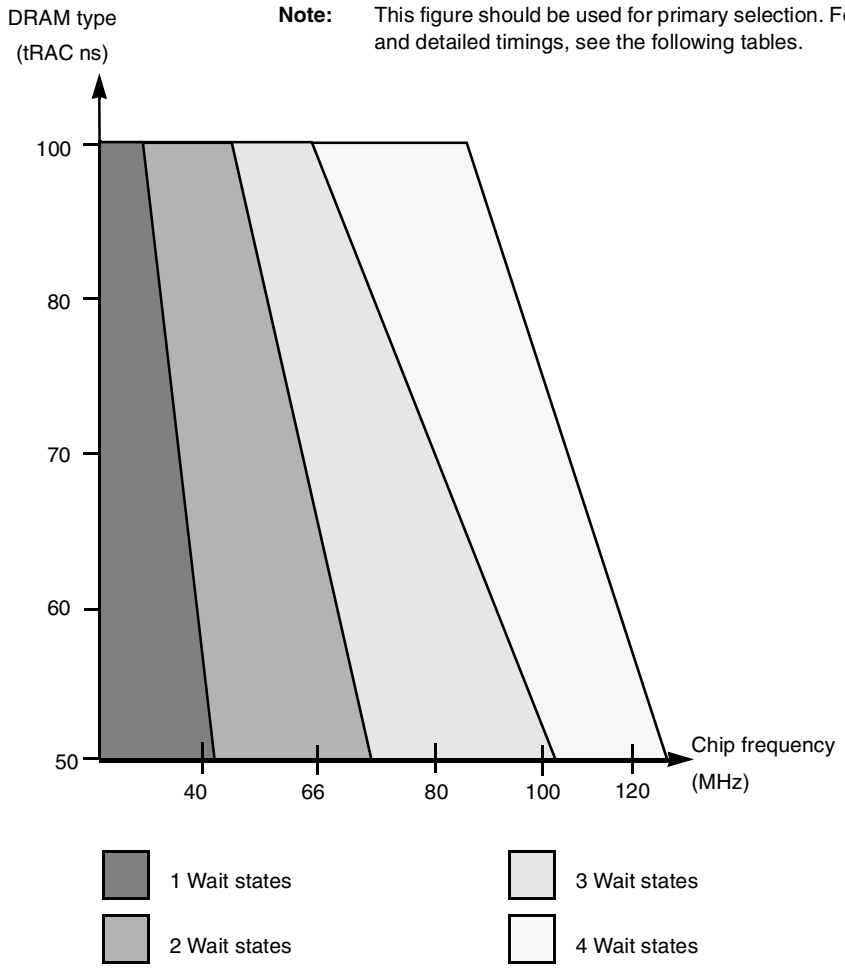


Figure 2-12. DRAM Page Mode Wait State Selection Guide

Table 2-9. DRAM Page Mode Timings, Three Wait States[1,2,3]

No.	Characteristics	Symbol	Expression[4]	100 MHz		Unit
				Min	Max	
131	Page mode cycle time for two consecutive accesses of the same direction		$4 \times T_C$	40.0	—	ns
	Page mode cycle time for mixed (read and write) accesses	t_{PC}	$3.5 \times T_C$	35.0	—	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$2 \times T_C - 5.7$	—	14.3	ns
133	Column address valid to data valid (read)	t_{AA}	$3 \times T_C - 5.7$	—	24.3	ns

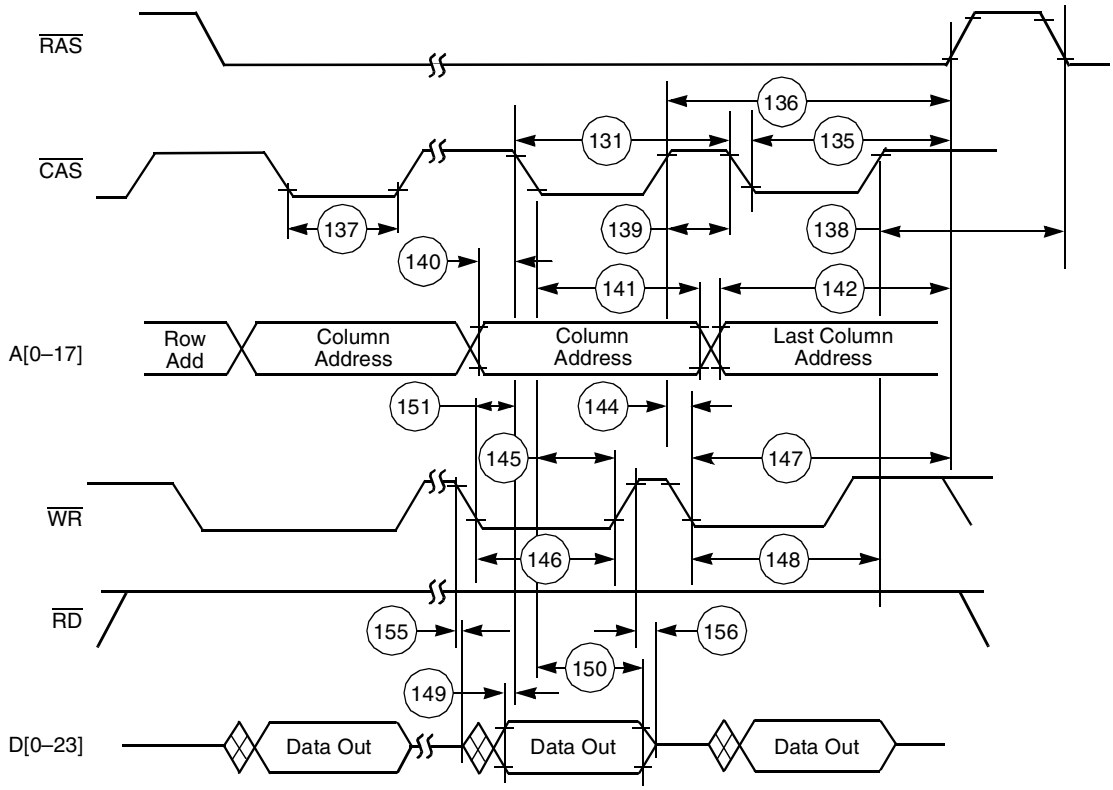


Figure 2-13. DRAM Page Mode Write Accesses

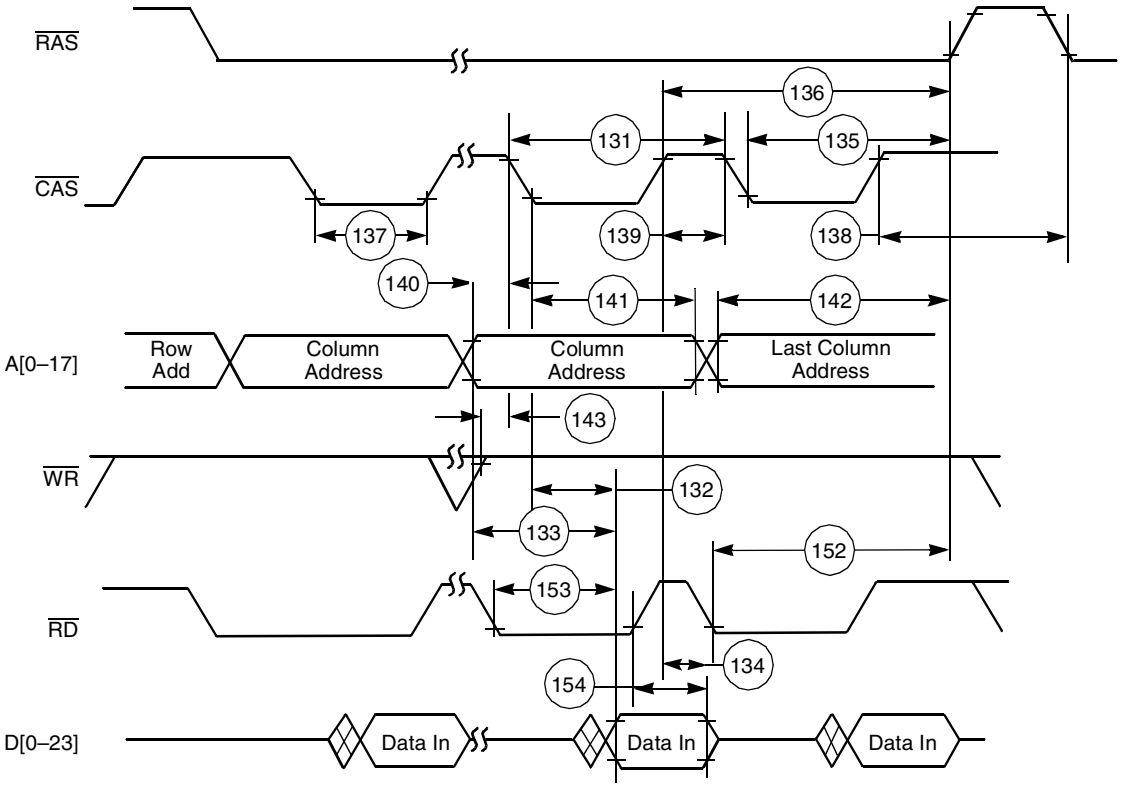


Figure 2-14. DRAM Page Mode Read Accesses

Table 2-11. DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1,2] (Continued)

No.	Characteristics	Symbol	Expression[3]	100 MHz		Unit
				Min	Max	
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$1.75 \times T_C - 4.0$	13.5	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	3.5	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$5.25 \times T_C - 4.0$	48.5	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$7.75 \times T_C - 4.0$	73.5	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$6 \times T_C - 4.0$	56.0	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$3.0 \times T_C - 4.0$	26.0	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[4] assertion	t_{RCH}	$1.75 \times T_C - 3.7$	13.8	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[4] assertion	t_{RRH}	$0.25 \times T_C - 2.0$	0.5	—	ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$5 \times T_C - 4.2$	45.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$7.5 \times T_C - 4.2$	70.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$11.5 \times T_C - 4.5$	110.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$11.75 \times T_C - 4.3$	113.2	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$10.25 \times T_C - 4.3$	98.2	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$5.75 \times T_C - 4.0$	53.5	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$5.25 \times T_C - 4.0$	48.5	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$7.75 \times T_C - 4.0$	73.5	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$6.5 \times T_C - 4.3$	60.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	11.0	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$2.75 \times T_C - 4.0$	23.5	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$11.5 \times T_C - 4.0$	111.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	$10 \times T_C - 7.0$	—	93.0	ns
193	$\overline{RD}$ deassertion to data not valid[5]	t_{GZ}		0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 1.5$	6.0	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	ns

Notes:
1. The number of wait states for an out-of-page access is specified in the DRAM Control Register.
2. The refresh period is specified in the DRAM Control Register.
3. Use the expression to compute the maximum or minimum value listed (or both if the expression includes ±).
4. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.
5. $\overline{RD}$ deassertion always occurs after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 2-14. Host Interface Timings[1,2,12] (Continued)

No.	Characteristic[10]	Expression	150 MHz		Unit
			Min	Max	
340	Delay from data strobe assertion to host request deassertion for "Last Data Register" read or write (HROD=0)[4, 7, 8]		—	13.0	ns
341	Delay from data strobe assertion to host request deassertion for "Last Data Register" read or write (HROD=1, open drain host request)[4, 7, 8, 9]		—	300.0	ns

Notes:
1. See the Programmer's Model section in the chapter on the HI08 in the *DSP56311 User's Manual*.
2. In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.
3. This timing is applicable only if two consecutive reads from one of these registers are executed.
4. The data strobe is Host Read (HRD) or Host Write (HWR) in the Dual Data Strobe mode and Host Data Strobe (HDS) in the Single Data Strobe mode.
5. The read data strobe is HRD in the Dual Data Strobe mode and HDS in the Single Data Strobe mode.
6. The write data strobe is HWR in the Dual Data Strobe mode and HDS in the Single Data Strobe mode.
7. The host request is HREQ in the Single Host Request mode and HRRQ and HTRQ in the Double Host Request mode.
8. The "Last Data Register" is the register at address $7, which is the last location to be read or written in data transfers. This is RXL/TXL in the Big Endian mode (HLEND = 0; HLEND is the Interface Control Register bit 7—ICR[7]), or RXH/TXH in the Little Endian mode (HLEND = 1).
9. In this calculation, the host request signal is pulled up by a 4.7 kΩ resistor in the Open-drain mode.
10. V_{CCQH} = 3.3 V ± 0.3 V, V_{CC} = 1.8 V ± 0.1 V; T_J = –40°C to +100 °C, C_L = 50 pF
11. This timing is applicable only if a read from the "Last Data Register" is followed by a read from the RXL, RXM, or RXH registers without first polling RXDF or HREQ bits, or waiting for the assertion of the HREQ signal.
12. After the external host writes a new value to the ICR, the HI08 is ready for operation after three DSP clock cycles (3 × Tc).

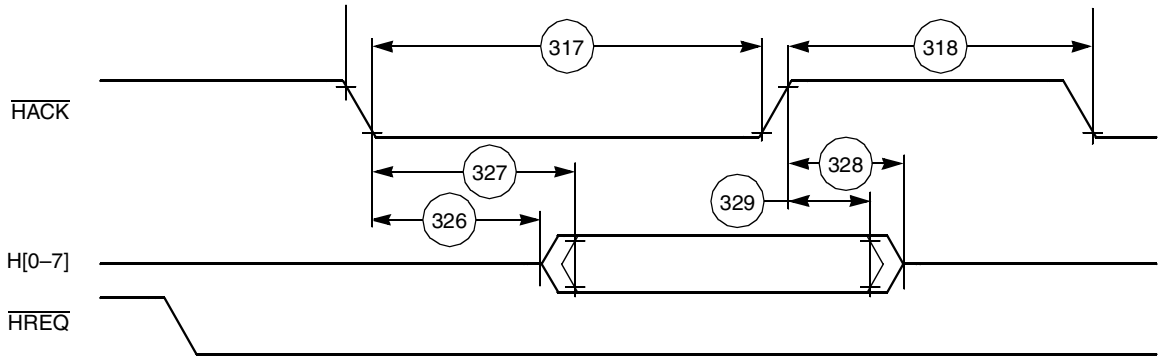
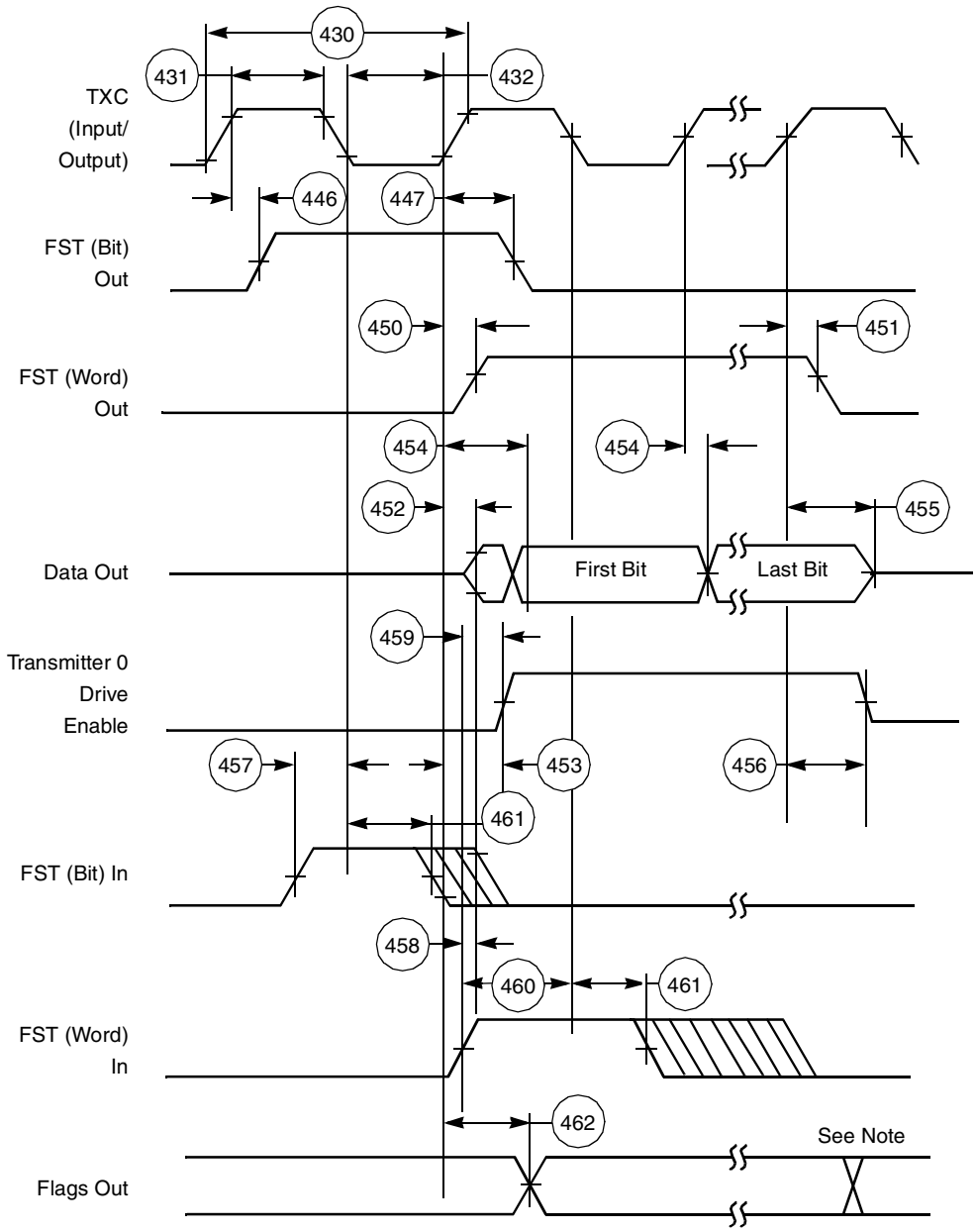


Figure 2-20. Host Interrupt Vector Register (IVR) Read Timing Diagram

2.4.8 ESSI0/ESSI1 Timing

Table 2-16. ESSI Timings

No.	Characteristics[4, 6]	Symbol	Expression	150 MHz		Cond-ition[5]	Unit
				Min	Max		
430	Clock cycle[1]	t_{SSICC}	$6 \times T_C$ $8 \times T_C$	40.0 53.4	— —	x ck i ck	ns ns
431	Clock high period • For internal clock • For external clock		 $4 \times T_C - 10.0$ $3 \times T_C$	 16.7 20.0	 — —		 ns ns
432	Clock low period • For internal clock • For external clock		 $4 \times T_C - 10.0$ $3 \times T_C$	 16.7 20.0	 — —		 ns ns
433	RXC rising edge to FSR out (bit-length) high			— —	37.0 22.0	x ck i ck a	ns
434	RXC rising edge to FSR out (bit-length) low			— —	37.0 22.0	x ck i ck a	ns
435	RXC rising edge to FSR out (word-length-relative) high[2]			— —	39.0 37.0	x ck i ck a	ns
436	RXC rising edge to FSR out (word-length-relative) low[2]			— —	39.0 37.0	x ck i ck a	ns
437	RXC rising edge to FSR out (word-length) high			— —	36.0 21.0	x ck i ck a	ns
438	RXC rising edge to FSR out (word-length) low			— —	37.0 22.0	x ck i ck a	ns
439	Data in set-up time before RXC (SCK in Synchronous mode) falling edge			10.0 19.0	— —	x ck i ck	ns
440	Data in hold time after RXC falling edge			5.0 3.0	— —	x ck i ck	ns
441	FSR input (bl, wr)[6] high before RXC falling edge[2]			1.0 23.0	— —	x ck i ck a	ns
442	FSR input (wl)[6] high before RXC falling edge			3.5 23.0	— —	x ck i ck a	ns
443	FSR input hold time after RXC falling edge			3.0 0.0	— —	x ck i ck a	ns
444	Flags input set-up before RXC falling edge			5.5 19.0	— —	x ck i ck s	ns
445	Flags input hold time after RXC falling edge			6.0 0.0	— —	x ck i ck s	ns
446	TXC rising edge to FST out (bit-length) high			— —	29.0 15.0	x ck i ck	ns
447	TXC rising edge to FST out (bit-length) low			— —	31.0 17.0	x ck i ck	ns
448	TXC rising edge to FST out (word-length-relative) high[2]			— —	31.0 17.0	x ck i ck	ns
449	TXC rising edge to FST out (word-length-relative) low[2]			— —	33.0 19.0	x ck i ck	ns
450	TXC rising edge to FST out (word-length) high			— —	30.0 16.0	x ck i ck	ns



Note: In Network mode, output flag transitions can occur at the start of each time slot within the frame. In Normal mode, the output flag state is asserted for the entire frame period.

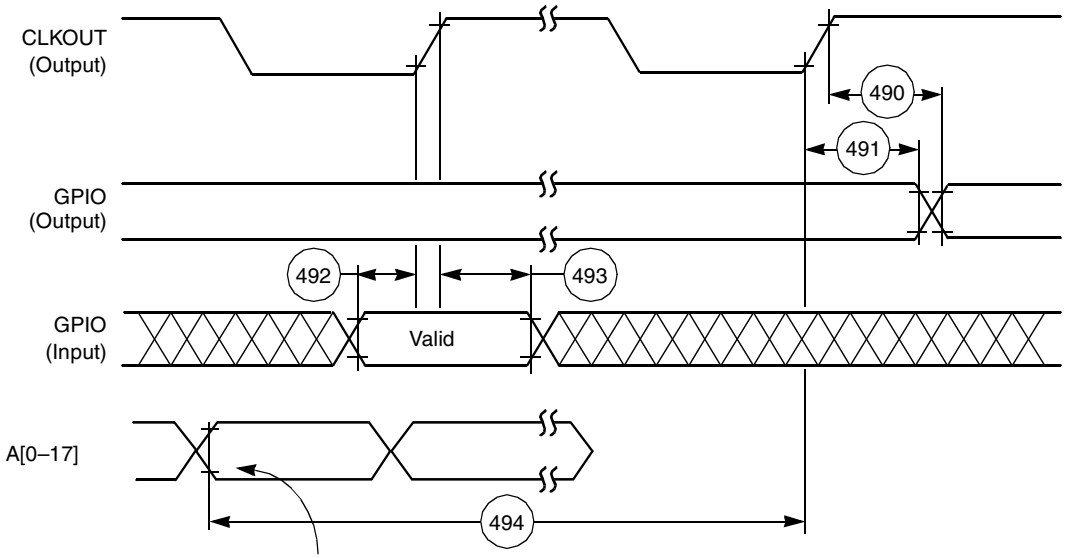
Figure 2-31. ESSI Transmitter Timing

2.4.10 Considerations For GPIO Use

2.4.10.1 Operating Frequency of 100 MHz or Less

Table 2-18. GPIO Timing

No.	Characteristics	Expression	100 MHz		Unit
			Min	Max	
490	CLKOUT edge to GPIO out valid (GPIO out delay time)		—	8.5	ns
491	CLKOUT edge to GPIO out not valid (GPIO out hold time)		0.0	—	ns
492	GPIO In valid to CLKOUT edge (GPIO in set-up time)		8.5	—	ns
493	CLKOUT edge to GPIO in not valid (GPIO in hold time)		0.0	—	ns
494	Fetch to CLKOUT edge before GPIO change	Minimum: 6.75 × T_C	67.5	—	ns
Note:	V_{CC} = 3.3 V ± 0.3 V; T_J = -40°C to +100 °C, C_L = 50 pF.				



Fetch the instruction MOVE X0,X:(R0); X0 contains the new value of GPIO and R0 contains the address of the GPIO data register.

Figure 2-34. GPIO Timing

3.1 Package Description

Top and bottom views of the MAP-BGA packages are shown in **Figure 3-1** and **Figure 3-2** with their pin-outs.

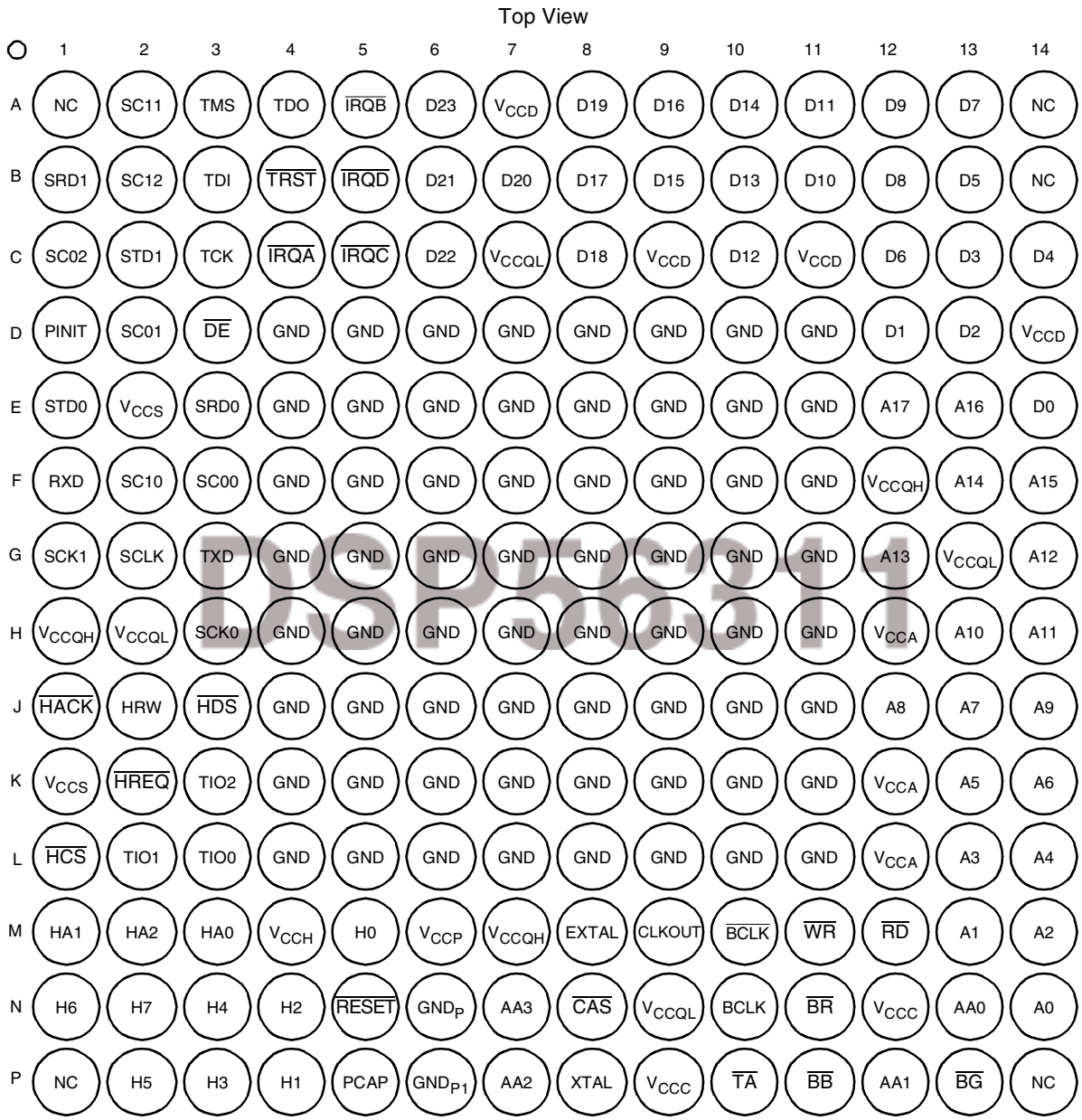


Figure 3-1. DSP56311 MAP-BGA Package, Top View

```
        page    132,55,0,0,0
        opt     mex

ioequ   ident   1,0

;---------------------------------------------------------------------------
;
;       EQUATES for I/O Port Programming
;
;---------------------------------------------------------------------------

;       Register Addresses

M_HDR EQU $FFFFC9                   ; Host port GPIO data Register
M_HDDR EQU $FFFFC8                  ; Host port GPIO direction Register
M_PCRC EQU $FFFFBF                  ; Port C Control Register
M_PRRC EQU $FFFFBE                  ; Port C Direction Register
M_PDRC EQU $FFFFBD                  ; Port C GPIO Data Register
M_PCRD EQU $FFFFAF                  ; Port D Control register
M_PRRD EQU $FFFFAE                  ; Port D Direction Data Register
M_PDRD EQU $FFFFAD                  ; Port D GPIO Data Register
M_PCRE EQU $FFFF9F                  ; Port E Control register
M_PRRE EQU $FFFF9E                  ; Port E Direction Register
M_PDRE EQU $FFFF9D                  ; Port E Data Register
M_OGDB EQU $FFFFFC                  ; OnCE GDB Register


;---------------------------------------------------------------------------
;
;       EQUATES for Host Interface
;
;---------------------------------------------------------------------------

;       Register Addresses

M_HCR EQU $FFFFC2                   ; Host Control Register
M_HSR EQU $FFFFC3                   ; Host Status Register
M_HPCR EQU $FFFFC4                  ; Host Polarity Control Register
M_HBAR EQU $FFFFC5                  ; Host Base Address Register
M_HRX EQU $FFFFC6                   ; Host Receive Register
M_HTX EQU $FFFFC7                   ; Host Transmit Register

;       HCR bits definition
M_HRIE EQU $0                       ; Host Receive interrupts Enable
M_HTIE EQU $1                       ; Host Transmit Interrupt Enable
M_HCIE EQU $2                       ; Host Command Interrupt Enable
M_HF2 EQU $3                        ; Host Flag 2
M_HF3 EQU $4                        ; Host Flag 3

;       HSR bits definition
M_HRDF EQU $0                       ; Host Receive Data Full
M_HTDE EQU $1                       ; Host Receive Data Empty
M_HCP EQU $2                        ; Host Command Pending
M_HF0 EQU $3                        ; Host Flag 0
M_HF1 EQU $4                        ; Host Flag 1


;       HPCR bits definition
M_HGEN EQU $0                       ; Host Port GPIO Enable
M_HA8EN EQU $1                      ; Host Address 8 Enable
M_HA9EN EQU $2                      ; Host Address 9 Enable
M_HCSEN EQU $3                      ; Host Chip Select Enable
```

```
M_SHFD EQU 6                          ; Shift Direction
M_FSL EQU $180                        ; Frame Sync Length Mask (FSL0-FSL1)
M_FSL0 EQU 7                          ; Frame Sync Length 0
M_FSL1 EQU 8                          ; Frame Sync Length 1
M_FSR EQU 9                           ; Frame Sync Relative Timing
M_FSP EQU 10                          ; Frame Sync Polarity
M_CKP EQU 11                          ; Clock Polarity
M_SYN EQU 12                          ; Sync/Async Control
M_MOD EQU 13                          ; SSI Mode Select
M_SSTE EQU $1C000                     ; SSI Transmit enable Mask
M_SSTE2 EQU 14                        ; SSI Transmit #2 Enable
M_SSTE1 EQU 15                        ; SSI Transmit #1 Enable
M_SSTE0 EQU 16                        ; SSI Transmit #0 Enable
M_SSRE EQU 17                         ; SSI Receive Enable
M_SSTIE EQU 18                        ; SSI Transmit Interrupt Enable
M_SSRIE EQU 19                        ; SSI Receive Interrupt Enable
M_STLIE EQU 20                        ; SSI Transmit Last Slot Interrupt Enable
M_SRLIE EQU 21                        ; SSI Receive Last Slot Interrupt Enable
M_STEIE EQU 22                        ; SSI Transmit Error Interrupt Enable
M_SREIE EQU 23                        ; SI Receive Error Interrupt Enable

;       SSI Status Register Bit Flags

M_IF EQU $3                           ; Serial Input Flag Mask
M_IF0 EQU 0                           ; Serial Input Flag 0
M_IF1 EQU 1                           ; Serial Input Flag 1
M_TFS EQU 2                           ; Transmit Frame Sync Flag
M_RFS EQU 3                           ; Receive Frame Sync Flag
M_TUE EQU 4                           ; Transmitter Underrun Error FLag
M_ROE EQU 5                           ; Receiver Overrun Error Flag
M_TDE EQU 6                           ; Transmit Data Register Empty
M_RDF EQU 7                           ; Receive Data Register Full

;       SSI Transmit Slot Mask Register A

M_SSTSA EQU $FFFF                     ; SSI Transmit Slot Bits Mask A (TS0-TS15)

;       SSI Transmit Slot Mask Register B

M_SSTSB EQU $FFFF                     ; SSI Transmit Slot Bits Mask B (TS16-TS31)

;       SSI Receive Slot Mask Register A

M_SSRSA EQU $FFFF                     ; SSI Receive Slot Bits Mask A (RS0-RS15)

;       SSI Receive Slot Mask Register B

M_SSRSB EQU $FFFF                     ; SSI Receive Slot Bits Mask B (RS16-RS31)



;------------------------------------------------------------------------
;
;       EQUATES for Exception Processing
;
;------------------------------------------------------------------------


;       Register Addresses

M_IPRC EQU $FFFFFF                    ; Interrupt Priority Register Core
M_IPRP EQU $FFFFFE                    ; Interrupt Priority Register Peripheral
```

```
M_PCOD EQU 19                           ; PLL Clock Output Disable Bit
M_PD EQU $F00000                        ; PreDivider Factor Bits Mask (PD0-PD3)



;---------------------------------------------------------------------
;
;       EQUATES for BIU
;
;---------------------------------------------------------------------

;       Register Addresses Of BIU


M_BCR EQU $FFFFFB                       ; Bus Control Register
M_DCR EQU $FFFFFA                       ; DRAM Control Register
M_AAR0 EQU $FFFFF9                      ; Address Attribute Register 0
M_AAR1 EQU $FFFFF8                      ; Address Attribute Register 1
M_AAR2 EQU $FFFFF7                      ; Address Attribute Register 2
M_AAR3 EQU $FFFFF6                      ; Address Attribute Register 3
M_IDR EQU  $FFFFF5                      ; ID Register

;       Bus Control Register

M_BA0W EQU $1F                          ; Area 0 Wait Control Mask (BA0W0-BA0W4)
M_BA1W EQU $3E0                         ; Area 1 Wait Control Mask (BA1W0-BA14)
M_BA2W EQU $1C00                        ; Area 2 Wait Control Mask (BA2W0-BA2W2)
M_BA3W EQU $E000                        ; Area 3 Wait Control Mask (BA3W0-BA3W3)
M_BDFW EQU $1F0000                      ; Default Area Wait Control Mask (BDFW0-BDFW4)
M_BBS EQU 21                            ; Bus State
M_BLH EQU 22                            ; Bus Lock Hold
M_BRH EQU 23                            ; Bus Request Hold

;       DRAM Control Register

M_BCW EQU $3                            ; In Page Wait States Bits Mask (BCW0-BCW1)
M_BRW EQU $C                            ; Out Of Page Wait States Bits Mask (BRW0-BRW1)
M_BPS EQU $300                          ; DRAM Page Size Bits Mask (BPS0-BPS1)
M_BPLE EQU 11                           ; Page Logic Enable
M_BME EQU 12                            ; Mastership Enable
M_BRE EQU 13                            ; Refresh Enable
M_BSTR EQU 14                           ; Software Triggered Refresh
M_BRF EQU $7F8000                       ; Refresh Rate Bits Mask (BRF0-BRF7)
M_BRP EQU 23                            ; Refresh prescaler

;       Address Attribute Registers

M_BAT EQU $3                            ; Ext. Access Type and Pin Def. Bits Mask (BAT0-BAT1)
M_BAAP EQU 2                            ; Address Attribute Pin Polarity
M_BPEN EQU 3                            ; Program Space Enable
M_BXEN EQU 4                            ; X Data Space Enable
M_BYEN EQU 5                            ; Y Data Space Enable
M_BAM EQU 6                             ; Address Muxing
M_BPAC EQU 7                            ; Packing Enable
M_BNC EQU $F00                          ; Number of Address Bits to Compare Mask (BNC0-BNC3)
M_BAC EQU $FFF000                       ; Address to Compare Bits Mask (BAC0-BAC11)


;       control and status bits in SR

M_CP EQU $c00000                        ; mask for CORE-DMA priority bits in SR
M_CA EQU 0                              ; Carry
M_V EQU 1                               ; Overflow
```

```
I_VEC EQU $0
       endif

;------------------------------------------------------------------------
; Non-Maskable interrupts
;------------------------------------------------------------------------
I_RESET EQU I_VEC+$00               ; Hardware RESET
I_STACK EQU I_VEC+$02               ; Stack Error
I_ILL EQU I_VEC+$04                 ; Illegal Instruction
I_DBG EQU I_VEC+$06                 ; Debug Request
I_TRAP EQU I_VEC+$08                ; Trap
I_NMI EQU I_VEC+$0A                 ; Non Maskable Interrupt

;------------------------------------------------------------------------
; Interrupt Request Pins
;------------------------------------------------------------------------
I_IRQA EQU I_VEC+$10                ; IRQA
I_IRQB EQU I_VEC+$12                ; IRQB
I_IRQC EQU I_VEC+$14                ; IRQC
I_IRQD EQU I_VEC+$16                ; IRQD

;------------------------------------------------------------------------
; DMA Interrupts
;------------------------------------------------------------------------
I_DMA0 EQU I_VEC+$18                ; DMA Channel 0
I_DMA1 EQU I_VEC+$1A                ; DMA Channel 1
I_DMA2 EQU I_VEC+$1C                ; DMA Channel 2
I_DMA3 EQU I_VEC+$1E                ; DMA Channel 3
I_DMA4 EQU I_VEC+$20                ; DMA Channel 4
I_DMA5 EQU I_VEC+$22                ; DMA Channel 5

;------------------------------------------------------------------------
; Timer Interrupts
;------------------------------------------------------------------------
I_TIM0C EQU I_VEC+$24               ; TIMER 0 compare
I_TIM0OF EQU I_VEC+$26              ; TIMER 0 overflow
I_TIM1C EQU I_VEC+$28               ; TIMER 1 compare
I_TIM1OF EQU I_VEC+$2A              ; TIMER 1 overflow
I_TIM2C EQU I_VEC+$2C               ; TIMER 2 compare
I_TIM2OF EQU I_VEC+$2E              ; TIMER 2 overflow

;------------------------------------------------------------------------
; ESSI Interrupts
;------------------------------------------------------------------------
I_SI0RD EQU I_VEC+$30               ; ESSI0 Receive Data
I_SI0RDE EQU I_VEC+$32              ; ESSI0 Receive Data w/ exception Status
I_SI0RLS EQU I_VEC+$34              ; ESSI0 Receive last slot
I_SI0TD EQU I_VEC+$36               ; ESSI0 Transmit data
I_SI0TDE EQU I_VEC+$38              ; ESSI0 Transmit Data w/ exception Status
I_SI0TLS EQU I_VEC+$3A              ; ESSI0 Transmit last slot
I_SI1RD EQU I_VEC+$40               ; ESSI1 Receive Data
I_SI1RDE EQU I_VEC+$42              ; ESSI1 Receive Data w/ exception Status
I_SI1RLS EQU I_VEC+$44              ; ESSI1 Receive last slot
I_SI1TD EQU I_VEC+$46               ; ESSI1 Transmit data
I_SI1TDE EQU I_VEC+$48              ; ESSI1 Transmit Data w/ exception Status
I_SI1TLS EQU I_VEC+$4A              ; ESSI1 Transmit last slot

;------------------------------------------------------------------------
; SCI Interrupts
;------------------------------------------------------------------------
I_SCIRD EQU I_VEC+$50               ; SCI Receive Data
I_SCIRDE EQU I_VEC+$52              ; SCI Receive Data With Exception Status
I_SCITD EQU I_VEC+$54               ; SCI Transmit Data
```