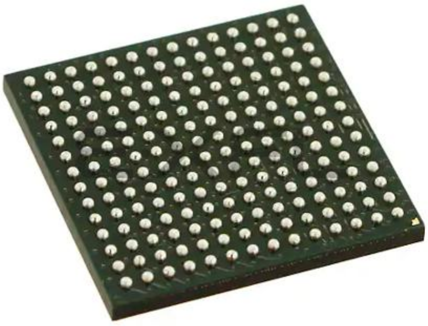

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	150MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spakdsp311vl150

Signals/Connections 1

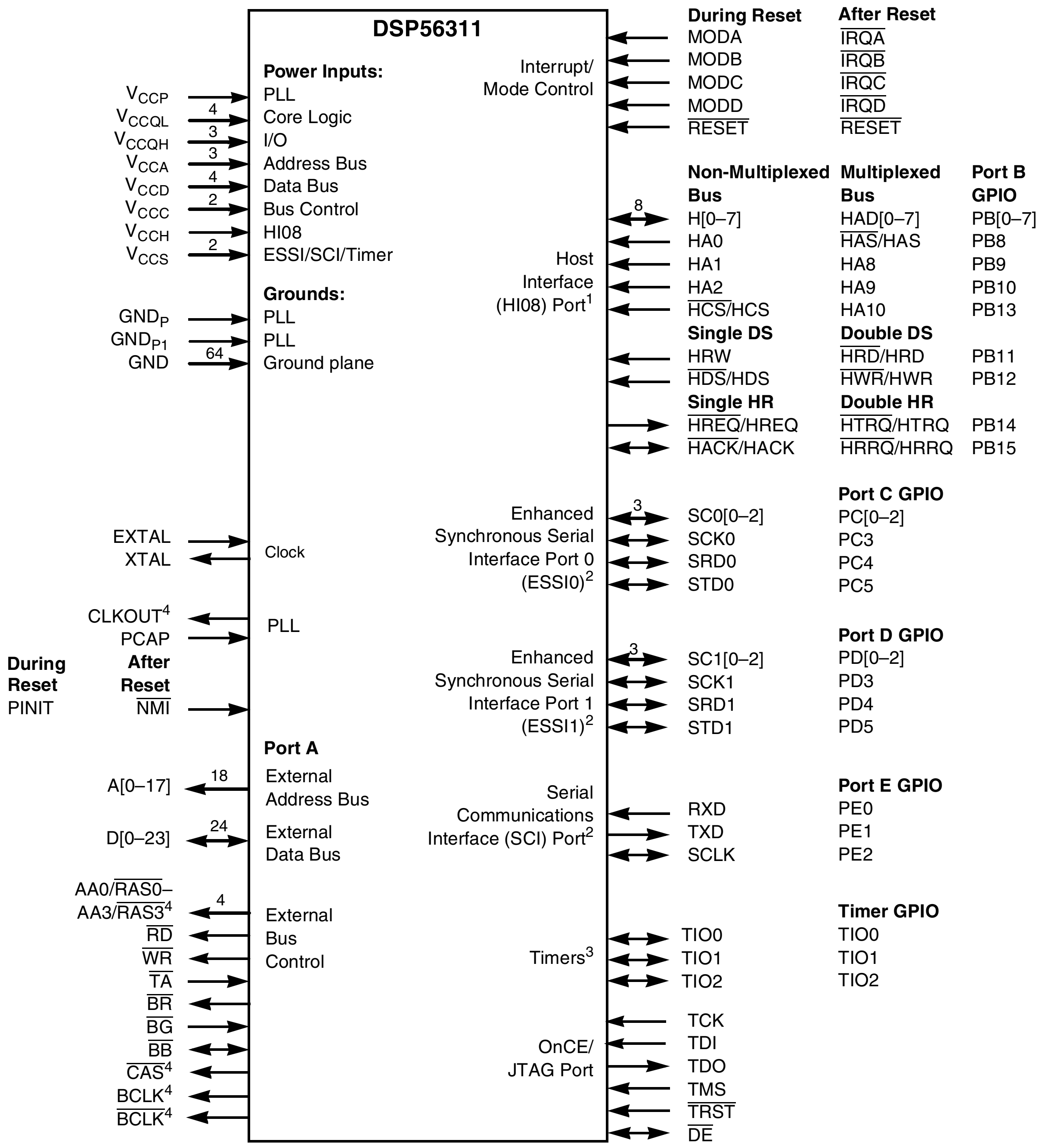
The DSP56311 input and output signals are organized into functional groups as shown in **Table 1-1**. **Figure 1-1** diagrams the DSP56311 signals by functional group. The remainder of this chapter describes the signal pins in each functional group.

Table 1-1. DSP56311 Functional Signal Groupings

Functional Group		Number of Signals
Power (V_{CC})		20
Ground (GND)		66
Clock		2
PLL		3
Address bus	Port A[1]	18
Data bus		24
Bus control		13
Interrupt and mode control		5
Host interface (HI08)	Port B[2]	16
Enhanced synchronous serial interface (ESSI)	Ports C and D[3]	12
Serial communication interface (SCI)	Port E[4]	3
Timer		3
OnCE/JTAG Port		6

Notes:
1. Port A signals define the external memory interface port, including the external address bus, data bus, and control signals.
2. Port B signals are the HI08 port signals multiplexed with the GPIO signals.
3. Port C and D signals are the two ESSI port signals multiplexed with the GPIO signals.
4. Port E signals are the SCI port signals multiplexed with the GPIO signals.
5. There are 5 signal connections that are not used. These are designated as no connect (NC) in the package description (see **Chapter 3**).

Note: The Clock Output (CLKOUT), BCLK, $\overline{\text{BCLK}}$, $\overline{\text{CAS}}$, and $\overline{\text{RAS[0–3]}}$ signals used by other DSP56300 family members are supported by the DSP56311 at operating frequencies up to 100 MHz. Therefore, above 100 MHz, you must enable bus arbitration by setting the Asynchronous Bus Arbitration Enable Bit (ABE) in the operating mode register. When set, the ABE bit eliminates the required set-up and hold times for $\overline{\text{BB}}$ and $\overline{\text{BG}}$ with respect to $\overline{\text{CLKOUT}}$. In addition, DRAM access is not supported above 100 MHz.



Notes:
1. The HI08 port supports a non-multiplexed or a multiplexed bus, single or double Data Strobe (DS), and single or double Host Request (HR) configurations. Since each of these modes is configured independently, any combination of these modes is possible. These HI08 signals can also be configured alternatively as GPIO signals (PB[0–15]). Signals with dual designations (for example, $\overline{\text{HAS}}$/HAS) have configurable polarity.
2. The ESSI0, ESSI1, and SCI signals are multiplexed with the Port C GPIO signals (PC[0–5]), Port D GPIO signals (PD[0–5]), and Port E GPIO signals (PE[0–2]), respectively.
3. TIO[0–2] can be configured as GPIO signals.
4. CLKOUT, BCLK, $\overline{\text{BCLK}}$, $\overline{\text{CAS}}$, and $\overline{\text{RAS}}$[0–3] are valid only for operating frequencies $\leq$100 MHz.

Figure 1-1. Signals Identified by Functional Group

1.1 Power

Table 1-2. Power Inputs

Power Name	Description
V_{CCP}	**PLL Power**—V_{CC} dedicated for PLL use. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail.
V_{CCQL}	**Quiet Core (Low) Power**—An isolated power for the core processing logic. This input must be isolated externally from all other chip power inputs.
V_{CCQH}	**Quiet External (High) Power**—A quiet power source for I/O lines. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCA}	**Address Bus Power**—An isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCD}	**Data Bus Power**—An isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCC}	**Bus Control Power**—An isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCH}	**Host Power**—An isolated power for the HI08 I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCS}	**ESSI, SCI, and Timer Power**—An isolated power for the ESSI, SCI, and timer I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
Note: The user must provide adequate external decoupling capacitors for all power connections.	

1.2 Ground

Table 1-3. Grounds

Name	Description
GND_P	**PLL Ground**—Ground-dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. V_{CCP} should be bypassed to GND_P by a 0.47 µF capacitor located as close as possible to the chip package.
GND_{P1}	**PLL Ground 1**—Ground-dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground.
GND	**Ground**—Connected to an internal device ground plane.
Note: The user must provide adequate external decoupling capacitors for all GND connections.	

1.3 Clock

Table 1-4. Clock Signals

Signal Name	Type	State During Reset	Signal Description
EXTAL	Input	Input	**External Clock/Crystal Input**—Interfaces the internal crystal oscillator input to an external crystal or an external clock.
XTAL	Output	Chip-driven	**Crystal Output**—Connects the internal crystal oscillator output to an external crystal. If an external clock is used, leave XTAL unconnected.

Table 1-8. External Bus Control Signals (Continued)

Signal Name	Type	State During Reset, Stop, or Wait	Signal Description
$\overline{BR}$	Output	Reset: Output (deasserted) State during Stop/Wait depends on BRH bit setting: • BRH = 0: Output, deasserted • BRH = 1: Maintains last state (that is, if asserted, remains asserted)	**Bus Request**—Asserted when the DSP requests bus mastership. $\overline{BR}$ is deasserted when the DSP no longer needs the bus. $\overline{BR}$ may be asserted or deasserted independently of whether the DSP56311 is a bus master or a bus slave. Bus “parking” allows $\overline{BR}$ to be deasserted even though the DSP56311 is the bus master. (See the description of bus “parking” in the $\overline{BB}$ signal description.) The bus request hold (BRH) bit in the BCR allows $\overline{BR}$ to be asserted under software control even though the DSP does not need the bus. $\overline{BR}$ is typically sent to an external bus arbitrator that controls the priority, parking, and tenure of each master on the same external bus. $\overline{BR}$ is affected only by DSP requests for the external bus, never for the internal bus. During hardware reset, $\overline{BR}$ is deasserted and the arbitration is reset to the bus slave state.
$\overline{BG}$	Input	Ignored Input	**Bus Grant**—Asserted by an external bus arbitration circuit when the DSP56311 becomes the next bus master. When $\overline{BG}$ is asserted, the DSP56311 must wait until $\overline{BB}$ is deasserted before taking bus mastership. When $\overline{BG}$ is deasserted, bus mastership is typically given up at the end of the current bus cycle. This may occur in the middle of an instruction that requires more than one external bus cycle for execution. The default operation of this bit requires a set-up and hold time as specified in **Chapter 2**. An alternate mode can be invoked: set the asynchronous bus arbitration enable (ABE) bit (Bit 13) in the Operating Mode Register. When this bit is set, $\overline{BG}$ and $\overline{BB}$ are synchronized internally. This eliminates the respective set-up and hold time requirements but adds a required delay between the deassertion of an initial $\overline{BG}$ input and the assertion of a subsequent $\overline{BG}$ input.
$\overline{BB}$	Input/ Output	Ignored Input	**Bus Busy**—Indicates that the bus is active. Only after $\overline{BB}$ is deasserted can the pending bus master become the bus master (and then assert the signal again). The bus master may keep $\overline{BB}$ asserted after ceasing bus activity regardless of whether $\overline{BR}$ is asserted or deasserted. Called “bus parking,” this allows the current bus master to reuse the bus without rearbitration until another device requires the bus. $\overline{BB}$ is deasserted by an “active pull-up” method (that is, $\overline{BB}$ is driven high and then released and held high by an external pull-up resistor). The default operation of this signal requires a set-up and hold time as specified in **Chapter 2**. An alternative mode can be invoked by setting the ABE bit (Bit 13) in the Operating Mode Register. When this bit is set, $\overline{BG}$ and $\overline{BB}$ are synchronized internally. See $\overline{BG}$ for additional information. **Note**: $\overline{BB}$ requires an external pull-up resistor.
$\overline{CAS}$	Output	Tri-stated	**Column Address Strobe**—When the DSP is the bus master, $\overline{CAS}$ is an active-low output used by DRAM to strobe the column address. Otherwise, if the Bus Mastership Enable (BME) bit in the DRAM control register is cleared, the signal is tri-stated. **Note:** DRAM access is not supported above 100 MHz.
BCLK	Output	Tri-stated	**Bus Clock** When the DSP is the bus master, BCLK is active when the ATE bit in the Operating Mode Register is set. When BCLK is active and synchronized to CLKOUT by the internal PLL, BCLK precedes CLKOUT by one-fourth of a clock cycle. **Note:** At operating frequencies above 100 MHz, this signal produces a low-amplitude waveform that is not usable externally by other devices.
$\overline{BCLK}$	Output	Tri-stated	**Bus Clock Not** When the DSP is the bus master, $\overline{BCLK}$ is the inverse of the BCLK signal. Otherwise, the signal is tri-stated. **Note:** At operating frequencies above 100 MHz, this signal produces a low-amplitude waveform that is not usable externally by other devices.

1.6 Interrupt and Mode Control

The interrupt and mode control signals select the chip operating mode as it comes out of hardware reset. After $\overline{\text{RESET}}$ is deasserted, these inputs are hardware interrupt request lines.

Table 1-9. Interrupt and Mode Control

Signal Name	Type	State During Reset	Signal Description
MODA $\overline{\text{IRQA}}$	Input Input	Schmitt-trigger Input	**Mode Select A**—MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the $\overline{\text{RESET}}$ signal is deasserted. **External Interrupt Request A**—After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the STOP or WAIT standby state and $\overline{\text{IRQA}}$ is asserted, the processor exits the STOP or WAIT state.
MODB $\overline{\text{IRQB}}$	Input Input	Schmitt-trigger Input	**Mode Select B**—MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the $\overline{\text{RESET}}$ signal is deasserted. **External Interrupt Request B**—After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the WAIT standby state and $\overline{\text{IRQB}}$ is asserted, the processor exits the WAIT state.
MODC $\overline{\text{IRQC}}$	Input Input	Schmitt-trigger Input	**Mode Select C**—MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the $\overline{\text{RESET}}$ signal is deasserted. **External Interrupt Request C**—After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the WAIT standby state and $\overline{\text{IRQC}}$ is asserted, the processor exits the WAIT state.
MODD $\overline{\text{IRQD}}$	Input Input	Schmitt-trigger Input	**Mode Select D**—MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the $\overline{\text{RESET}}$ signal is deasserted. **External Interrupt Request D**—After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the WAIT standby state and $\overline{\text{IRQD}}$ is asserted, the processor exits the WAIT state.
$\overline{\text{RESET}}$	Input	Schmitt-trigger Input	**Reset**—Places the chip in the Reset state and resets the internal phase generator. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. When the $\overline{\text{RESET}}$ signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The $\overline{\text{RESET}}$ signal must be asserted after powerup.

1.12 JTAG and OnCE Interface

The DSP56300 family and in particular the DSP56311 support circuit-board test strategies based on the **IEEE® Std.** 1149.1™ test access port and boundary scan architecture, the industry standard developed under the sponsorship of the Test Technology Committee of IEEE and the JTAG. The OnCE module provides a means to interface nonintrusively with the DSP56300 core and its peripherals so that you can examine registers, memory, or on-chip peripherals. Functions of the OnCE module are provided through the JTAG TAP signals. For programming models, see the chapter on debugging support in the *DSP56300 Family Manual*.

Table 1-16. JTAG/OnCE Interface

Signal Name	Type	State During Reset	Signal Description
TCK	Input	Input	**Test Clock**—A test clock input signal to synchronize the JTAG test logic.
TDI	Input	Input	**Test Data Input**—A test data serial input signal for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor.
TDO	Output	Tri-stated	**Test Data Output**—A test data serial output signal for test instructions and data. TDO is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.
TMS	Input	Input	**Test Mode Select**—Sequences the test controller's state machine. TMS is sampled on the rising edge of TCK and has an internal pull-up resistor.
$\overline{\text{TRST}}$	Input	Input	**Test Reset**—Initializes the test controller asynchronously. $\overline{\text{TRST}}$ has an internal pull-up resistor. $\overline{\text{TRST}}$ must be asserted during and after power-up (see EB610/D for details).
$\overline{\text{DE}}$	Input/ Output	Input	**Debug Event**—As an input, initiates Debug mode from an external command controller, and, as an open-drain output, acknowledges that the chip has entered Debug mode. As an input, $\overline{\text{DE}}$ causes the DSP56300 core to finish executing the current instruction, save the instruction pipeline information, enter Debug mode, and wait for commands to be entered from the debug serial input line. This signal is asserted as an output for three clock cycles when the chip enters Debug mode as a result of a debug request or as a result of meeting a breakpoint condition. The $\overline{\text{DE}}$ has an internal pull-up resistor. This signal is not a standard part of the JTAG TAP controller. The signal connects directly to the OnCE module to initiate debug mode directly or to provide a direct external indication that the chip has entered Debug mode. All other interface with the OnCE module must occur through the JTAG port.

2.4.4 Reset, Stop, Mode Select, and Interrupt Timing

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[6]

No.	Characteristics	Expression	150 MHz		Unit
			Min	Max	
8	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[3]	—	—	26.0	ns
9	Required $\overline{\text{RESET}}$ duration[4] • Power on, external clock generator, PLL disabled • Power on, external clock generator, PLL enabled • Power on, internal oscillator • During STOP, XTAL disabled (PCTL Bit 16 = 0) • During STOP, XTAL enabled (PCTL Bit 16 = 1) • During normal operation	Minimum: $50 \times ET_C$ $1000 \times ET_C$ $75000 \times ET_C$ $75000 \times ET_C$ $2.5 \times T_C$ $2.5 \times T_C$	 333.3 6.67 0.50 0.50 16.7 16.7	 — — — — — —	 ns µs ms ms ns ns
10	Delay from asynchronous $\overline{\text{RESET}}$ deassertion to first external address output (internal reset deassertion)[5] • Minimum • Maximum	$3.25 \times T_C + 2.0$ $20.25 \times T_C + 10$	23.7 —	— 145.0	ns ns
13	Mode select set-up time		30.0	—	ns
14	Mode select hold time		0.0	—	ns
15	Minimum edge-triggered interrupt request assertion width		6.6	—	ns
16	Minimum edge-triggered interrupt request deassertion width		6.6	—	ns
17	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory access address out valid • Caused by first interrupt instruction fetch • Caused by first interrupt instruction execution	Minimum: $4.25 \times T_C + 2.0$ $7.25 \times T_C + 2.0$	 30.4 51.0	 — —	 ns ns
18	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution	Minimum: $10 \times T_C + 5.0$	72.0	—	ns
19	Delay from address output valid caused by first interrupt instruction execute to interrupt request deassertion for level sensitive fast interrupts[1, 7, 8]	Maximum: $(WS + 3.75) \times T_C - 10.94$	—	Note 8	ns
20	Delay from $\overline{\text{RD}}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1, 7, 8]	Maximum: $(WS + 3.25) \times T_C - 10.94$	—	Note 8	ns
21	Delay from $\overline{\text{WR}}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1, 7, 8] • DRAM for all WS • SRAM WS = 1 • SRAM WS = 2, 3 • SRAM WS ≥ 4	Maximum: $(WS + 3.5) \times T_C - 10.94$ $(WS + 3.5) \times T_C - 10.94$ $(WS + 3) \times T_C - 10.94$ $(WS + 2.5) \times T_C - 10.94$	 — — — —	 Note 8 Note 8 Note 8 Note 8	 ns ns ns ns
24	Duration for $\overline{\text{IRQA}}$ assertion to recover from Stop state		5.9	—	ns
25	Delay from $\overline{\text{IRQA}}$ assertion to fetch of first instruction (when exiting Stop)[2, 3] • PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (Operating Mode Register Bit 6 = 0) • PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (Operating Mode Register Bit 6 = 1) • PLL is active during Stop (PCTL Bit 17 = 1) (Implies No Stop Delay)	$PLC \times ET_C \times PDF + (128\text{ K} - PLC/2) \times T_C$ $PLC \times ET_C \times PDF + (23.75 \pm 0.5) \times T_C$ $(8.25 \pm 0.5) \times T_C$	1.3 232.5 ns 51.7	9.1 12.3 ms 58.3	ms ns

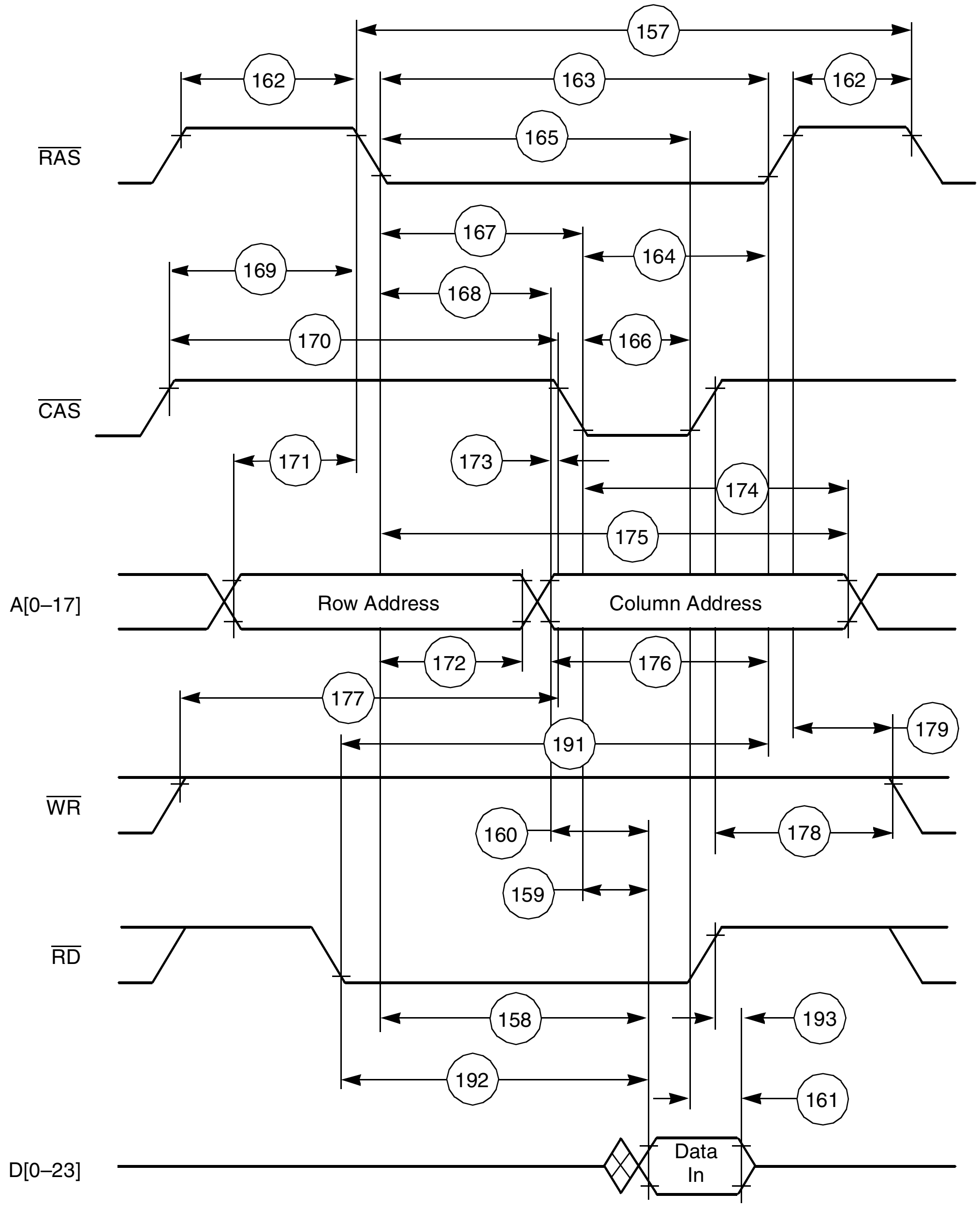


Figure 2-16. DRAM Out-of-Page Read Access

2.4.5.3 Asynchronous Bus Arbitration Timings

Table 2-13. Asynchronous Bus Timings

No.	Characteristics	Expression	150 MHz		Unit
			Min	Max	
250	$\overline{BB}$ assertion window from $\overline{BG}$ input deassertion.	$2.5 \times Tc + 5$	—	22	ns
251	Delay from $\overline{BB}$ assertion to $\overline{BG}$ assertion	$2 \times Tc + 5$	18.3	—	ns

Notes:
1. Bit 13 in the Operating Mode Register must be set to enable Asynchronous Arbitration mode.
2. At 150 MHz, Asynchronous Arbitration mode is recommended.
3. To guarantee timings 250 and 251, it is recommended that you assert non-overlapping $\overline{BG}$ inputs to different DSP56300 devices (on the same bus), as shown in **Figure 2-19**, where $\overline{BG1}$ is the $\overline{BG}$ signal for one DSP56300 device while $\overline{BG2}$ is the $\overline{BG}$ signal for a second DSP56300 device.

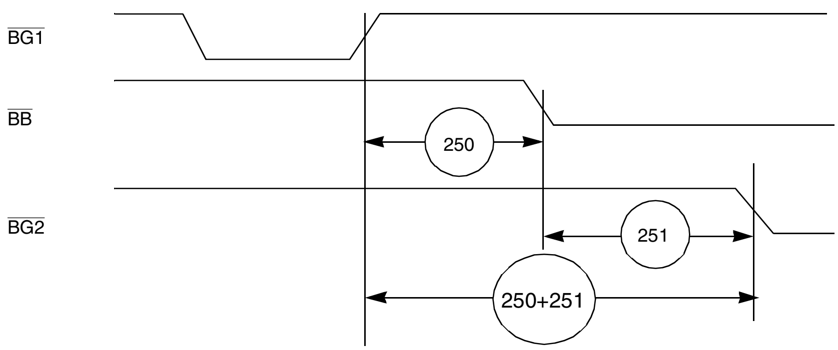


Figure 2-19. Asynchronous Bus Arbitration Timing

The asynchronous bus arbitration is enabled by internal synchronization circuits on $\overline{BG}$ and $\overline{BB}$ inputs. These synchronization circuits add delay from the external signal until it is exposed to internal logic. As a result of this delay, a DSP56300 part may assume mastership and assert $\overline{BB}$, for some time after $\overline{BG}$ is deasserted. This is the reason for timing 250.

Once $\overline{BB}$ is asserted, there is a synchronization delay from $\overline{BB}$ assertion to the time this assertion is exposed to other DSP56300 components that are potential masters on the same bus. If $\overline{BG}$ input is asserted before that time, and $\overline{BG}$ is asserted and $\overline{BB}$ is deasserted, another DSP56300 component may assume mastership at the same time. Therefore, some non-overlap period between one $\overline{BG}$ input active to another $\overline{BG}$ input active is required. Timing 251 ensures that overlaps are avoided.

2.4.6 Host Interface Timing

Table 2-14. Host Interface Timings[1,2,12]

No.	Characteristic[10]	Expression	150 MHz		Unit
			Min	Max	
317	Read data strobe assertion width[5] $\overline{\text{HACK}}$ assertion width	$T_C + 6.5$	13.1	—	ns
318	Read data strobe deassertion width[5] $\overline{\text{HACK}}$ deassertion width		6.5	—	ns
319	Read data strobe deassertion width[5] after “Last Data Register” reads[8,11], or between two consecutive CVR, ICR, or ISR reads[3] $\overline{\text{HACK}}$ deassertion width after “Last Data Register” reads[8,11]	$2.5 \times T_C + 4.4$	20.8	—	ns
320	Write data strobe assertion width[6]		8.7	—	ns
321	Write data strobe deassertion width[8] $\overline{\text{HACK}}$ write deassertion width • after ICR, CVR and “Last Data Register” writes • after IVR writes, or after TXH:TXM:TXL writes (with HLEND= 0), or after TXL:TXM:TXH writes (with HLEND = 1)	 $2.5 \times T_C + 4.4$	 20.8 10.9	 — —	 ns ns
322	$\overline{\text{HAS}}$ assertion width		6.5	—	ns
323	$\overline{\text{HAS}}$ deassertion to data strobe assertion[4]		0.0	—	ns
324	Host data input set-up time before write data strobe deassertion[6]		6.5	—	ns
325	Host data input hold time after write data strobe deassertion[6]		2.2	—	ns
326	Read data strobe assertion to output data active from high impedance[5] $\overline{\text{HACK}}$ assertion to output data active from high impedance		2.2	—	ns
327	Read data strobe assertion to output data valid[5] $\overline{\text{HACK}}$ assertion to output data valid		—	16.5	ns
328	Read data strobe deassertion to output data high impedance[5] $\overline{\text{HACK}}$ deassertion to output data high impedance		—	6.5	ns
329	Output data hold time after read data strobe deassertion[5] Output data hold time after $\overline{\text{HACK}}$ deassertion		2.2	—	ns
330	$\overline{\text{HCS}}$ assertion to read data strobe deassertion[5]	$T_C + 6.5$	13.1	—	ns
331	$\overline{\text{HCS}}$ assertion to write data strobe deassertion[6]		6.5	—	ns
332	$\overline{\text{HCS}}$ assertion to output data valid		—	13.0	ns
333	$\overline{\text{HCS}}$ hold time after data strobe deassertion[4]		0.0	—	ns
334	Address (HAD[0–7]) set-up time before $\overline{\text{HAS}}$ deassertion (HMUX=1)		3.0	—	ns
335	Address (HAD[0–7]) hold time after $\overline{\text{HAS}}$ deassertion (HMUX=1)		2.2	—	ns
336	HA[8–10] (HMUX=1), HA[0–2] (HMUX=0), HR/$\overline{\text{W}}$ set-up time before data strobe assertion[4] • Read • Write		 0 3.0	 — —	 ns ns
337	HA[8–10] (HMUX=1), HA[0–2] (HMUX=0), HR/$\overline{\text{W}}$ hold time after data strobe deassertion[4]		2.2	—	ns
338	Delay from read data strobe deassertion to host request assertion for “Last Data Register” read[5, 7, 8]	$T_C + 3.5$	10.1	—	ns
339	Delay from write data strobe deassertion to host request assertion for “Last Data Register” write[6, 7, 8]	$1.5 \times T_C + 3.5$	13.4	—	ns

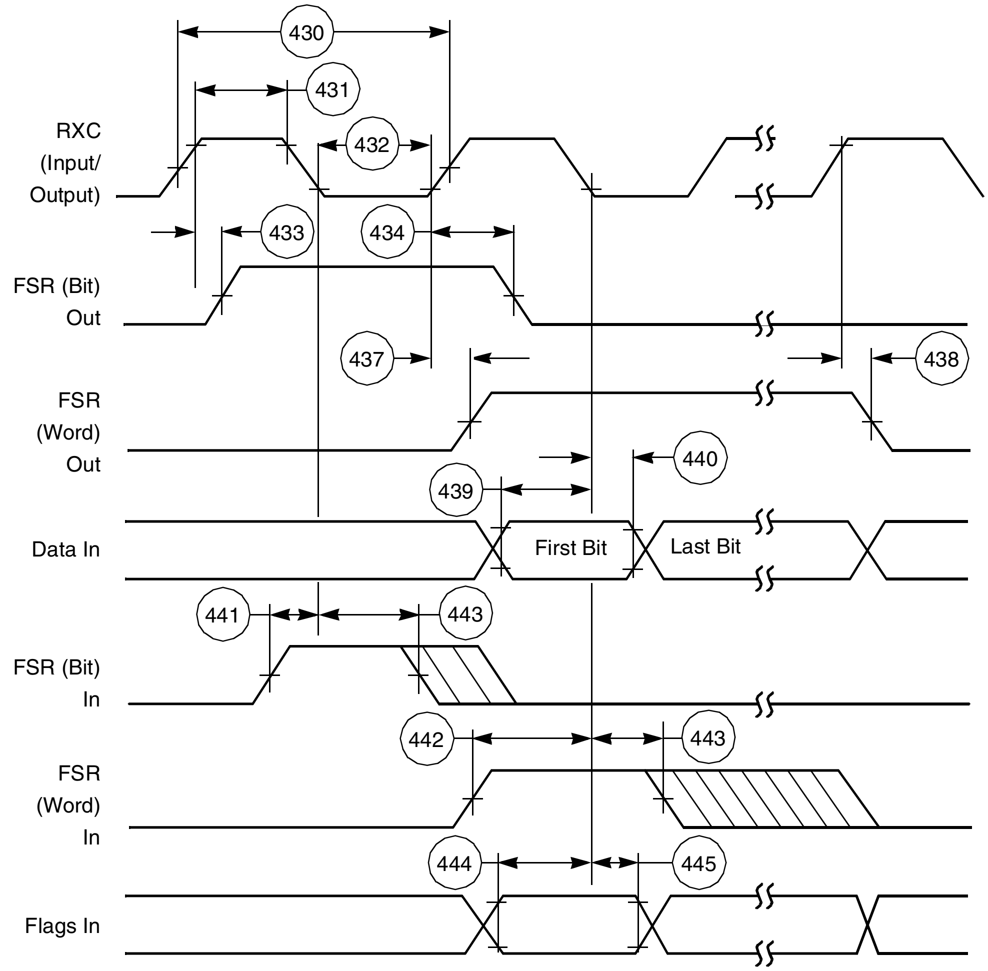


Figure 2-32. ESSI Receiver Timing

2.4.9 Timer Timing

Table 2-17. Timer Timing

No.	Characteristics	Expression	150 MHz		Unit
			Min	Max	
480	TIO Low	$2 \times T_C + 2.0$	15.4	—	ns
481	TIO High	$2 \times T_C + 2.0$	15.4	—	ns
Note:	$V_{CCQH} = 3.3$ V ± 0.3 V, $V_{CC} = 1.8$ V ± 0.1 V; $T_J = -40$°C to +100 °C, $C_L = 50$ pF				

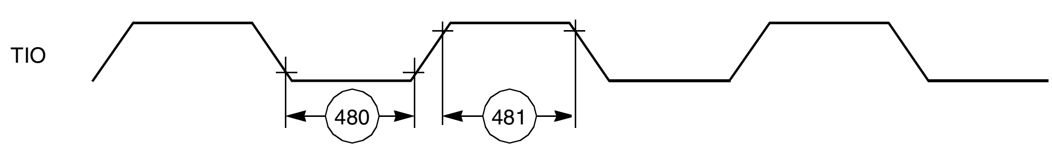


Figure 2-33. TIO Timer Event Input Restrictions

3.1 Package Description

Top and bottom views of the MAP-BGA packages are shown in **Figure 3-1** and **Figure 3-2** with their pin-outs.

Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	SC11	TMS	TDO	$\overline{IRQB}$	D23	V_{CCD}	D19	D16	D14	D11	D9	D7	NC
B	SRD1	SC12	TDI	$\overline{TRST}$	$\overline{IRQD}$	D21	D20	D17	D15	D13	D10	D8	D5	NC
C	SC02	STD1	TCK	$\overline{IRQA}$	$\overline{IRQC}$	D22	V_{CCQL}	D18	V_{CCD}	D12	V_{CCD}	D6	D3	D4
D	PINIT	SC01	$\overline{DE}$	GND	GND	GND	GND	GND	GND	GND	GND	D1	D2	V_{CCD}
E	STD0	V_{CCS}	SRD0	GND	GND	GND	GND	GND	GND	GND	GND	A17	A16	D0
F	RXD	SC10	SC00	GND	GND	GND	GND	GND	GND	GND	GND	V_{CCQH}	A14	A15
G	SCK1	SCLK	TXD	GND	GND	GND	GND	GND	GND	GND	GND	A13	V_{CCQL}	A12
H	V_{CCQH}	V_{CCQL}	SCK0	GND	GND	GND	GND	GND	GND	GND	GND	V_{CCA}	A10	A11
J	$\overline{HACK}$	HRW	$\overline{HDS}$	GND	GND	GND	GND	GND	GND	GND	GND	A8	A7	A9
K	V_{CCS}	$\overline{HREQ}$	TIO2	GND	GND	GND	GND	GND	GND	GND	GND	V_{CCA}	A5	A6
L	$\overline{HCS}$	TIO1	TIO0	GND	GND	GND	GND	GND	GND	GND	GND	V_{CCA}	A3	A4
M	HA1	HA2	HA0	V_{CCH}	H0	V_{CCP}	V_{CCQH}	EXTAL	CLKOUT	$\overline{BCLK}$	$\overline{WR}$	$\overline{RD}$	A1	A2
N	H6	H7	H4	H2	$\overline{RESET}$	GND_P	AA3	$\overline{CAS}$	V_{CCQL}	BCLK	$\overline{BR}$	V_{CCC}	AA0	A0
P	NC	H5	H3	H1	PCAP	GND_{P1}	AA2	XTAL	V_{CCC}	$\overline{TA}$	$\overline{BB}$	AA1	$\overline{BG}$	NC

Figure 3-1. DSP56311 MAP-BGA Package, Top View

Bottom View

	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	NC	D7	D9	D11	D14	D16	D19	V_{CCD}	D23	$\overline{IRQB}$	TDO	TMS	SC11	NC	A
B	NC	D5	D8	D10	D13	D15	D17	D20	D21	$\overline{IRQD}$	$\overline{TRST}$	TDI	SC12	SRD1	B
C	D4	D3	D6	V_{CCD}	D12	V_{CCD}	D18	V_{CCQL}	D22	$\overline{IRQC}$	$\overline{IRQA}$	TCK	STD1	SC02	C
D	V_{CCD}	D2	D1	GND	GND	GND	GND	GND	GND	GND	GND	$\overline{DE}$	SC01	PINIT	D
E	D0	A16	A17	GND	GND	GND	GND	GND	GND	GND	GND	SRD0	V_{CCS}	STD0	E
F	A15	A14	V_{CCQH}	GND	GND	GND	GND	GND	GND	GND	GND	SC00	SC10	RXD	F
G	A12	V_{CCQL}	A13	GND	GND	GND	GND	GND	GND	GND	GND	TXD	SCLK	SCK1	G
H	A11	A10	V_{CCA}	GND	GND	GND	GND	GND	GND	GND	GND	SCK0	V_{CCQL}	V_{CCQH}	H
J	A9	A7	A8	GND	GND	GND	GND	GND	GND	GND	GND	$\overline{HDS}$	HRW	$\overline{HACK}$	J
K	A6	A5	V_{CCA}	GND	GND	GND	GND	GND	GND	GND	GND	TIO2	$\overline{HREQ}$	V_{CCS}	K
L	A4	A3	V_{CCA}	GND	GND	GND	GND	GND	GND	GND	GND	TIO0	TIO1	$\overline{HCS}$	L
M	A2	A1	$\overline{RD}$	$\overline{WR}$	$\overline{BCLK}$	CLKOUT	EXTAL	V_{CCQH}	V_{CCP}	H0	V_{CCH}	HA0	HA2	HA1	M
N	A0	AA0	V_{CCC}	$\overline{BR}$	BCLK	V_{CCQL}	$\overline{CAS}$	AA3	GND_P	$\overline{RESET}$	H2	H4	H7	H6	N
P	NC	$\overline{BG}$	AA1	$\overline{BB}$	$\overline{TA}$	V_{CCC}	XTAL	AA2	GND_{P1}	PCAP	H1	H3	H5	NC	P

Figure 3-2. DSP56311 MAP-BGA Package, Bottom View

Table 3-1. Signal List by Ball Number (Continued)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
F6	GND	H3	SCK0 or PC3	J14	A9
F7	GND	H4	GND	K1	V_{CCS}
F8	GND	H5	GND	K2	$\overline{\text{HREQ}}$/HREQ, $\overline{\text{HTRQ}}$/HTRQ, or PB14
F9	GND	H6	GND	K3	TIO2
F10	GND	H7	GND	K4	GND
F11	GND	H8	GND	K5	GND
F12	V_{CCQH}	H9	GND	K6	GND
F13	A14	H10	GND	K7	GND
F14	A15	H11	GND	K8	GND
G1	SCK1 or PD3	H12	V_{CCA}	K9	GND
G2	SCLK or PE2	H13	A10	K10	GND
G3	TXD or PE1	H14	A11	K11	GND
G4	GND	J1	$\overline{\text{HACK}}$/HACK, $\overline{\text{HRRQ}}$/HRRQ, or PB15	K12	V_{CCA}
G5	GND	J2	HRW, $\overline{\text{HRD}}$/HRD, or PB11	K13	A5
G6	GND	J3	$\overline{\text{HDS}}$/HDS, $\overline{\text{HWR}}$/HWR, or PB12	K14	A6
G7	GND	J4	GND	L1	$\overline{\text{HCS}}$/HCS, HA10, or PB13
G8	GND	J5	GND	L2	TIO1
G9	GND	J6	GND	L3	TIO0
G10	GND	J7	GND	L4	GND
G11	GND	J8	GND	L5	GND
G12	A13	J9	GND	L6	GND
G13	V_{CCQL}	J10	GND	L7	GND
G14	A12	J11	GND	L8	GND
H1	V_{CCQH}	J12	A8	L9	GND
H2	V_{CCQL}	J13	A7	L10	GND

Table 3-1. Signal List by Ball Number (Continued)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
L11	GND	M13	A1	P1	NC
L12	V_{CCA}	M14	A2	P2	H5, HAD5, or PB5
L13	A3	N1	H6, HAD6, or PB6	P3	H3, HAD3, or PB3
L14	A4	N2	H7, HAD7, or PB7	P4	H1, HAD1, or PB1
M1	HA1, HA8, or PB9	N3	H4, HAD4, or PB4	P5	PCAP
M2	HA2, HA9, or PB10	N4	H2, HAD2, or PB2	P6	GND_{P1}
M3	HA0, $\overline{HAS}$/HAS, or PB8	N5	$\overline{RESET}$	P7	AA2/$\overline{RAS2}$
M4	V_{CCH}	N6	GND_P	P8	XTAL
M5	H0, HAD0, or PB0	N7	AA3/$\overline{RAS3}$	P9	V_{CCC}
M6	V_{CCP}	N8	CAS	P10	$\overline{TA}$
M7	V_{CCQH}	N9	V_{CCQL}	P11	$\overline{BB}$
M8	EXTAL	N10	BCLK[2]	P12	AA1/$\overline{RAS1}$
M9	CLKOUT[2]	N11	$\overline{BR}$	P13	$\overline{BG}$
M10	$\overline{BCLK}$[2]	N12	V_{CCC}	P14	NC
M11	$\overline{WR}$	N13	AA0/$\overline{RAS0}$		
M12	$\overline{RD}$	N14	A0		

Notes:
1. Signal names are based on configured functionality. Most connections supply a single signal. Some connections provide a signal with dual functionality, such as the MODx/$\overline{IRQx}$ pins that select an operating mode after $\overline{RESET}$ is deasserted but act as interrupt lines during operation. Some signals have configurable polarity; these names are shown with and without overbars, such as $\overline{HAS}$/HAS. Some connections have two or more configurable functions; names assigned to these connections indicate the function for a specific configuration. For example, connection N2 is data line H7 in non-multiplexed bus mode, data/address line HAD7 in multiplexed bus mode, or GPIO line PB7 when the GPIO function is enabled for this pin. Unlike in the TQFP package, most of the GND pins are connected internally in the center of the connection array and act as heat sink for the chip. Therefore, except for GND_P and GND_{P1} that support the PLL, other GND signals do not support individual subsystems in the chip.
2. CLKOUT, $\overline{BCLK}$, and BCLK are available only if the operating frequency is ≤100 MHz.

Table 3-2. Signal List by Signal Name

Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.
A0	N14	$\overline{\text{BR}}$	N11	D9	A12
A1	M13	$\overline{\text{CAS}}$	N8	$\overline{\text{DE}}$	D3
A10	H13	CLKOUT	M9	EXTAL	M8
A11	H14	D0	E14	GND	D4
A12	G14	D1	D12	GND	D5
A13	G12	D10	B11	GND	D6
A14	F13	D11	A11	GND	D7
A15	F14	D12	C10	GND	D8
A16	E13	D13	B10	GND	D9
A17	E12	D14	A10	GND	D10
A2	M14	D15	B9	GND	D11
A3	L13	D16	A9	GND	E4
A4	L14	D17	B8	GND	E5
A5	K13	D18	C8	GND	E6
A6	K14	D19	A8	GND	E7
A7	J13	D2	D13	GND	E8
A8	J12	D20	B7	GND	E9
A9	J14	D21	B6	GND	E10
AA0	N13	D22	C6	GND	E11
AA1	P12	D23	A6	GND	F4
AA2	P7	D3	C13	GND	F5
AA3	N7	D4	C14	GND	F6
$\overline{\text{BB}}$	P11	D5	B13	GND	F7
$\overline{\text{BCLK}}$	M10	D6	C12	GND	F8
BCLK	N10	D7	A13	GND	F9
$\overline{\text{BG}}$	P13	D8	B12	GND	F10

Power Consumption Benchmark A

The following benchmark program evaluates DSP56311 power use in a test situation. It enables the PLL, disables the external clock, and uses repeated multiply-accumulate (MAC) instructions with a set of synthetic DSP application data to emulate intensive sustained DSP operation.

```
;**************************************************************************
;**************************************************************************
;*                                                                        *
;*                     CHECKS   Typical Power Consumption                  *
;*                                                                        *
;**************************************************************************

        page    200,55,0,0,0
        nolist

I_VEC EQU $000000                   ; Interrupt vectors for program debug only
START EQU $8000                     ; MAIN (external) program starting address
INT_PROG  EQU $100                  ; INTERNAL program memory starting address
INT_XDAT  EQU $0                    ; INTERNAL X-data memory starting address
INT_YDAT  EQU $0                    ; INTERNAL Y-data memory starting address

        INCLUDE "ioequ.asm"
        INCLUDE "intequ.asm"

        list

        org     P:START
;
        movep #$0243FF,x:M_BCR ;    ; BCR: Area 3 = 2 w.s (SRAM)
                                    ; Default: 2w.s (SRAM)
;
        movep   #$0d0000,x:M_PCTL   ; XTAL disable
                                    ; PLL enable
                                    ; CLKOUT disable
;
                                    ; Load the program
;
        move    #INT_PROG,r0
        move    #PROG_START,r1
        do      #(PROG_END-PROG_START),PLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,p:(r0)+
        nop
PLOAD_LOOP
;
                                    ; Load the X-data
;
        move    #INT_XDAT,r0
        move    #XDAT_START,r1
        do      #(XDAT_END-XDAT_START),XLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,x:(r0)+
```

```
I_SCIIL EQU I_VEC+$56                ; SCI Idle Line
I_SCITM EQU I_VEC+$58                ; SCI Timer

;-------------------------------------------------------------------------
; HOST Interrupts
;-------------------------------------------------------------------------
I_HRDF EQU I_VEC+$60                 ; Host Receive Data Full
I_HTDE EQU I_VEC+$62                 ; Host Transmit Data Empty
I_HC EQU I_VEC+$64                   ; Default Host Command
;------------------------------------------------------------------------
; EFCOP Filter Interrupts
;------------------------------------------------------------------------

I_FDIIE  EQU     I_VEC+$68           ; EFilter input buffer empty
I_FDOIE  EQU     I_VEC+$6A           ; EFilter output buffer full

;-------------------------------------------------------------------------
; INTERRUPT ENDING ADDRESS
;-------------------------------------------------------------------------
I_INTEND EQU I_VEC+$FF               ; last address of interrupt vector space
```