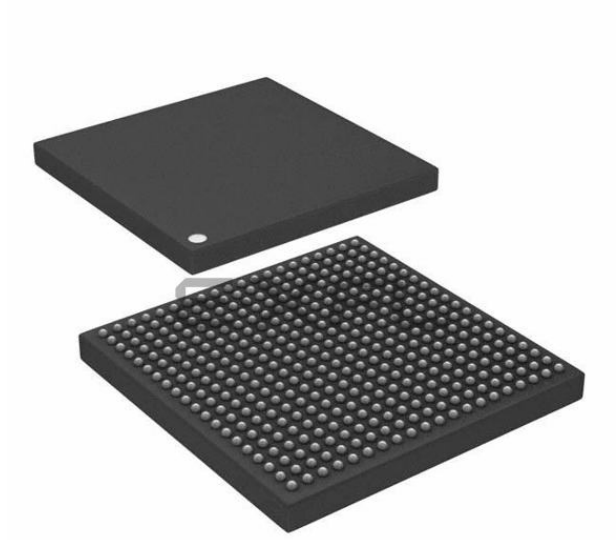


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Boot Security, Cryptography, Secure JTAG
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx502cvm8b

Table 4. i.MX50 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SDMA	Smart Direct Memory Access	Master Connectivity Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by offloading various cores in dynamic data routing. The SDMA features list is as follows: • Powered by a 16-bit instruction-set micro-RISC engine • Multi-channel DMA supports up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM Cortex-A8 and SDMA • Very fast context-switching with two-level priority-based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle uni-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers for EMI • Support of byte-swapping and CRC calculations • A library of scripts and API is available
SJC	Secure JTAG Controller	System Control Peripherals	The Secure JTAG Controller provides a mechanism for regulating JTAG access, preventing unauthorized JTAG usage while allowing JTAG access for manufacturing tests and software debugging. The i.MX50 JTAG port provides debug access to several hardware blocks including the ARM processor and the system bus, therefore, it must be accessible for initial laboratory bring-up, manufacturing tests and troubleshooting, and for software debugging by authorized entities. However, if the JTAG port is left unsecured it provides a method for executing unauthorized program code, getting control over secure applications, and running code in privileged modes. The Secure JTAG controller provides three different security modes that can be selected through an e-fuse configuration to prevent unauthorized JTAG access.
SPBA	Shared Peripheral Bus Arbiter	System Control Peripherals	SPBA (Shared Peripheral Bus Arbiter) is a two-to-one IP bus interface (IP bus) arbiter.
SRTC	Secure Real Time Clock	Security Peripherals	The SRTC incorporates a special System State Retention Register (SSRR) that stores system parameters during system shutdown modes. This register and all SRTC counters are powered by dedicated supply rail NVCC_SRTC. The NVCC_SRTC can be energized separately even if all other supply rails are shut down. This register is helpful for storing warm boot parameters. The SSRR also stores the system security state. In case of a security violation, the SSRR marks the event (security violation indication).

- All other supply voltages at nominal levels
- External (MHz) crystal and on-chip oscillator disabled
- CKIL input ON with 32 kHz signal present
- All PLLs OFF, all CCM-generated clocks OFF
- All modules disabled
- No external resistive loads that cause current

4.1.6 USB-OH-1 (OTG + 1 Host Port) Current Consumption

Table 17 shows the USB interface current consumption.

Table 17. USB Interface Current Consumption

Parameter	Conditions		Typical @ 25 °C	Max	Unit
Analog supply 3.3 V USB_H1_VDDA33 USB_OTG_VDDA33	Full speed	RX	5.5	6	mA
		TX	7	8	
	High speed	RX	5	6	
		TX	5	6	
Analog supply 2.5 V USB_H1_VDDA25 USB_OTG_VDDA25	Full speed	RX	6.5	7	mA
		TX	6.5	7	
	High speed	RX	12	13	
		TX	21	22	
Digital supply VCC (1.2 V)	Full speed	RX	6	7	mA
		TX	6	7	
	High speed	RX	6	7	
		TX	6	7	

4.2 Supply Power-Up/Power-Down Requirements and Restrictions

The system design must comply with the power-up and power-down sequence guidelines as described in this section to guarantee reliable operation of the device. Any deviation from these sequences can result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the i.MX50 processor (worst-case scenario)

4.4.1 GPIO Output Buffer Impedance

Table 24 shows the GPIO output buffer impedance of the i.MX50 processor.

Table 24. GPIO Output Buffer Impedance

Parameter	Symbol	Test Conditions	Min	Typ		Max	Unit
				OVDD 2.775 V	OVDD 1.875V		
Output driver impedance	Rpu	Low drive strength, Ztl = 150 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω Max drive strength, Ztl = 37.5 Ω	80 40 27 20	104 52 35 26	150 75 51 38	250 125 83 62	Ω
Output driver impedance	Rpd	Low drive strength, Ztl = 150 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω Max drive strength, Ztl = 37.5 Ω	64 32 21 16	88 44 30 22	134 66 44 34	243 122 81 61	Ω

4.4.2 LVIO Output Buffer Impedance

Table 25 shows the LVIO output buffer impedance of the i.MX50 processor.

Table 25. LVIO Output Buffer Impedance

Parameter	Symbol	Test Conditions	Min	Typ		Max	Unit
				OVDD 2.775 V	OVDD 1.875V		
Output driver impedance	Rpu	Low drive strength, Ztl = 150 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω Max drive strength, Ztl = 37.5 Ω	80 40 27 20	104 52 35 26	150 75 51 38	250 125 83 62	Ω
Output driver impedance	Rpd	Low drive strength, Ztl = 150 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω Max drive strength, Ztl = 37.5 Ω	64 32 21 16	88 44 30 22	134 66 44 34	243 122 81 61	Ω

4.5.8 LPDDR1 I/O AC Parameters

Table 34 shows the AC parameters for LPDDR1 I/O.

Table 34. LPDDR1 I/O AC Parameters

Parameter	Symbol	Min	Max	Unit
AC input logic high	Vihd(ac)	0.8*ovdd	ovdd+0.3	V
AC input logic low	Vild(ac)	-0.3	0.2*ovdd	
AC input differential voltage[1]	Vid(ac)	0.6*ovdd	ovdd+0.6	
AC input differential crosspoint voltage[2]	Vix(ac)	0.4*ovdd	0.6*ovdd	
Output propagation delay high to low	tPOHLD		2.5	ns
Output propagation delay low to high	tPOLHD		2.5	
Input propagation delay high to low	tPIHLD		1.5	
Input propagation delay low to high	tPILHD		1.5	
Single output slew rate	tsr	0.3	2.5	V/ns

[1]Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac)-Vil(ac)

[2]The typical value of Vix(ac) is expected to be about 0.5*ovdd. and Vix(ac) is expected to track variation of ovdd. Vix(ac) indicates the voltage at which differential input signal must cross.

4.5.9 LPDDR2 I/O AC Parameters

Table 35 shows the AC parameters for LPDDR2 I/O.

Table 35. LPDDR2 I/O AC Parameters

Parameter	Symbol	Min	Max	Unit
AC input logic high	Vih(ac)	Vref+0.22	ovdd	V
AC input logic low	Vil(ac)	ovss	Vref-0.22	
AC differential input high voltage[1]	Vidh(ac)	0.44	-	
AC differential input low voltage	Vidhl(ac)	-	0.44	
AC input differential cross point voltage (relative to ovdd / 2)[2]	Vix(ac)	-0.12	0.12	
Over/undershoot peak	Vpeak		0.35	ns
Over/undershoot area (above OVDD or below OVSS)	Varea		0.6 (at 266 MHz)	V-ns
Output propagation delay high to low	tPOHLD		3.5	ns
Output propagation delay low to high	tPOLHD		3.5	
Input propagation delay high to low	tPIHLD		1.5	
Input propagation delay low to high	tPILHD		1.5	

Table 37. WDOG_RST_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC5	Duration of WDOG_RST_B Assertion	1	—	T_{CKIL}

NOTE

CKIL is approximately 32 kHz. T_{CKIL} is one period or approximately 30 µs.

4.6.3 Clock Amplifier Parameters (CKIH)

The input to clock amplifier (CAMP) is internally ac-coupled allowing direct interface to a square wave or sinusoidal frequency source. No external series capacitors are required.

Table 38 shows the electrical parameters of CAMP.

Table 38. CAMP Electrical Parameters (CKIH)

Parameter	Min	Typ	Max	Unit
Input frequency	8.0	—	40.0	MHz
VIL (for square wave input)	0	—	0.3	V
VIH (for square wave input)	(VCC[1] – 0.25)	—	3	V
Sinusoidal input amplitude	0.4 [2]	—	VDD	Vp-p
Output duty cycle	45	50	55	%

1 VCC is the supply voltage of CAMP.

2 This value of the sinusoidal input is determined during characterization.

4.6.4 DPLL Electrical Parameters

Table 39 shows the electrical parameters of digital phase-locked loop (DPLL).

Table 39. DPLL Electrical Parameters

Parameter	Test Conditions/Remarks	Min	Typ	Max	Unit
Reference clock frequency range[1]	—	10	—	100	MHz
Reference clock frequency range after pre-divider	—	10	—	40	MHz
Output clock frequency range (dpdck_2)	—	300	—	1025	MHz
Pre-division factor[2]	—	1	—	16	—
Multiplication factor integer part	—	5	—	15	—
Multiplication factor numerator[3]	Should be less than denominator	–67108862	—	67108862	—
Multiplication factor denominator[2]	—	1	—	67108863	—
Output duty cycle	—	48.5	50	51.5	%

Table 43. EIM Bus Timing Parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	EIM_BCLK Cycle time[2]	t	—	2t	—	3t	—	4t	—
WE2	EIM_BCLK Low Level Width	0.4t	—	0.8t	—	1.2t	—	1.6t	—
WE3	EIM_BCLK High Level Width	0.4t	—	0.8t	—	1.2t	—	1.6t	—
WE4	Clock rise to address valid[3]	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE5	Clock rise to address invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE6	Clock rise to EIM_CSx valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE7	Clock rise to EIM_CSx invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE8	Clock rise to EIM_RW valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE9	Clock rise to EIM_RW invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE10	Clock rise to EIM_OE valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE11	Clock rise to EIM_OE invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE12	Clock rise to EIM_EBx valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE13	Clock rise to EIM_EBx invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE14	Clock rise to EIM_LBA valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE15	Clock rise to EIM_LBA invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE16	Clock rise to Output Data valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	2t – 1.25	2t + 1.75
WE17	Clock rise to Output Data Invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	2t – 1.25	2t + 1.75
WE18	Input Data setup time to Clock rise	2	—	2	—	2	—	2	—
WE19	Input Data hold time from Clock rise	2.5	—	2.5	—	2.5	—	2.5	—
WE20	EIM_WAIT setup time to Clock rise	2	—	2	—	2	—	2	—
WE21	EIM_WAIT hold time from Clock rise	2.5	—	2.5	—	2.5	—	2.5	—

1 *t* is axi_clk cycle time. The maximum allowed axi_clk frequency is 133 MHz, whereas the maximum allowed EIM_BCLK frequency is 66.5 MHz. As a result, if BCD = 0, axi_clk must be ≤ 66.5 MHz. If BCD = 1, then 133 MHz is allowed for axi_clk, resulting in a EIM_BCLK of 66.5 MHz. When the clock branch to EIM is decreased to 66.5 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM) for a detailed clock tree description.

[2] EIM_BCLK parameters are being measured from the 50% point that is, high is defined as 50% of signal value and low is defined as 50% as signal value.

[3] For signal measurements *High* is defined as 80% of signal value and *Low* is defined as 20% of signal value.

4.7.2 Examples of EIM Accesses

Figure 19, Figure 20, Figure 21, Figure 22, Figure 23, and Figure 24 give a few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

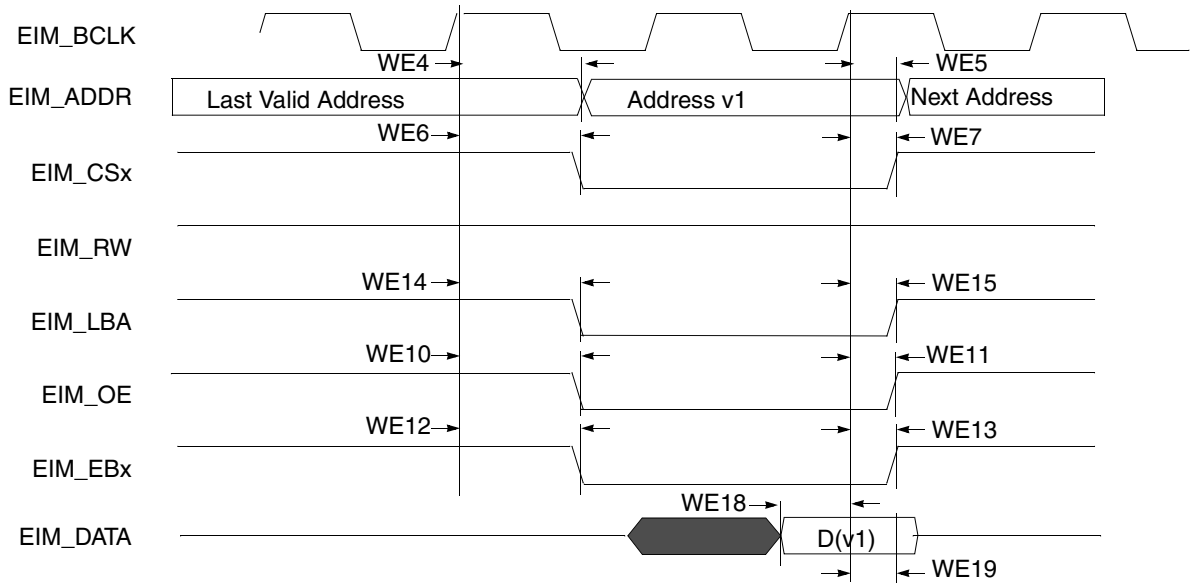


Figure 19. Synchronous Memory Read Access, WSC=1

Table 47. DDR Output AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR16 CK >= 200 MHz	DQ & DQM output hold time relative to DQS	tDH	0.5 tCK - 1.3	—	ns
DDR15 CK < 200 MHz	DQ & DQM output setup time relative to DQS	tDS	1	—	ns
DDR16 CK < 200 MHz	DQ & DQM output hold time relative to DQS	tDH	1	—	ns

NOTE

The DDR15,16 could be adjusted by the parameter “DLL_WR_DELAY”;

The ideal case is that SDQS is center aligned to the DRAM_D data valid window;

For this table, HW_DRAM_PHY15[14:8] (DLL_WR_DELAY) = 0x10;

4.8.4 DRAM Data Input Timing

DRAM Data input timing is defined for all DDR types: DDR2, LPDDR1, and LPDDR2.

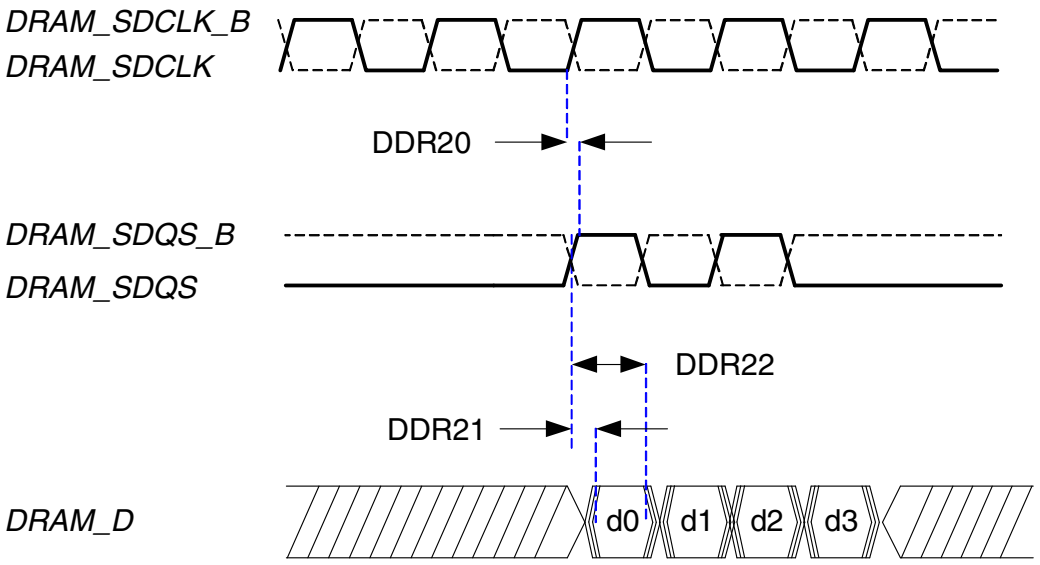


Figure 31. DRAM Data Input Timing

Table 48. DDR2 Input AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR20	Positive DQS latching edge to associated CK edge	tDQSCK	-0.5 tCK	—	ns

Table 48. DDR2 Input AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR21	DQS to DQ input skew	tDQSQ	—	0.65	ns
DDR22	DQS to DQ input hold time	tQH	0.45 tCK -0.85	—	ns

NOTE

The timing parameter DDR20(tDQSCK) is not strictly required by this DRAM MC design.

4.9 External Peripheral Interfaces

The following sections provide information on external peripheral interfaces.

4.9.1 AUDMUX Timing Parameters

The AUDMUX provides programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is hence governed by the SSI module.

4.9.2 CSPI and eCSPI Timing Parameters

This section describes the timing parameters of the CSPI and eCSPI modules. The CSPI and eCSPI have separate timing parameters for master and slave modes. The nomenclature used with the CSPI/eCSPI modules and the respective routing of these signals is shown in Table 49.

Table 49. CSPI Nomenclature and Routing

Module	I/O Access
eCSPI1	GPIO, KPP, DISP0_DAT, CSI0_DAT, and EIM_D through IOMUX
eCSPI2	DISP0_DAT, CSI0_DAT, and EIM through IOMUX
CSPI	DISP0_DAT, EIM_A/D, SD1, and SD2 through IOMUX

4.9.3 Enhanced Secured Digital Host Controller (eSDHCv2/v3) and uSDHC AC Timing

This section describes the electrical information of the eSDHCv2/v3 and the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4 (Dual Date Rate) timing.

4.9.3.1 SD/eMMC4.3 (Single Data Rate) eSDHCv3 and uSDHC AC Timing

Figure 36 depicts the timing of SD/eMMC4.3, and Table 54 lists the SD/eMMC4.3 timing characteristics.

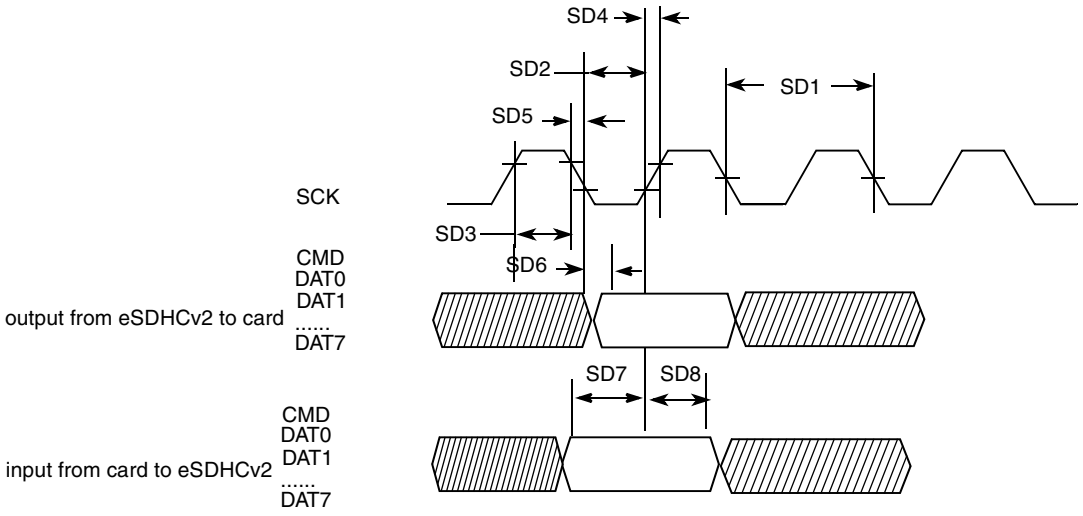


Figure 36. SD/eMMC4.3 Timing

Table 54. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns

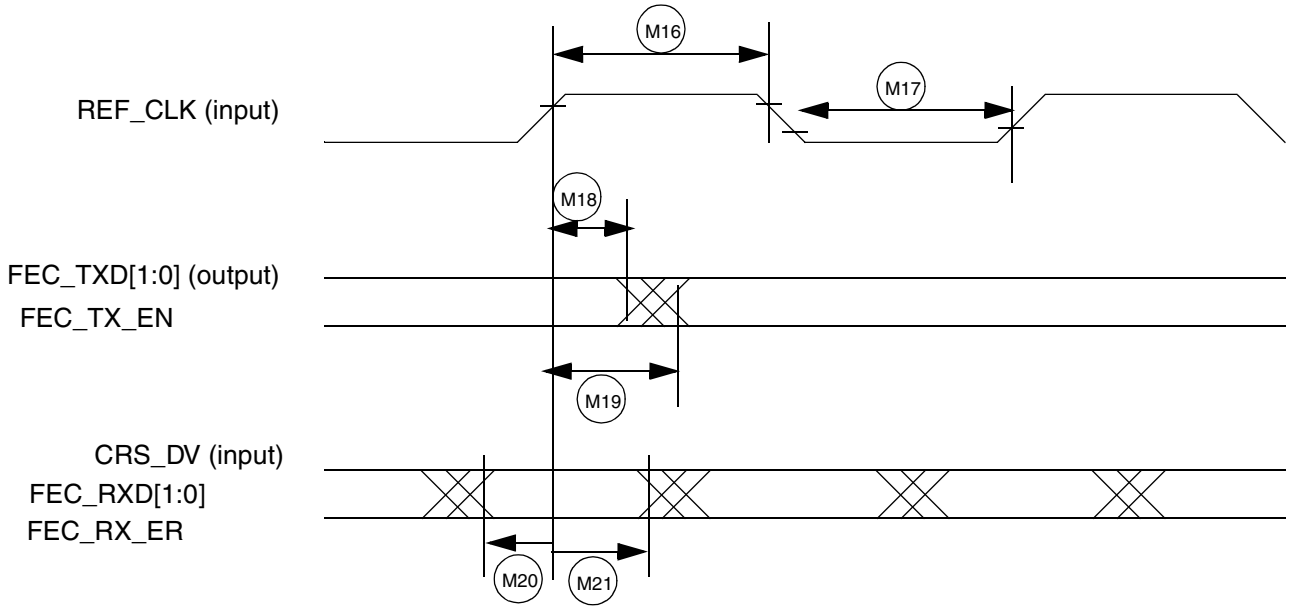


Figure 40. RMII Mode Signal Timing Diagram

4.9.5 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 41 depicts the timing of I²C module, and Table 59 lists the I²C module timing characteristics.

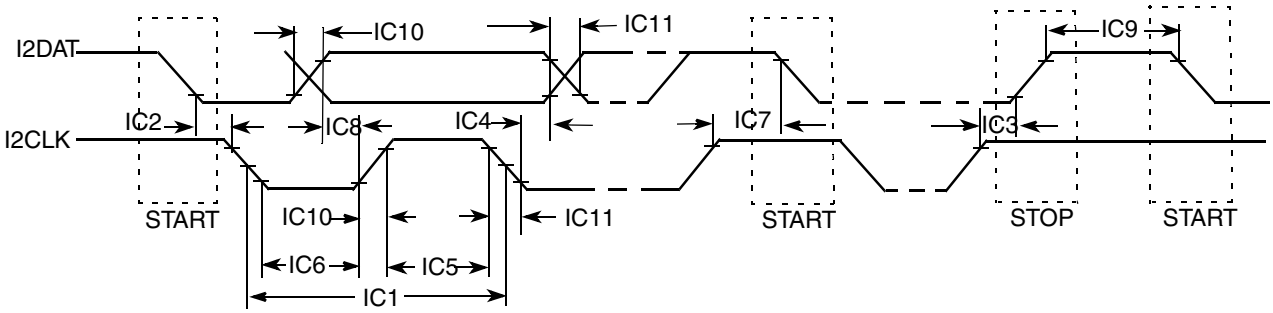


Figure 41. I²C Bus Timing

Table 59. I²C Module Timing Parameters

ID	Parameter	Standard Mode Supply Voltage = 1.65 V–1.95 V, 2.7 V–3.3 V		Fast Mode Supply Voltage = 2.7 V–3.3 V		Unit
		Min	Max	Min	Max	
IC1	I2CLK cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs

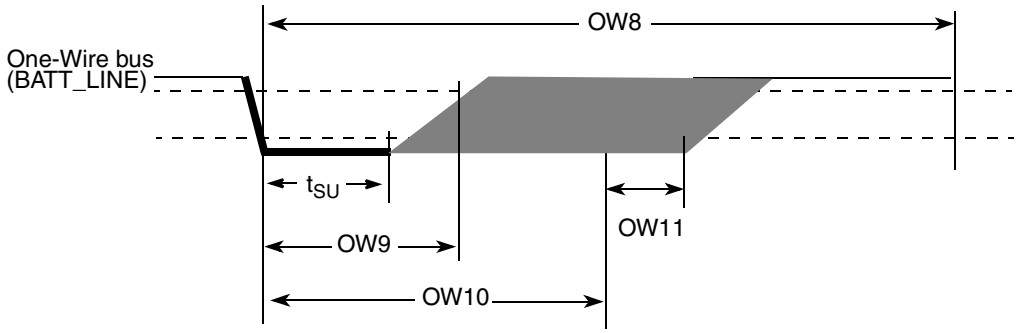


Figure 45. Read Sequence Timing Diagram

Table 62. WR1 /RD Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Unit
OW7	Write 1 Low Time	t_{LOW1}	1	5	15	µs
OW8	Transmission Time Slot	t_{SLOT}	60	117	120	µs
—	Read Data Setup	t_{SU}	—	—	1	µs
OW9	Read Low Time	t_{LOWR}	1	5	15	µs
OW10	Read Data Valid	t_{RDV}	—	15	—	µs
OW11	Release Time	$t_{RELEASE}$	0	—	45	µs

4.9.7 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 46 depicts the timing of the PWM, and Table 63 lists the PWM timing parameters.

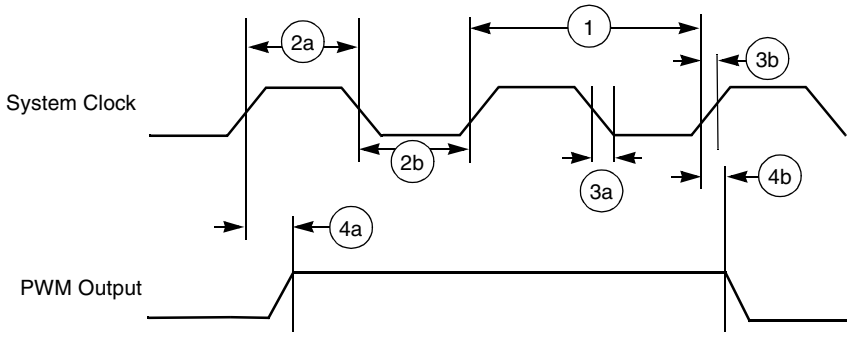
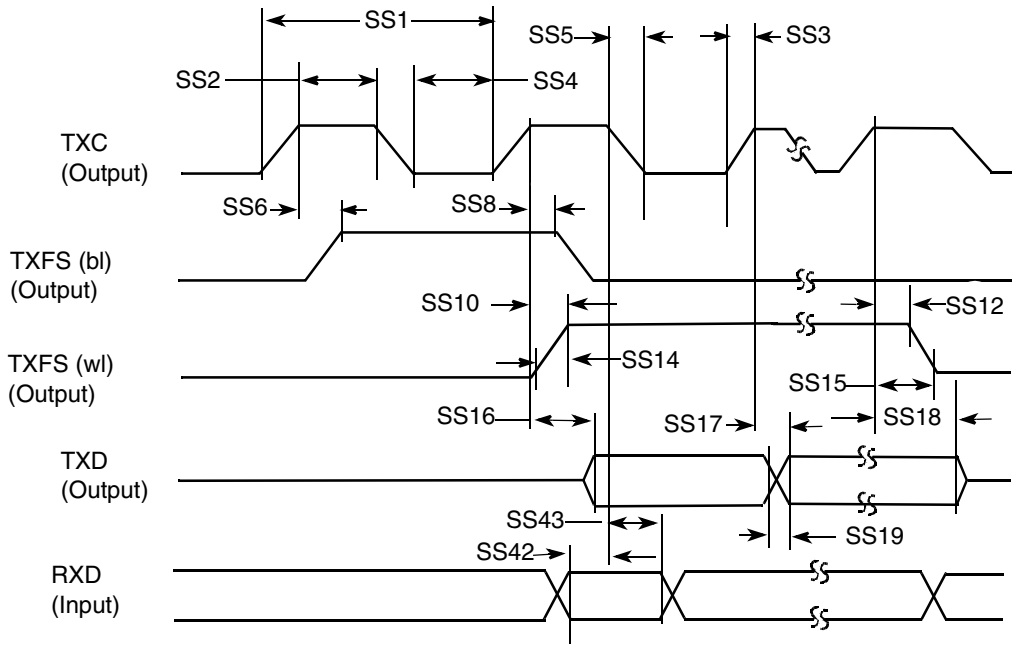


Figure 46. PWM Timing

4.9.9.1 SSI Transmitter Timing with Internal Clock

Figure 51 depicts the SSI transmitter internal clock timing and Table 66 lists the timing parameters for the SSI transmitter internal clock.



Note: SRXD input in synchronous mode only

Figure 51. SSI Transmitter Internal Clock Timing Diagram

Table 66. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6.0	ns
SS15	(Tx/Rx) Internal FS fall time	—	6.0	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns

4.9.9.3 SSI Transmitter Timing with External Clock

Figure 53 depicts the SSI transmitter external clock timing and Table 68 lists the timing parameters for the transmitter timing with external clock.

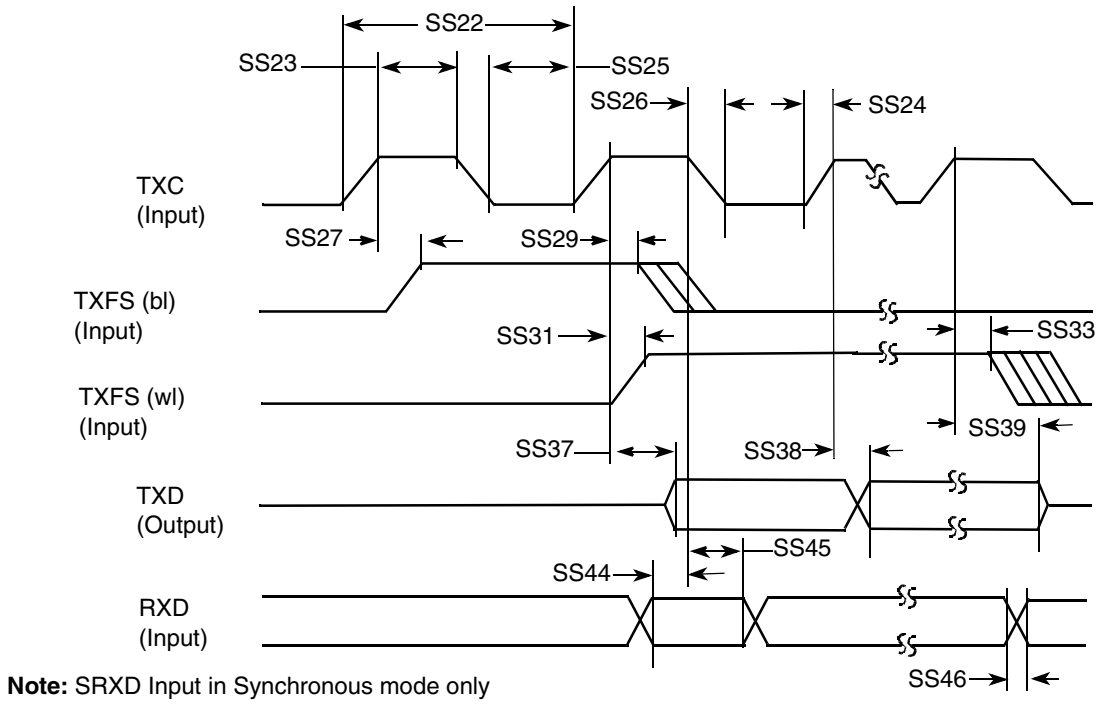


Figure 53. SSI Transmitter External Clock Timing Diagram

Table 68. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	–10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	–10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns

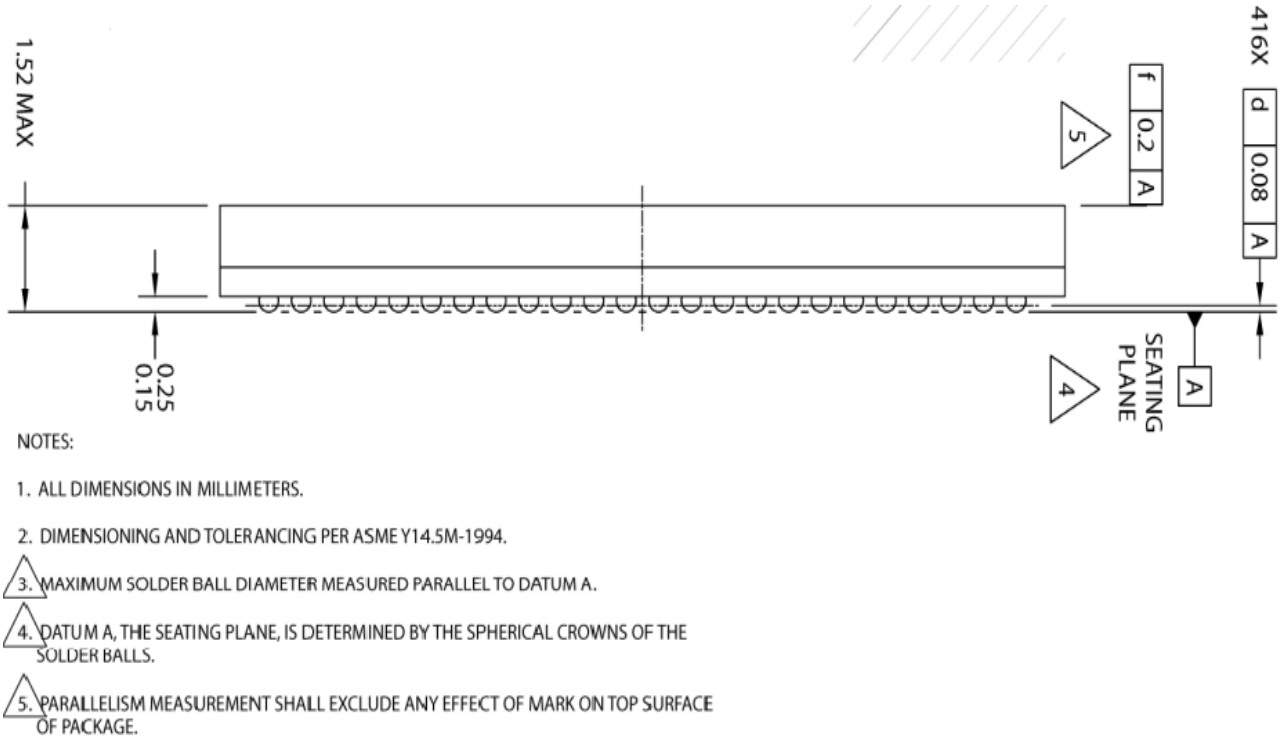


Figure 61. 416 MAPBGA 13x13 mm Package Side View

The following notes apply to Figure 59, Figure 60, and Figure 61:

- Unless otherwise specified dimensions are in millimeters.
- All dimensions and tolerances conform to ASME Y14.5M-1994.
- Parallelism measurement shall exclude any effect of mark on top surface of package.

Table 82. 416 PoPBGA 13 x 13 mm Ground, Power, Sense, and Reference Contact Signals (continued)

NVCC_RESET	V8	—
NVCC_SD1	T7	—
NVCC_SD2	U8	—
NVCC_SPI	R7	—
NVCC_SRTC	AA1	—
NVCC_SSI	R8	—
NVCC_UART	T8	—
POP_EMMC_RST	A19	This is PoP eMMC 4.4 NAND Reset input pin. This pin does not connect to the i.MX50. If using eMMC 4.4 NAND, this pin can be connected to a GPIO. For non 4.4 eMMC applications, leave floating.
POP_LPDDR2_1.8V	A20, B19, B20, M5, N5	This is the 1.8V supply for the PoP LPDDR2. These pins do not connect to the i.MX50.
POP_LPDDR2_ZQ0	AA24	This is the PoP LPDDR2 ZQ0 pin. This pin does not connect to the i.MX50. This should be connected on the PCB to a 240 Ω 1% resistor to ground
POP_LPDDR2_ZQ1	AA23	This is the PoP LPDDR2 ZQ1 pin. This pin does not connect to the i.MX50. If used, this should be connected on the PCB to a 240 Ω 1% resistor to ground
POP_NAND_VCC	D19, D20	This is the 3.3V I/O and memory supply for the PoP eMMC NAND. Note that because the eMMC memory and I/O domains are shorted together, it is not possible to support 1.8 V I/O for the PoP eMMC NAND.
USB_VDDA25	AC9, AD9	Note that on the PoPBGA package, USB_OTG_VDDA25 and USB_H1_VDDA25 are shorted together.
USB_VDDA33	AC11, AD11	Note that on the PoPBGA package, USB_OTG_VDDA33 and USB_H1_VDDA33 are shorted together.
VCC	H14, H15, H16, H17, J17, K14, K15, K17, L15	—
VDD_DCDCI	Y6	—
VDD_DCDCO	Y5	—
VDD1P2	AD6	—
VDD1P8	AD7	—

Table 84. 400 MAPBGA 17x17 Ground, Power, Sense, and Reference Contact Signals (continued)

VDD_DCDCI	R7
VDD_DCDCO	T6
GND_DCDC	R6

5.4 Signal Assignments

Table 85. Alphabetical List of Signal Assignments

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
BOOT_MODE0	AB1	AB1	V3	NVCC_RESET	LVIO	ALT0	IN	100K PU
BOOT_MODE1	AB2	AB2	U3	NVCC_RESET	LVIO	ALT0	IN	100K PU
CHGR_DET_B	V11	AA15	T10	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG25	—	OUT-OD	—
CKIH	AA6	AA6	V4	NVCC_JTAG	ANALOG	—	—	—
CKIL	Y1	Y1	Y4	NVCC_SRTC	ANALOG	—	—	—
CSPI_MISO	M5	H2	K4	NVCC_SPI	HVIO	ALT1	IN	Keeper
CSPI_MOSI	M2	J1	L3	NVCC_SPI	HVIO	ALT1	IN	Keeper
CSPI_SCLK	M1	H1	M1	NVCC_SPI	HVIO	ALT1	IN	Keeper
CSPI_SS0	M4	J2	J4	NVCC_SPI	HVIO	ALT1	IN	Keeper
DISP_BUSY	AC12	AA21	U11	NVCC_LCD	HVIO	ALT1	IN	Keeper
DISP_CS	AD14	AC21	T12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D0	AA12	AC17	V11	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D1	Y12	AC16	T11	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D10	Y17	AD22	Y16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D11	V12	AD19	W14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D12	V13	AC22	V14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D13	V14	AC23	T13	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D14	V15	AB23	U14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D15	V16	AD21	Y15	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D2	AA13	AD15	W12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D3	Y13	AC15	W13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D4	AA14	AC24	Y13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D5	Y14	AB24	U13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
ECSPI1_SCLK	N1	M4	N2	NVCC_SPI	HVIO	ALT1	IN	Keeper
ECSPI1_SS0	P7	L4	N3	NVCC_SPI	HVIO	ALT1	IN	Keeper
ECSPI2_MISO	N5	L2	L4	NVCC_SPI	HVIO	ALT1	IN	Keeper
ECSPI2_MOSI	P5	K2	N1	NVCC_SPI	HVIO	ALT1	IN	Keeper
ECSPI2_SCLK	P4	L1	N4	NVCC_SPI	HVIO	ALT1	IN	Keeper
ECSPI2_SS0	N4	K1	M2	NVCC_SPI	HVIO	ALT1	IN	Keeper
EIM_BCLK	A5	A12	A5	NVCC_EIM	HVIO	ALT0	OUT-LO	100K PU
EIM_CRE	A3	D13	A3	NVCC_EIM	HVIO	ALT0	OUT-LO	100K PU
EIM_CS0	B10	B24	B11	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU
EIM_CS1	D10	D17	C9	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU
EIM_CS2	E10	D16	D9	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU
EIM_DA0	A9	B23	B10	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA1	B9	C24	B9	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA10	D7	A14	C6	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA11	E7	B16	D6	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA12	A6	A16	A6	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA13	B6	A15	B6	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA14	D6	A13	C5	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA15	E6	B15	D5	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA2	D9	C23	C8	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA3	E9	A22	D8	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA4	A8	A23	A9	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA5	B8	B22	B8	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA6	D8	B18	C7	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA7	E8	B17	D7	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA8	A7	A18	A7	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA9	B7	A17	B7	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_EB0	A4	D15	A4	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU
EIM_EB1	B4	D14	B4	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU
EIM_LBA	E5	B13	D4	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
EIM_OE	B3	B12	B3	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU
EIM_RDY	A2	B11	A2	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_RW	B5	B14	B5	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU
EIM_WAIT	D5	A11	C4	NVCC_EIM	HVIO	ALT0	IN	100K PU
EPDC_BDR0	E20	Y21	A15	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_BDR1	E21	Y23	D16	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D0	A17	Y24	B15	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D1	B17	W24	A14	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D10	D15	V23	D13	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D11	E15	R21	F14	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D12	A14	J23	F13	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D13	B14	M21	E14	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D14	D14	N21	E11	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D15	E14	P21	E13	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D2	D17	U23	B16	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D3	E17	V24	C16	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D4	A16	R24	D15	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D5	B16	T24	A13	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D6	D16	U24	C14	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D7	E16	T23	D14	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D8	A15	W23	E15	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_D9	B15	T21	E16	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_GDCLK	A11	G24	A11	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_GDOE	B11	J24	C10	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_GDRL	A12	L23	A10	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_GDSP	B12	P23	D11	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_PWRCOM	G11	E23	E7	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_PWRCTRL0	G12	E24	E10	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_PWRCTRL1	G13	K23	E9	NVCC_EPDC	HVIO	ALT1	IN	Keeper

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
UART2_RTS	L2	C2		NVCC_UART	HVIO	ALT1	IN	Keeper
UART2_RXD	L1	C1	L2	NVCC_UART	HVIO	ALT1	IN	Keeper
UART2_TXD	K1	B1	L1	NVCC_UART	HVIO	ALT1	IN	Keeper
UART3_RXD	L4	E4	K3	NVCC_UART	HVIO	ALT1	IN	Keeper
UART3_TXD	K4	D4	J2	NVCC_UART	HVIO	ALT1	IN	Keeper
UART4_RXD	L5	D5	J3	NVCC_UART	HVIO	ALT1	IN	Keeper
UART4_TXD	K5	D6	H2	NVCC_UART	HVIO	ALT1	IN	Keeper
USB_H1_DN	AC10	AC10	W10	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	—	—
USB_H1_DP	AD10	AD10	Y10	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	—	—
USB_H1_GPANAIO	Y11	AA17	U10	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG25	—	—	—
USB_H1_RREFEXT	AA10	AA10	U9	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG25	—	—	—
USB_H1_VBUS	Y10	AA16	V9	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	—	—
USB_OTG_DN	AC8	AC8	W8	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG50	—	—	—
USB_OTG_DP	AD8	AD8	Y8	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG50	—	—	—
USB_OTG_GPANAIO	Y7	AA14	V7	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	—	—
USB_OTG_ID	Y8	AA12	Y7	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	—	—
USB_OTG_RREFEXT	AA8	AA8	W7	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	—	—
USB_OTG_VBUS	Y9	AA13	V8	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG50	—	—	—
VREF	M23	M23	K17	VDDO25	ANALOG	—	—	—
WDOG	G5	D9	F4	NVCC_MISC	HVIO	ALT1	IN	—
XTAL	AD5	AD5	Y6	VDD2P5	ANALOG	—	—	—