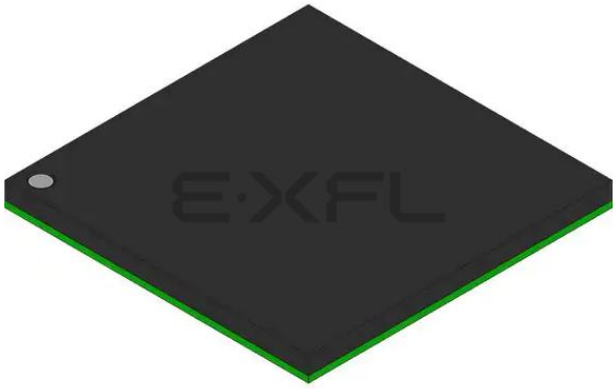

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	-20°C ~ 70°C (TA)
Security Features	Boot Security, Cryptography, Secure JTAG
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx502evm8b

- Pixel Processing Pipeline (ePXP)

  The ePXP is a high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma mapping, and rotation. The ePXP is enhanced with features specifically for grayscale applications working in conjunction with the electrophoretic display controller to form a full grayscale display solution. In addition, the ePXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated LCD controller (eLCDIF).
- Graphics acceleration

  The i.MX50 provides a 2D graphics accelerator with performance up to 200 Mpix/s.

1.1.5 Multilevel Memory System

The multilevel memory system of the i.MX50 is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The i.MX50 supports many types of external memory devices, including DDR2, LPDDR2, LPDDR1, NOR Flash, PSRAM, Cellular RAM, NAND Flash (MLC and SLC) and OneNAND™, and managed NAND including eMMC up to rev. 4.4.

1.1.6 Smart Speed™ Technology

The i.MX50 device has power management throughout the SOC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart Speed technology enables the designer to deliver a feature-rich product that requires levels of power that are far less than industry expectations.

1.1.7 Interface Flexibility

The i.MX50 supports connection to a variety of interfaces, including an LCD controller for displays, two high-speed USB on-the-go-capable PHYs, multiple expansion card ports (high-speed MMC/SDIO host and others), 10/100 Ethernet controller, and a variety of other popular interfaces (for example, UART, I^2C, and I^2S serial audio).

1.1.8 Advanced Security

The i.MX50 delivers hardware-enabled security features, such as High-Assurance Boot 4 (HAB4) for signed/authenticated firmware images, basic DRM support with random private keys and AES encryption/decryption, and storage and programmability of on-chip fuses.

1.2 Features

The i.MX50 applications processor is based on the ARM Cortex-A8 platform and has the following features:

- MMU, L1 instruction cache, and L1 data cache
- Unified L2 cache
- 800 MHz or 1 GHz target frequency of the core (including NEON, VFPv3, and L1 cache)

1.4 Part Number Feature Comparison

Table 2 provides an overview of the feature differences between the i.MX50 part numbers.

Table 2. Part Number Feature Comparison

Part Number	Disabled Features	Comments
MCIMX508	None	
MCIMX507	GPU	
MCIMX503	EPDC	The i.MX503 has the same ball map and IOMUX as the i.MX508. The EPDC pins still exist on the i.MX503, but because the EPDC block is disabled, those pins cannot be used for EPDC functionality (ALT0) and must be configured in the IOMUX with another ALT-mode setting.
MCIMX502	GPU, EPDC	The i.MX502 has the same ball map and IOMUX as the i.MX508. The EPDC pins still exist on the i.MX502, but because the EPDC block is disabled, those pins cannot be used for EPDC functionality (ALT0) and must be configured in the IOMUX with another ALT-mode setting.

Table 4. i.MX50 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SSI-1 SSI-2	I2S/SSI/AC97 Interface	Slave Connectivity Peripherals	The SSI is a full-duplex synchronous interface used on the i.MX50 processor to provide connectivity with off-chip audio peripherals. The SSI interfaces connect internally to the AUDMUX for mapping to external ports. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock/frame sync options. Each SSI has two pairs of 8 x 24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream, which reduces CPU overhead in use cases where two time slots are being used simultaneously.
Temperature Monitor	Temp Sensor	Analog	The temperature sensor is an internal module to the i.MX50 that monitors the die temperature.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface, ver. 2	Slave Connectivity Peripherals	Each of the UARTv2 modules supports the following serial data transmit/receive protocols and configurations: • 7 or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none) • Programmable bit-rates up to 4 Mbps. This is a higher max baud rate relative to the 1.875 Mbps, which is specified by the TIA/EIA-232-F standard. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps)
USB-OH-1	USB 2.0 High-Speed OTG-capable and Host ports	Master Connectivity Peripherals	USB-OH-1 supports USB2.0 HS/FS/LS, and contains: • One high-speed OTG-capable module with integrated HS USB PHY • One high-speed Host module with integrated HS USB PHY
WDOG-1	Watch Dog	Timer Peripherals	The Watchdog (WDOG) timer module protects against system failures by providing a method of escaping from unexpected events or programming errors. The WDOG Timer supports two comparison points during each counting period. Each of the comparison points is configurable to invoke an interrupt to the ARM core, and a second point invokes an external event on the WDOG line.
XTALOSC	Crystal Oscillator I/F	Clocking	The XTALOSC module combined with an external 24 MHz crystal with load capacitors implements a crystal oscillator.

Table 7. Absolute Maximum Ratings (continued)

Parameter Description	Symbol	Min	Max	Unit
ESD damage immunity: Human Body Model (HBM) Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	V
Storage temperature range	$T_{STORAGE}$	–40	125	°C

1 The term OVDD in this section refers to the associated supply rail of an input or output. The maximum range can be superseded by the DC tables.

4.1.2 Thermal Resistance Data

4.1.2.1 13 x 13 mm MAPBGA Package Thermal Resistance Data

Table 8 provides thermal resistance data for a 13 x 13 mm MAPBGA package.

Table 8. 13 x 13 mm MAPBGA Package Thermal Resistance Data

Rating	Board	Symbol	Value	Unit
Junction to Ambient (natural convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	51	°C/W
Junction to Ambient (natural convection)[1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	28	°C/W
Junction to Ambient (at 200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	40	°C/W
Junction to Ambient (at 200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	24	°C/W
Junction to Board[4]	—	$R_{\theta JB}$	14	°C/W
Junction to Case[5]	—	$R_{\theta JC}$	9	°C/W
Junction to Package Top (natural convection)[6]	—	Ψ_{JT}	2	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per JEDEC JESD51-2 with the single layer board horizontal. The thermal test board meets JESD51-9 specification.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by using the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by using the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1.3 Operating Ranges

Table 11 provides the operating ranges of the i.MX50 processor.

Table 11. i.MX50 Operating Ranges

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
VDDGP	ARM core supply voltage f_{ARM} = 1 GHz	1.20	1.275	1.35	V
	ARM core supply voltage 400 < f_{ARM} ≤ 800 MHz	0.95	1.05	1.15	V
	ARM core supply voltage 167 < f_{ARM} ≤ 400 MHz	0.85	0.95	1.15	V
	ARM core supply voltage 24 ≤ f_{ARM} ≤ 167 MHz	0.8	0.9	1.15	V
	ARM core supply voltage Stop mode	0.75	0.85	1.15	V
VCC	Peripheral supply voltage Low Performance mode (LPM). The DDR clock rate is 24 MHz.	1[3]	1.05	1.275	V
	Peripheral supply voltage Reduced Performance mode (RPM). The DDR clock rate is 133 MHz.	1[3]	1.05	1.275	V
	Peripheral supply voltage High Performance mode (HPM). The clock frequencies are derived from AHB bus using 133 MHz and AXI bus using 266 MHz (as needed). The DDR clock rate is 266 MHz.	1.175	1.225	1.275	V
	Peripheral supply voltage Stop mode	0.9[3]	0.95	1.275	V
VDDA/VDDAL1	Memory arrays voltage—Run mode 24 ≤ f_{ARM} ≤ 800 MHz	1.15	1.20	1.275	V
	Memory arrays voltage—Run mode f_{ARM} = 1 GHz	1.25	1.30	1.35	V
	Memory arrays voltage—Stop mode	0.9	0.95	1.275	V
VDD3P0	Bandgap and 480 MHz PLL supply	2.7	3.0	3.3	V
VDD2P5	Efuse, 24 MHz oscillator, 32 kHz oscillator mux supply	2.375	2.5	2.625	V
VDD1P2	PLL digital supplies	1.15	1.2	1.32	V
VDD1P8	PLL analog supplies	1.75	1.8	1.95	V

2. OSCNT. This register is in the CCM block and may be set to a maximum of 256 x 32 kHz cycles, or 8 msec. This counter is intended to give the 24MHz clock time to start up and stabilize.

If the PMIC_RDY input is used and BYPASS_PMIC_VFUNCTIONAL_READY = 0, the i.MX50 will wait for STBY_COUNT cycles after PMIC_STBY_REQ negation before checking PMIC_RDY status. Once the STBY_COUNT has expired AND the PMIC_RDY signal has been asserted, the OSCNT counter begins and the 24MHz oscillator is powered up. After OSCNT expires the processor will enter RUN mode.

If the PMIC_RDY input is not used, the processor will attempt to start the 24 MHz oscillator after STBY_COUNT expires. So at a minimum, all the supplies necessary to start up the 24 MHz oscillator need to be powered before STBY_COUNT expires: NVCC_SRTC,VDD1P2, VDD1P8, VDD2P5, VDD3P0. After STBY_COUNT expires, the OSCNT counter begins and the 24 MHz oscillator is powered up. After OSCNT expires the processor will enter RUN mode, so all other supplies need to be at the appropriate operating levels before OSCNT expires.

4.3 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O and High-Speed General Purpose I/O (GPIO)
- Double Data Rate 2 (DDR2)
- Low Power Double Data Rate 2 (LPDDR2)
- Low Power Double Data Rate 1(LPDDR1)
- Low Voltage I/O (LVIO)
- High Voltage I/O (HVIO)
- Secure Digital Host Controllers (eSDHCv2 and eSDHCv3)
- USB-OTG and USB Host ports

NOTE

The term **OVDD** in this section refers to the associated supply rail of an input or output.

4.3.1 GPIO I/O DC Parameters

The parameters in Table 18 are guaranteed per the operating ranges in Table 11, unless otherwise noted.

Table 18. GPIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	MIN	Typ	MAX	Units
High-level output voltage	Voh	Ioh=-1mA Ioh=spec'ed Drive	OVDD-0.15 0.8*OVDD	—	—	V
Low-level output voltage	Vol	Iol=1mA Iol=specified Drive	—	—	0.15 0.2*OVDD	V

Table 18. GPIO DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	MIN	Typ	MAX	Units
High-level output current (1.1-1.3V ovdd)	I Ioh	Voh=0.8*OVDD Low Drive Medium Drive High Drive Max Drive	 -0.85 -1.7 -2.5 -3.4	—	—	 mA
Low-level output current (1.1-1.3V ovdd)	I Iol	Vol=0.2*OVDD Low Drive Medium Drive High Drive Max Drive	 0.9 1.9 2.9 3.8	—	—	 mA
High-level output current (1.65-3.1V ovdd)	I Ioh	Voh=0.8*OVDD Low Drive Medium Drive High Drive Max Drive	 -2.1 -4.2 -6.3 -8.4	—	—	 mA
Low-level output current (1.65-3.1V ovdd)	I Iol	Vol=0.2*OVDD Low Drive Medium Drive High Drive Max Drive	 2.1 4.2 6.3 8.4	—	—	 mA
High-Level DC input voltage [1]	VIH	—	0.7*OVDD	—	OVDD	V
Low-Level DC input voltage	VIL	—	0V	—	0.3*OVDD	V
Input Hysteresis	VHYS	OVDD=1.875 OVDD=2.775	0.25	0.34 0.45	—	V
Schmitt trigger VT+ [2]	VT+	—	0.5*OVDD	—	—	V
Schmitt trigger VT-	VT-	—	—	—	0.5*OVDD	V
Pull-up resistor (22 KΩ PU)	Rpu	Vi=OVDD/2	20	24	28	KΩ
Pull-up resistor (47 KΩ PU)	Rpu	Vi=OVDD/2	43	51	59	KΩ
Pull-up resistor (100 KΩ PU)	Rpu	Vi=OVDD/2	91	108	125	KΩ
Pull-down resistor (100 KΩ PD)	Rpd	Vi=OVDD/2	91	108	126	KΩ
Input current (no pull-up/down)	IIN	VI = 0 VI=OVDD	—	1.7	250 120	nA
Input current (22 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	161 0.12	μA
Input current (47 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	76 0.12	μA
Input current (100 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	36 0.12	μA

4.5.8 LPDDR1 I/O AC Parameters

Table 34 shows the AC parameters for LPDDR1 I/O.

Table 34. LPDDR1 I/O AC Parameters

Parameter	Symbol	Min	Max	Unit
AC input logic high	Vihd(ac)	0.8*ovdd	ovdd+0.3	V
AC input logic low	Vild(ac)	-0.3	0.2*ovdd	
AC input differential voltage[1]	Vid(ac)	0.6*ovdd	ovdd+0.6	
AC input differential crosspoint voltage[2]	Vix(ac)	0.4*ovdd	0.6*ovdd	
Output propagation delay high to low	tPOHLD		2.5	ns
Output propagation delay low to high	tPOLHD		2.5	
Input propagation delay high to low	tPIHLD		1.5	
Input propagation delay low to high	tPILHD		1.5	
Single output slew rate	tsr	0.3	2.5	V/ns

[1]Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac)-Vil(ac)

[2]The typical value of Vix(ac) is expected to be about 0.5*ovdd. and Vix(ac) is expected to track variation of ovdd. Vix(ac) indicates the voltage at which differential input signal must cross.

4.5.9 LPDDR2 I/O AC Parameters

Table 35 shows the AC parameters for LPDDR2 I/O.

Table 35. LPDDR2 I/O AC Parameters

Parameter	Symbol	Min	Max	Unit
AC input logic high	Vih(ac)	Vref+0.22	ovdd	V
AC input logic low	Vil(ac)	ovss	Vref-0.22	
AC differential input high voltage[1]	Vidh(ac)	0.44	-	
AC differential input low voltage	Vidhl(ac)	-	0.44	
AC input differential cross point voltage (relative to ovdd / 2)[2]	Vix(ac)	-0.12	0.12	
Over/undershoot peak	Vpeak		0.35	ns
Over/undershoot area (above OVDD or below OVSS)	Varea		0.6 (at 266 MHz)	V-ns
Output propagation delay high to low	tPOHLD		3.5	ns
Output propagation delay low to high	tPOLHD		3.5	
Input propagation delay high to low	tPIHLD		1.5	
Input propagation delay low to high	tPILHD		1.5	

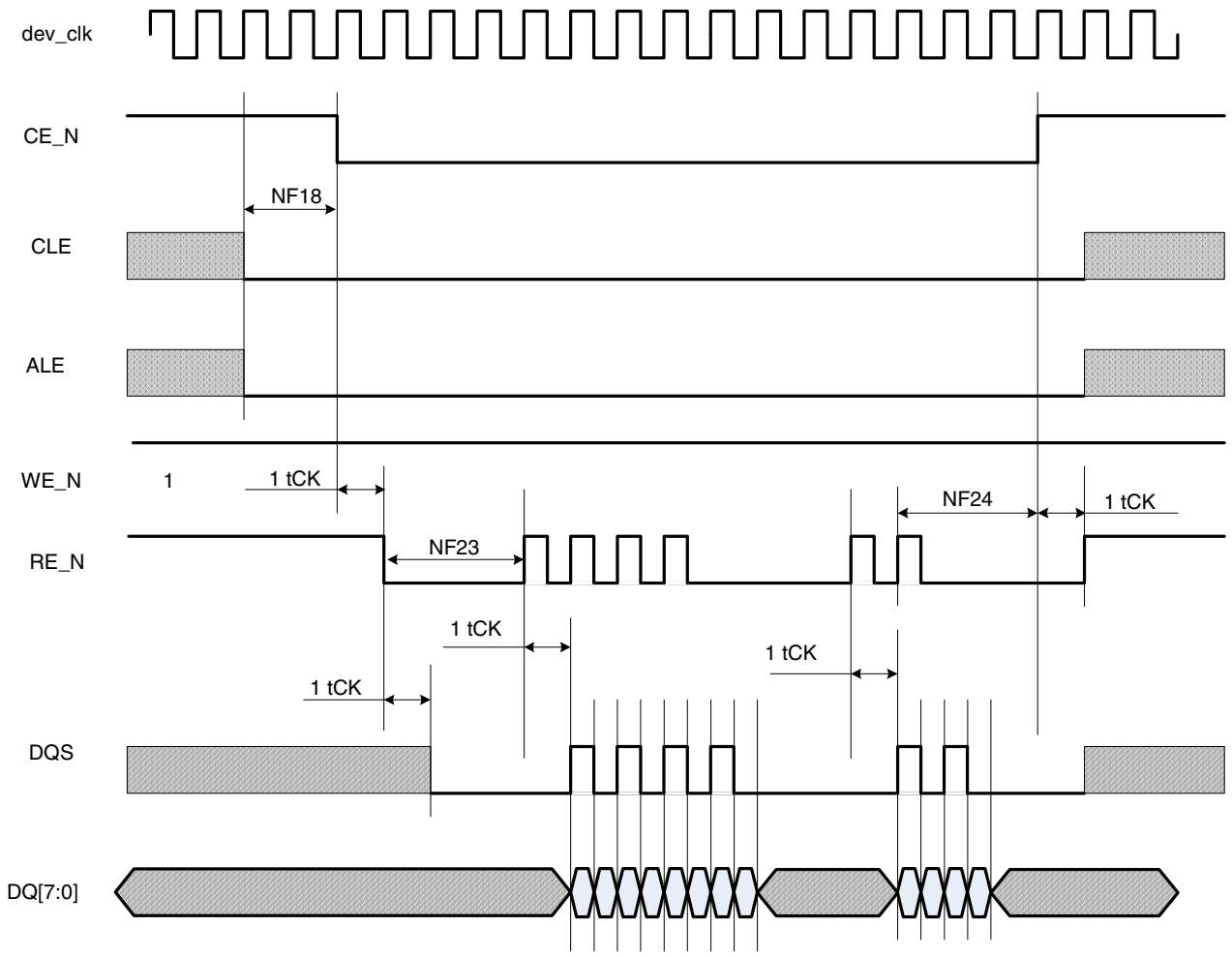

Figure 16. Samsung Toggle Mode Data Read Timing

Table 42. Samsung Toggle Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	CE# access time	t_{CE}	CE_DELAY*t_{CK}	—	ns
NF19	CE# hold time	t_{CH}	0.5 *t_{CK}	—	ns
NF20	Command/address DQ setup time	t_{CAS}	0.5*t_{CK}	—	ns
NF21	Command/address DQ hold time	t_{CAH}	0.5*t_{CK}	—	ns
NF22	clock period	t_{CK}	7.5	—	ns

Table 44. EIM Asynchronous Timing Parameters Table Relative Chip Select (continued)

ID	Parameter	Determination by Synchronous Measured Parameters [1]	Min	Max	Unit
WE34	EIM_RW invalid to EIM_CSx invalid	WE7 – WE9 + (WEN – CSN)	—	3 – (WEN_CSN)	ns
WE35	EIM_CSx valid to EIM_OE valid	WE10 – WE6 + (OEA – CSA)	—	3 + (OEA – CSA)	ns
WE36	EIM_OE invalid to EIM_CSx invalid	WE7 – WE11 + (OEN – CSN)	—	3 – (OEN – CSN)	ns
WE37	EIM_CSx valid to EIM_EBx valid (Read access)	WE12 – WE6 + (RBEA – CSA)	—	3 + (RBEA[4] – CSA)	ns
WE38	EIM_EBx invalid to EIM_CSx invalid (Read access)	WE7 – WE13 + (RBEN – CSN)	—	3 – (RBEN[5] – CSN)	ns
WE39	EIM_CSx valid to EIM_LBA valid	WE14 – WE6 + (ADV – CSA)	—	3 + (ADVA – CSA)	ns
WE40	EIM_LBA invalid to EIM_CSx invalid (ADVL is asserted)	WE7 – WE15 – CSN	—	3 – CSN	ns
WE41	EIM_CSx valid to Output Data valid	WE16 – WE6 – WCSA	—	3 – WCSA	ns
WE42	Output Data invalid to EIM_CSx invalid	WE17 – WE7 – CSN	—	3 – CSN	ns
WE43	Input Data valid to EIM_CSx invalid	MAXCO + MAXDI	MAXCO[6] + MAXDI[7]	—	ns
WE44	EIM_CSx invalid to Input Data invalid	0	0	—	ns
WE45	EIM_CSx valid to EIM_EBx valid (Write access)	WE12 – WE6 + (WBEA – CSA)	—	3 + (WBEA – CSA)	ns
WE46	EIM_EBx invalid to EIM_CSx invalid (Write access)	WE7 – WE13 + (WBEN – CSN)	—	–3 + (WBEN – CSN)	ns
WE47	EIM_DTACK valid to EIM_CSx invalid	MAXCO + MAXDTI	MAXCO[6] + MAXDTI[8]	—	ns
WE48	EIM_CSx invalid to EIM_DTACK invalid	0	0	—	ns

1 Parameters WE4–WE21 value, see in the Table 44.

2 EIM_CSx Assertion. This bit field determines when EIM_CSx signal is asserted during read/write cycles.

3 EIM_CSx Negation. This bit field determines when EIM_CSx signal is negated during read/write cycles.

4 EIM_EBx Assertion. This bit field determines when EIM_EBx signal is asserted during read cycles.

5 EIM_EBx Negation. This bit field determines when EIM_EBx signal is negated during read cycles.

6 Output maximum delay from internal driving the FFs to chip outputs. The maximum delay between all memory controls (EIM_ADDR, EIM_CSx, EIM_OE, EIM_RW, EIM_EBx, and EIM_LBA).

7 Maximum delay from chip input data to internal FFs. The maximum delay between all data input pins.

8 DTACK maximum delay from chip input data to internal FF.

4.8 DRAM Timing Parameters

This section includes descriptions of the electrical specifications of DRAM MC module which interfaces external DDR2, LPDDR1, and LPDDR2 memory devices.

4.9.2.2 CSPI Slave Mode Timing

Figure 33 depicts the timing of CSPI in slave mode. Table 51 lists the CSPI slave mode timing characteristics.

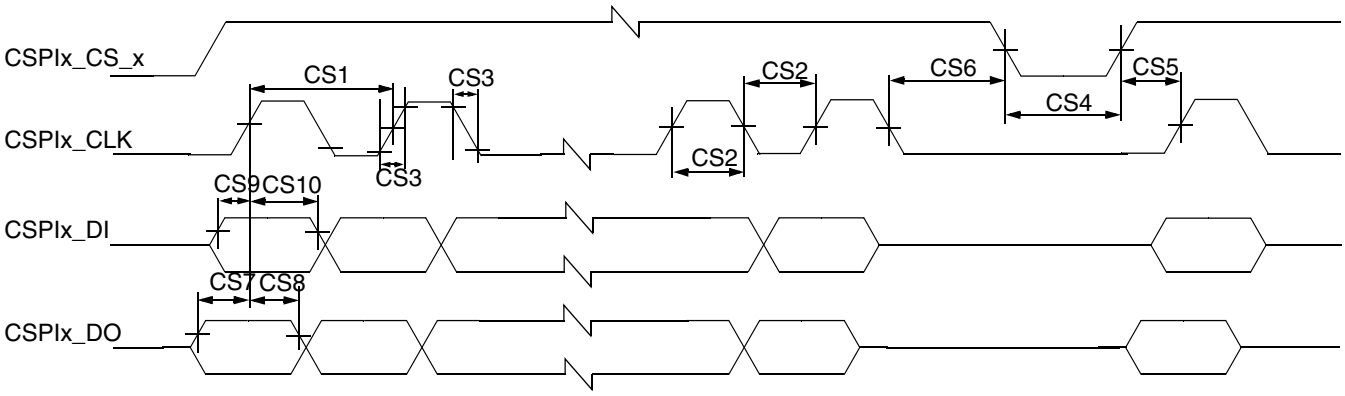

Figure 33. CSPI Slave Mode Timing Diagram

Table 51. CSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	CSPIx_CLK Cycle Time	t_{clk}	60	—	ns
CS2	CSPIx_CLK High or Low Time	t_{SW}	15	—	ns
CS3	CSPIx_CLK Rise or Fall	$t_{RISE/FALL}$	—	—	ns
CS4	CSPIx_CS_x pulse width	t_{CSLH}	30	—	ns
CS5	CSPIx_CS_x Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	CSPIx_CS_x Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	CSPIx_DO Setup Time	t_{Smosi}	5	—	ns
CS8	CSPIx_DO Hold Time	t_{Hmosi}	5	—	ns
CS9	CSPIx_DI Setup Time	t_{Smiso}	5	—	ns
CS10	CSPIx_DI Hold Time	t_{Hmiso}	5	—	ns

Table 55. eMMC4.4 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD2	eSDHC Output Delay	t_{OD}	–5	5	ns
eSDHC Input/Card Outputs CMD, DAT (Reference to CLK)					
SD3	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD4	eSDHC Input Hold Time	t_{IH}	1.5	—	ns

4.9.4 FEC AC Timing Parameters

This section describes the AC timing specifications of the FEC. The i.MX50 FEC supports 10/100 Mbps RMII with MII serial management interface. The RMII and serial management signals are compatible with transceivers operating at a voltage of 3.3 V.

4.9.4.1 RMII Async Inputs Signal Timing (FEC_COL)

Table 56 lists RMII asynchronous inputs signal timing information. Figure 38 shows MII asynchronous input timings listed in Table 56.

Table 56. RMII Async Inputs Signal Timing

Num	Characteristics	Min	Max	Unit
M9	FEC_COL minimum pulse width	1.5	—	FEC_TX_CLK period

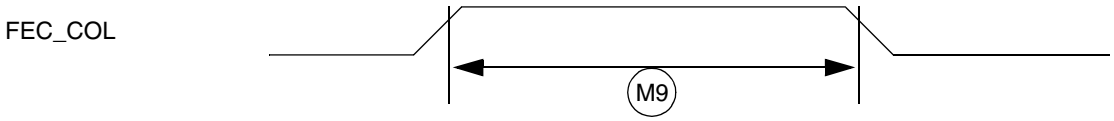

Figure 38. MII Async Inputs Timing Diagram

4.9.4.2 RMII Serial Management Channel Timing (FEC_MDIO and FEC_MDC)

Table 57 lists RMII serial management channel timings. Figure 39 shows RMII serial management channel timings listed in Table 57. The MDC frequency should be equal to or less than 2.5 MHz to be compliant with the IEEE 802.3 RMII specification. However, the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Table 57. RMII Transmit Signal Timing

ID	Characteristics	Min	Max	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns

Table 67. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS as shown in both the tables and figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- **Tx** and **Rx** refer to the transmit and receive sections of the SSI.
- The terms WL and BL refer to word length (WL) and bit length (BL).
- For internal frame sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

Table 68. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in both the tables and figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- Tx and Rx refer to the transmit and receive sections of the SSI.
- The terms WL and BL refer to word length (WL) and bit length (BL).
- For internal frame sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

5.1.2 416 MAPBGA 13 x 13 mm, 0.5 mm Pitch Ball Map

Table 79 shows the 416 MAPBGA 13 x 13 mm, 0.5 mm pitch ball map.

Table 79. 416 MAPBGA 13x13 mm, 0.5 mm Pitch Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
A	VSS	EIM_RDY	EIM_CRE	EIM_EB0	EIM_BCLK	EIM_DA12	EIM_DA8	EIM_DA4	EIM_DA0	EPDC_SDSHR	EPDC_GDCLK	EPDC_GDRL	EPDC_SDCLK	EPDC_D12	EPDC_D8	EPDC_D4	EPDC_D0	VSS	DRAM_D30	DRAM_D29	NVCC_EMI_DRAM	DRAM_D26	DRAM_D25	VSS	A
B	KEY_COL0	KEY_COL1	EIM_OE	EIM_EB1	EIM_RW	EIM_DA13	EIM_DA9	EIM_DA5	EIM_DA1	EIM_CS0	EPDC_GDOE	EPDC_GDSP	EPDC_SDCLKN	EPDC_D13	EPDC_D9	EPDC_D5	EPDC_D1	VSS	DRAM_D31	DRAM_D28	NVCC_EMI_DRAM	DRAM_D27	DRAM_D24	DRAM_DQM3	B
C	KEY_COL2	KEY_COL3	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	DRAM_SDQS3	DRAM_SDQS3_B	C
D	KEY_ROW0	KEY_ROW1	NC	KEY_ROW2	EIM_WAIT	EIM_DA14	EIM_DA10	EIM_DA6	EIM_DA2	EIM_CS1	EPDC_SDCE4	EPDC_SDCE2	EPDC_SDCE0	EPDC_D14	EPDC_D10	EPDC_D6	EPDC_D2	EPDC_SDLE	EPDC_SDOED	EPDC_VCOM1	NVCC_EMI_DRAM	NC	NVCC_EMI_DRAM	NVCC_EMI_DRAM	D
E	I2C1_SCL	I2C1_SDA	NC	KEY_ROW3	EIM_LBA	EIM_DA15	EIM_DA11	EIM_DA7	EIM_DA3	EIM_CS2	EPDC_SDCE5	EPDC_SDCE3	EPDC_SDCE1	EPDC_D15	EPDC_D11	EPDC_D7	EPDC_D3	EPDC_SDOE	EPDC_SDOEZ	EPDC_BDR0	EPDC_BDR1	NC	DRAM_D15	DRAM_D14	E
F	I2C2_SCL	I2C2_SDA	NC	PWM2	PWM1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	DRAM_A14	DRAM_A13	NC	DRAM_D12	DRAM_D13	F
G	I2C3_SCL	I2C3_SDA	NC	EPITO	WDOG	NC	OWIRE	VDDGP	VDDGP	VDDGP	EPDC_PWRCOM	EPDC_PWRCTRL0	EPDC_PWRCTRL1	EPDC_PWRCTRL2	EPDC_PWRCTRL3	EPDC_PWRSTAT	EPDC_VCOM0	DRAM_SDODT0	NC	VSS	VSS	NC	VSS	DRAM_D10	G

Table 80. 416 MAPBGA 13x13 Ground, Power, Sense, and Reference Contact Signals (continued)

NVCC_SRTC	AA1	—
NVCC_SSI	R8	—
NVCC_UART	T8	—
USB_H1_VDDA25	AD9	Note that on the 416 MAPBGA package, USB_OTG_VDDA25 and USB_H1_VDDA25 are shorted together on the substrate.
USB_H1_VDDA33	AC11	Note that on the 416 MAPBGA package, USB_OTG_VDDA33 and USB_H1_VDDA33 are shorted together on the substrate.
USB_OTG_VDDA25	AC9	Note that on the 416 MAPBGA package, USB_OTG_VDDA25 and USB_H1_VDDA25 are shorted together on the substrate.
USB_OTG_VDDA33	AD11	Note that on the 416 MAPBGA package, USB_OTG_VDDA33 and USB_H1_VDDA33 are shorted together on the substrate.
VCC	H14, H15, H16, H17, J17, K14, K15, K17, L15	—
VDD_DCDCI	Y6	—
VDD_DCDCO	Y5	—
VDD1P2	AD6	—
VDD1P8	AD7	—
VDD2P5	AD4	—
VDD3P0	AD3	—
VDDA	P17, R17	—
VDDAL1	P15, R15	—
VDDGP	G10, G8, G9, H10, H11, H8, H9, J8, K10, K11, K7, K8, L10, L11, L8	—
VDDO25	N23	—
VSS	A1, A18, A24, AA11, AA2, AA9, AC18, AC3, AC4, AC6, AC7, AD1, AD18, AD24, B18, G20, G21, G23, H12, H13, K12, K13, L12, L13, L14, L17, M11, M14, M15, M17, M18, M20, M21, N11, N14, N15, N17, P11, P12, P13, P14, R11, R12, R13, R14, T17, T18, U12, U13, U14, U15, U16, U17, U18, V17, V18, V20, V21, V23	—

Table 82. 416 PoPBGA 13 x 13 mm Ground, Power, Sense, and Reference Contact Signals (continued)

NVCC_RESET	V8	—
NVCC_SD1	T7	—
NVCC_SD2	U8	—
NVCC_SPI	R7	—
NVCC_SRTC	AA1	—
NVCC_SSI	R8	—
NVCC_UART	T8	—
POP_EMMC_RST	A19	This is PoP eMMC 4.4 NAND Reset input pin. This pin does not connect to the i.MX50. If using eMMC 4.4 NAND, this pin can be connected to a GPIO. For non 4.4 eMMC applications, leave floating.
POP_LPDDR2_1.8V	A20, B19, B20, M5, N5	This is the 1.8V supply for the PoP LPDDR2. These pins do not connect to the i.MX50.
POP_LPDDR2_ZQ0	AA24	This is the PoP LPDDR2 ZQ0 pin. This pin does not connect to the i.MX50. This should be connected on the PCB to a 240 Ω 1% resistor to ground
POP_LPDDR2_ZQ1	AA23	This is the PoP LPDDR2 ZQ1 pin. This pin does not connect to the i.MX50. If used, this should be connected on the PCB to a 240 Ω 1% resistor to ground
POP_NAND_VCC	D19, D20	This is the 3.3V I/O and memory supply for the PoP eMMC NAND. Note that because the eMMC memory and I/O domains are shorted together, it is not possible to support 1.8 V I/O for the PoP eMMC NAND.
USB_VDDA25	AC9, AD9	Note that on the PoPBGA package, USB_OTG_VDDA25 and USB_H1_VDDA25 are shorted together.
USB_VDDA33	AC11, AD11	Note that on the PoPBGA package, USB_OTG_VDDA33 and USB_H1_VDDA33 are shorted together.
VCC	H14, H15, H16, H17, J17, K14, K15, K17, L15	—
VDD_DCDCI	Y6	—
VDD_DCDCO	Y5	—
VDD1P2	AD6	—
VDD1P8	AD7	—

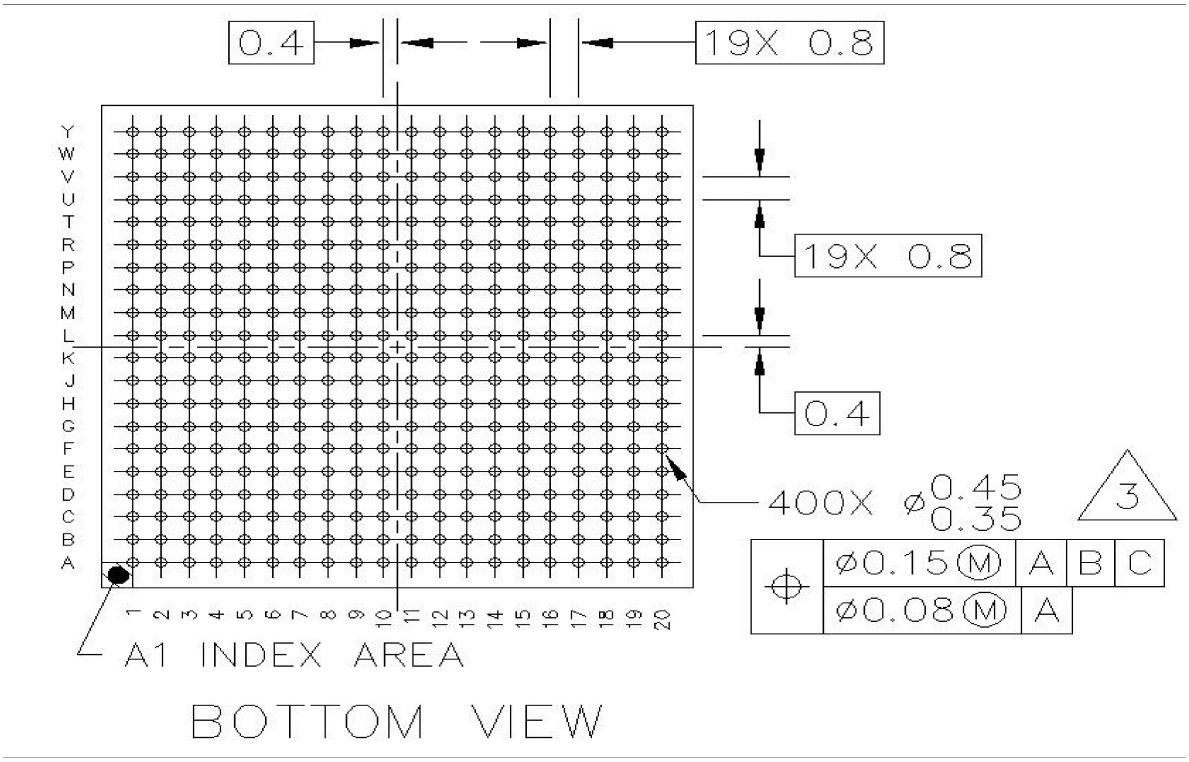

Figure 66. 400 MAPBGA 17x17 mm Package Bottom View

5.3.3 400 MAPBGA 17 x 17 Power Rails

Table 84. 400 MAPBGA 17x17 Ground, Power, Sense, and Reference Contact Signals

Pin Name	Ball Number
NC	A1 Y1 A20 Y20
NVCC_EIM	F6 F7 F8
NVCC_EMI_DRAM	K14 N14 J15 K15 L15 N15 P15 H16 J16 K16 L16 M16 N16 P16 R16
NVCC_EPDC	F9 F10 F11 F12
NVCC_JTAG	P9
NVCC_KEYPAD	H5
NVCC_LCD	P10
NVCC_MISC	J5
NVCC_NANDF	P11 P12
NVCC_RESET	P6
NVCC_SD1	N5
NVCC_SD2	P5
NVCC_SPI	M5
NVCC_SRTC	R5
NVCC_SSI	K5
NVCC_UART	L5
USB_H1_VDDA25	Y9
USB_H1_VDDA33	W11
USB_OTG_VDDA25	W9
USB_OTG_VDDA33	Y11
VCC	K10 L10 M10 K11 L11 M11 J12 K12 L12
VDD1P2	U6
VDD1P8	V6
VDD2P5	V5
VDD3P0	U5
VDDA	K9 J11
VDDAL1	J9 J10
VDDGP	G6 H6 J6 K6 L6 G7 H7 J7 K7 G8 H8 G9 H9 G10 H10
VDDO25	L17
VSS	T5 W5 M6 N6 L7 M7 N7 P7 J8 K8 L8 M8 N8 P8 L9 M9 N9 N10 R10 G11 H11 N11 R11 G12 H12 M12 N12 R12 G13 H13 J13 K13 L13 M13 N13 P13 R13 G14 H14 J14 L14 M14 P14 R14 H15 M15 R15

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
JTAG_TDI	AA4	AA4	U8	NVCC_JTAG	GPIO	ALT0	IN	47K PU
JTAG_TDO	U7	V4	T9	NVCC_JTAG	GPIO	ALT0	OUT-LO	Keeper
JTAG_TMS	Y4	Y4	R9	NVCC_JTAG	GPIO	ALT0	IN	47K PU
JTAG_TRSTB	AA5	AA5	U7	NVCC_JTAG	GPIO	ALT0	IN	47K PU
KEY_COL0	B1	A9	B1	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_COL1	B2	A10	B2	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_COL2	C1	B9	C1	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_COL3	C2	B10	C2	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW0	D1	A8	D1	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW1	D2	B8	D2	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW2	D4	D7	C3	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW3	E4	A7	D3	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
OWIRE	G7	D12	E5	NVCC_MISC	HVIO	ALT1	IN	Keeper
PMIC_ON_REQ	W1	W1	Y3	NVCC_SRTC	GPIO	ALT0	OUT-LO	—
PMIC_STBY_REQ	W2	W2	Y2	NVCC_SRTC	GPIO	ALT0	OUT-LO	—
POR_B	AD2	AD2	Y5	NVCC_RESET	LVIO	ALT0	IN	100K PU
PWM1	F5	D11	E4	NVCC_MISC	HVIO	ALT1	IN	Keeper
PWM2	F4	D10	E3	NVCC_MISC	HVIO	ALT1	IN	Keeper
RESET_IN_B	AC1	AC1	W3	NVCC_RESET	LVIO	ALT0	IN	100K PU
SD1_CLK	P1	M1	R1	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_CMD	R1	N1	P4	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D0	R2	P2	R2	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D1	P2	N2	P1	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D2	R4	M2	P3	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D3	R5	R4	P2	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD2_CD	T4	J4	T1	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_CLK	U1	E1	T3	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_CMD	V5	G1	V1	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D0	T1	D1	R3	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D1	T2	D2	U1	NVCC_SD2	HVIO	ALT1	IN	Keeper