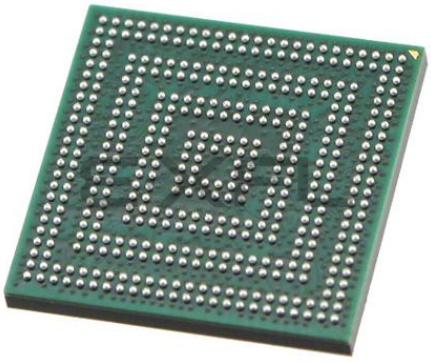

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Boot Security, Cryptography, Secure JTAG
Package / Case	416-LFBGA
Supplier Device Package	416-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx503cvk8b

application chipset, the i.MX50 provides a rich set of interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, and displays.

1.1 Product Overview

The i.MX50 is designed to enable high-tier portable applications by satisfying the performance requirements of advanced operating systems and applications.

1.1.1 Dynamic Performance Scaling

Freescale's dynamic voltage and frequency scaling (DVFS) allows the device to run at much lower voltage and frequency with ample processing capacity for tasks, such as audio decode, resulting in significant power reduction.

1.1.2 Multimedia Processing Powerhouse

The multimedia performance of the i.MX50 processor ARM Cortex-A8 core is boosted by a multi-level cache system, a NEON™ coprocessor with SIMD media processing architecture and 32-bit single-precision floating point support, and two vector floating point coprocessors. The system is further enhanced by a programmable smart DMA (SDMA) controller.

1.1.3 Powerful Display System

The i.MX50 includes support for both standard LCD displays as well as electrophoretic displays (e-paper). The display subsystem consists of the following modules:

- Electrophoretic Display Controller (EPDC) (i.MX508 only)

  The EPDC is a feature-rich, low power, and high-performance direct-drive active matrix EPD controller. It is specifically designed to drive E-INK^{TM} EPD panels, supporting a wide variety of TFT architectures. The goal of the EPDC is to provide an efficient SoC integration of this functionality for e-paper applications, allowing a significant bill of materials cost savings over an external solution while reaching much higher levels of performance and lower power. The EPDC module is defined in the context of an optimized hardware/software partitioning and works in conjunction with the ePXP (see Section 1.1.4, "Graphics Accelerators").
- Enhanced LCD Controller Interface (eLCDIF)

  The eLCDIF is a high-performance LCD controller interface that supports a rich set of modes and allows interoperability with a wide variety of LCD panels, including DOTCK/RGB and smart panels. The module also supports synchronous operation with the ePXP to allow the processed frames to be passed from the ePXP to the eLCDIF through an on-chip SRAM buffer. The eLCDIF can support up to 32-bit interfaces.

1.1.4 Graphics Accelerators

Integrated graphics accelerators offload processing from the ARM processor, enabling high performance graphic applications at minimum power.

Table 4. i.MX50 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SDMA	Smart Direct Memory Access	Master Connectivity Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by offloading various cores in dynamic data routing. The SDMA features list is as follows: • Powered by a 16-bit instruction-set micro-RISC engine • Multi-channel DMA supports up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM Cortex-A8 and SDMA • Very fast context-switching with two-level priority-based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle uni-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers for EMI • Support of byte-swapping and CRC calculations • A library of scripts and API is available
SJC	Secure JTAG Controller	System Control Peripherals	The Secure JTAG Controller provides a mechanism for regulating JTAG access, preventing unauthorized JTAG usage while allowing JTAG access for manufacturing tests and software debugging. The i.MX50 JTAG port provides debug access to several hardware blocks including the ARM processor and the system bus, therefore, it must be accessible for initial laboratory bring-up, manufacturing tests and troubleshooting, and for software debugging by authorized entities. However, if the JTAG port is left unsecured it provides a method for executing unauthorized program code, getting control over secure applications, and running code in privileged modes. The Secure JTAG controller provides three different security modes that can be selected through an e-fuse configuration to prevent unauthorized JTAG access.
SPBA	Shared Peripheral Bus Arbiter	System Control Peripherals	SPBA (Shared Peripheral Bus Arbiter) is a two-to-one IP bus interface (IP bus) arbiter.
SRTC	Secure Real Time Clock	Security Peripherals	The SRTC incorporates a special System State Retention Register (SSRR) that stores system parameters during system shutdown modes. This register and all SRTC counters are powered by dedicated supply rail NVCC_SRTC. The NVCC_SRTC can be energized separately even if all other supply rails are shut down. This register is helpful for storing warm boot parameters. The SSRR also stores the system security state. In case of a security violation, the SSRR marks the event (security violation indication).

Table 5. Special Signal Considerations (continued)

Signal Name	Remarks
DRAM_OPEN, DRAM_OPENFB (for 416 MAPBGA and 400 MAPBGA)	These pins are the echo gating output and feedback pins used by the DRAM PHY to bound a window around the DQS transition. For an application using a single DRAM device, these pins should be routed so that the trace length (DRAM_OPEN + DRAM_OPENFB) = trace length (DRAM_SDCLK0 + DRAM_SDQS0). For an application using two DRAM devices, they should be routed so that the trace length (DRAM_OPEN + DRAM_OPENFB) = trace length (AVG(DRAM_SDCLK0+DRAM_SDCLK1) + AVG (DRAM_SDQS0_to_Device0 + DRAM_SDQS0_to_Device1)). This connection is required for LPDDR1, LPDDR2, and DDR2. For the i.MX50 PoP package, these signals are connected on the substrate.
DRAM_SDODT0 (for 416 MAPBGA and 400 MAPBGA), DRAM_SDODT1 (for 416 MAPBGA only)	These pins are the On-die termination outputs from the i.MX50. For DDR2, these pins should be connected to the DDR2 DRAM ODT pins. For LPDDR1 and LPDDR2, these pins should be left floating. Note that both SDODT pins are removed on the 416 PoPBGA package, and only SDODT0 exists on the 400 MAPBGA package.
DRAM_CALIBRATION	This pin is the ZQ calibration used to calibrate DRAM Ron and ODT. For LPDDR2, this pin should be connected to ground through a 240 Ω 1% resistor. For DDR2 and LPDDR1, this pin should be connected to ground through a 300 Ω 1% resistor.
JTAG_MOD	This input has an internal 100K pull-up, by default. Note that JTAG_MOD is referenced as SJC_MOD in the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM) - both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. If JTAG port is not needed, the internal pull-up can be disabled in order to reduce supply current to the pin.
JTAG_TCK	This input has an internal 100K pull-down. This pin is in the NVCC_JTAG domain.
JTAG_TDI	This input has an internal 47K pull-up to NVCC_JTAG. This pin is in the NVCC_JTAG domain.
JTAG_TDO	This is a 3-state output with an internal gate keeper enable to prevent a floating condition. An external pull-up or pull-down resistor on JTAG_TDO is detrimental and should be avoided. This pin is in the NVCC_JTAG domain.
JTAG_TMS	This input has an internal 47K pull-up to NVCC_JTAG. This pin is in the NVCC_JTAG domain.
JTAG_TRSTB	This input has an internal 47K pull-up to NVCC_JTAG. This pin is in the NVCC_JTAG domain.
NC	These signals are No Connect (NC) and should be floated by the user.
LOW_BATT_GPIO	If the LOW_BATT_GPIO (UART4_TXD) is asserted at power up, the i.MX50 will boot up at a lower ARM clock frequency to reduce system power. The actual ARM clock frequency used when LOW_BATT_GPIO is asserted is determined by the BT_LPB_FREQ[1:0] pins (220 MHz to 55.3 MHz). The polarity of the LOW_BATT_GPIO is active high by default, but may be set to active low by setting the LOW_BATT_GPIO_LEVEL OTP bit. See the “System Boot” chapter of the Reference Manual for more details. Note that this is not a dedicated pin: LOW_BATT_GPIO appears on the UART4_TXD pin.
PMIC_STBY_REQ	This output may be driven high when the i.MX50 enters the STOP mode to notify the PMIC to enter its low power standby state. This output is in the NVCC_SRTC domain.
PMIC_ON_REQ	This output from the i.MX50 can instruct the PMIC to turn on when the i.MX50 only has NVCC_SRTC power. This may be useful for an alarm application, as it allows the i.MX50 to turn off all blocks except for the RTC and then power on again at a specified time. This output is in the NVCC_SRTC domain.

4.5 I/O AC Parameters

The load circuit and output transition time waveforms are shown in Figure 4 and Figure 5. The AC electrical characteristics for slow and fast I/O are presented in the Table 27 and Table 28, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bit in the IOMUX control registers.

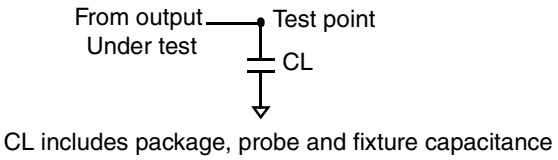

Figure 4. Load Circuit for Output

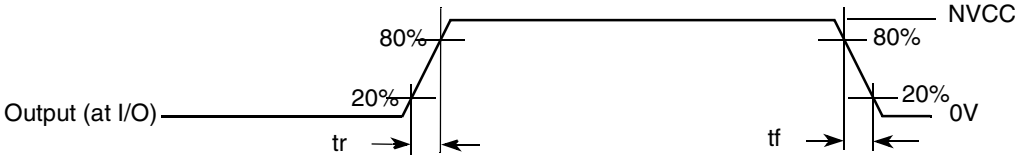

Figure 5. Output Transition Time Waveform

4.5.1 GPIO I/O Slow AC Parameters

Table 27 shows the AC parameters for GPIO slow I/O.

Table 27. GPIO I/O Slow AC Parameters

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF			1.91/1.52 3.07/2.65	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF			2.22/1.81 3.81/3.42	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF			2.88/2.42 5.43/5.02	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF			4.94/4.50 10.55/9.70	ns
Output Pad Slew Rate (Max Drive)[1]	tps	15 pF 35 pF	0.5/0.65 0.32/0.37			V/ns
Output Pad Slew Rate (High Drive)	tps	15 pF 35 pF	0.43/0.54 0.26/0.41			V/ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0.34/0.41 0.18/0.2			V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0.20/0.22 0.09/0.1			V/ns
Output Pad di/dt (Max Drive)	tdit				30	mA/ns

4.5.7 DDR2 I/O AC Parameters

Table 33 shows the AC parameters for DDR2 I/O.

Table 33. DDR2 I/O AC Parameters

Parameter	Symbol	Min	Max	Unit
AC input logic high	Vih(ac)	Vref+0.25	-	V
AC input logic low	Vil(ac)	-	Vref-0.25	
AC differential input voltage[1]	Vid(ac)	0.5	ovdd	
AC Input differential cross point voltage[2]	Vix(ac)	0.5*ovdd -0.175	0.5*ovdd + 0.175	
AC output differential cross point voltage [3]	Vox(ac)	0.5*ovdd -0.125	0.5*ovdd+ 0.125	
Output propagation delay high to low	t_{POHLD}		3.5	ns
Output propagation delay low to high	t_{POLHD}		3.5	
Input propagation delay high to low	t_{PIHLD}		1.5	
Input propagation delay low to high	t_{PILHD}		1.5	
Single output slew rate	tsr	0.4	2	V/ns

[1]Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac)-Vil(ac)

[2]The typical value of Vix(ac) is expected to be about 0.5*OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

[3]The typical value of Vox(ac) is expected to be about 0.5*OVDD and Vox(ac) is expected to track variation in OVDD. Vox(ac) indicates the voltage at which differential output signal must cross.

Table 41. Source Synchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF24	postamble delay	t_{POST}	POST_DELAY*t_{CK}	—	ns
NF25	CLE and ALE setup time	t_{CALS}	0.5*t_{CK}	—	ns
NF26	CLE and ALE hold time	t_{CALH}	0.5*t_{CK}	—	ns
NF27	Data input to first DQS latching transition	t_{DQSS}	t_{CK}	—	ns

1 GPMI's sync mode output timing could be controlled by module's internal register, say HW_GPMI_TIMING2_CE_DELAY, HW_GPMI_TIMING_PREAMBLE_DELAY, and HW_GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers' setting. In the above table, we use CE_DELAY/PRE_DELAY/POST_DELAY representing these settings each.

4.6.5.3 Samsung Toggle Mode AC Timing

4.6.5.3.1 Command and Address Timing

NOTE

Samsung Toggle Mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. Please refer to the above chapter for details.

Table 43. EIM Bus Timing Parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	EIM_BCLK Cycle time[2]	t	—	2t	—	3t	—	4t	—
WE2	EIM_BCLK Low Level Width	0.4t	—	0.8t	—	1.2t	—	1.6t	—
WE3	EIM_BCLK High Level Width	0.4t	—	0.8t	—	1.2t	—	1.6t	—
WE4	Clock rise to address valid[3]	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE5	Clock rise to address invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE6	Clock rise to EIM_CSx valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE7	Clock rise to EIM_CSx invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE8	Clock rise to EIM_RW valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE9	Clock rise to EIM_RW invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE10	Clock rise to EIM_OE valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE11	Clock rise to EIM_OE invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE12	Clock rise to EIM_EBx valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE13	Clock rise to EIM_EBx invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE14	Clock rise to EIM_LBA valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE15	Clock rise to EIM_LBA invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE16	Clock rise to Output Data valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	2t – 1.25	2t + 1.75
WE17	Clock rise to Output Data Invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	2t – 1.25	2t + 1.75
WE18	Input Data setup time to Clock rise	2	—	2	—	2	—	2	—
WE19	Input Data hold time from Clock rise	2.5	—	2.5	—	2.5	—	2.5	—
WE20	EIM_WAIT setup time to Clock rise	2	—	2	—	2	—	2	—
WE21	EIM_WAIT hold time from Clock rise	2.5	—	2.5	—	2.5	—	2.5	—

1 *t* is axi_clk cycle time. The maximum allowed axi_clk frequency is 133 MHz, whereas the maximum allowed EIM_BCLK frequency is 66.5 MHz. As a result, if BCD = 0, axi_clk must be ≤ 66.5 MHz. If BCD = 1, then 133 MHz is allowed for axi_clk, resulting in a EIM_BCLK of 66.5 MHz. When the clock branch to EIM is decreased to 66.5 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM) for a detailed clock tree description.

[2] EIM_BCLK parameters are being measured from the 50% point that is, high is defined as 50% of signal value and low is defined as 50% as signal value.

[3] For signal measurements *High* is defined as 80% of signal value and *Low* is defined as 20% of signal value.

4.7.2 Examples of EIM Accesses

Figure 19, Figure 20, Figure 21, Figure 22, Figure 23, and Figure 24 give a few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

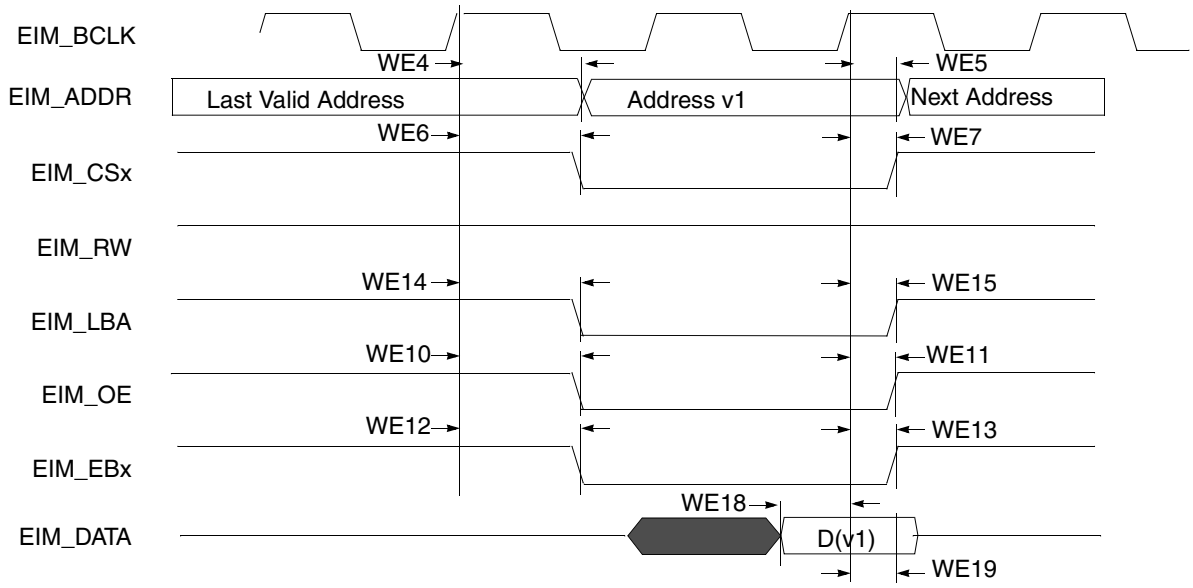

Figure 19. Synchronous Memory Read Access, WSC=1

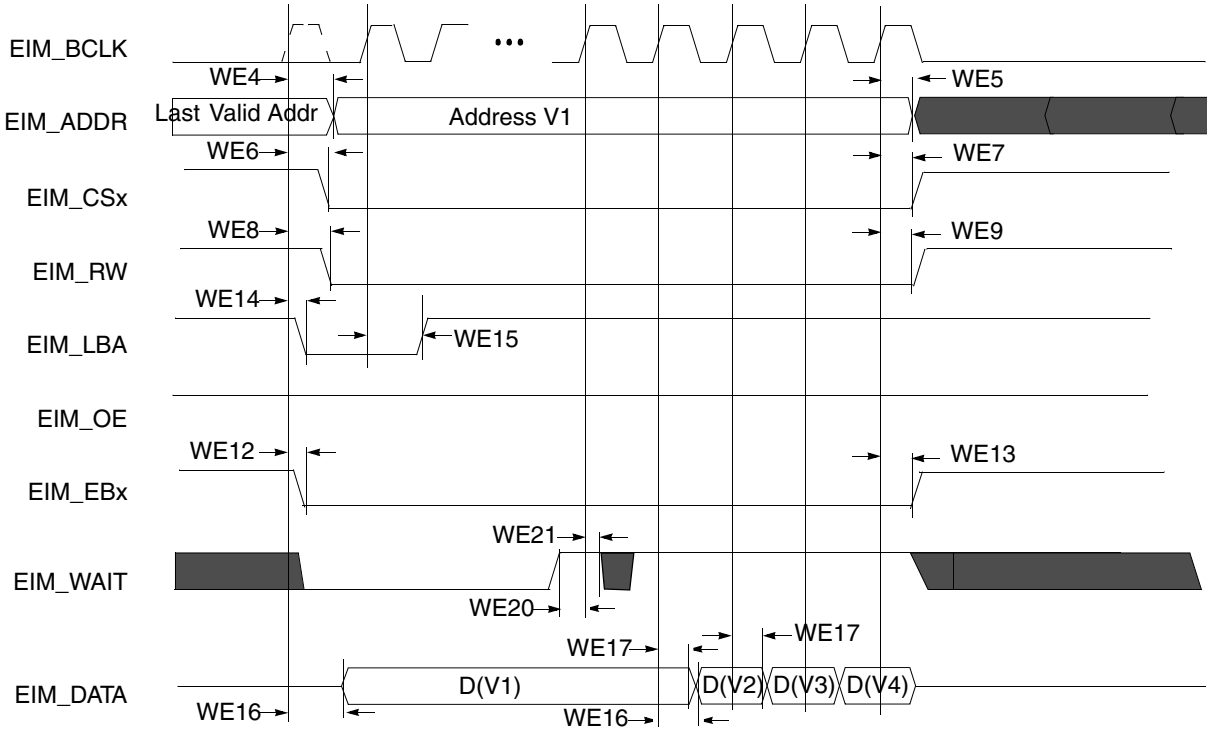

Figure 22. Synchronous Memory, Burst Write, BCS=1, WSC=4, SRD=1, and BCD=0

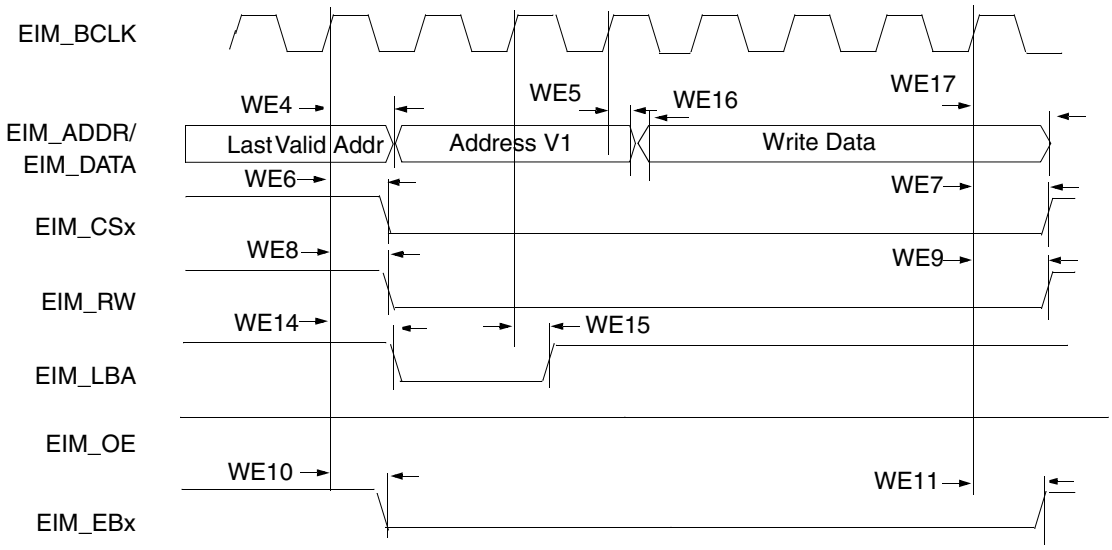

Figure 23. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6, ADVA=1, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode, the 16 MSBs are driven on the data bus.

4.8.1 DRAM Command & Address Output Timing—DDR2 and LPDDR1

The following diagrams and tables specify the timings related to the address and command pins, which interfaces DDR2 and LPDDR1 memory devices.

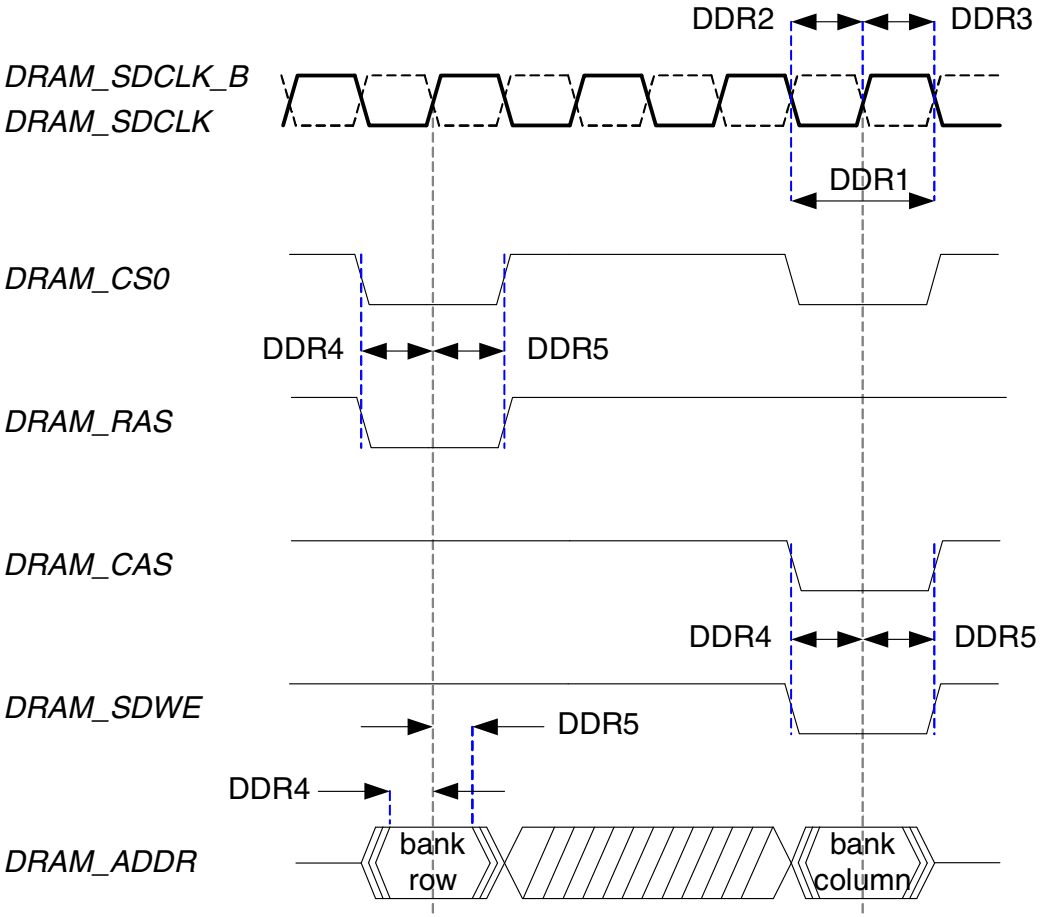

Figure 28. DRAM Command/Address Output Timing—DDR2 and LPDDR1

Table 45. EMI Command/Address AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR1	CK cycle time	tCK	3.75	—	ns
DDR2	CK high level width	tCH	0.48 tCK	0.52 tCK	ns
DDR3	CK low level width	tCL	0.48 tCK	0.52 tCK	ns
DDR4	Address and control output setup time	tIS	0.5 tCK - 0.3	—	ns
DDR5	Address and control output hold time	tIH	0.5 tCK - 0.3	—	ns

4.9.3 Enhanced Secured Digital Host Controller (eSDHCv2/v3) and uSDHC AC Timing

This section describes the electrical information of the eSDHCv2/v3 and the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4 (Dual Date Rate) timing.

4.9.3.1 SD/eMMC4.3 (Single Data Rate) eSDHCv3 and uSDHC AC Timing

Figure 36 depicts the timing of SD/eMMC4.3, and Table 54 lists the SD/eMMC4.3 timing characteristics.

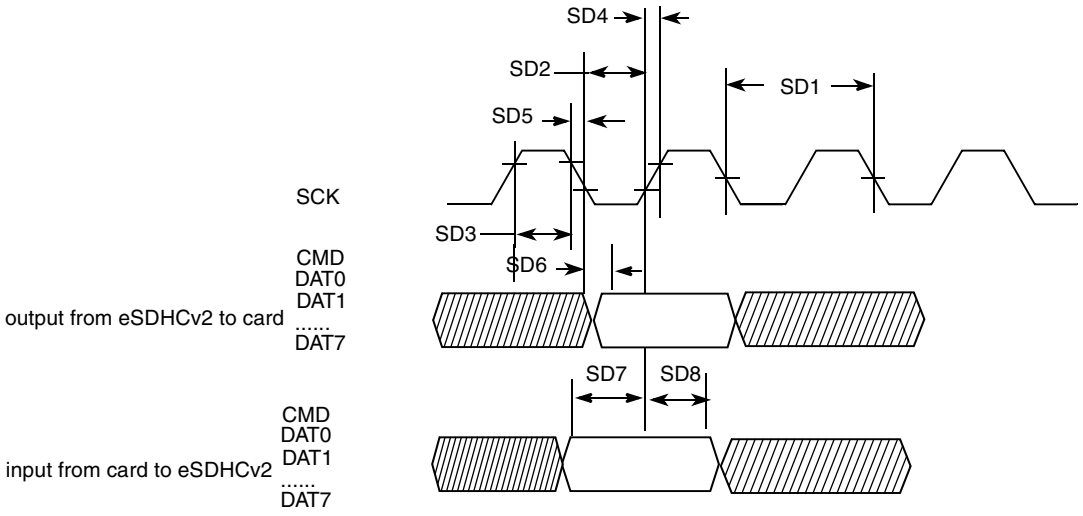

Figure 36. SD/eMMC4.3 Timing

Table 54. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns

Table 66. SSI Transmitter Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns
SS19	STXD rise/fall time	—	6.0	ns
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0.0	—	ns
SS52	Loading	—	25.0	pF

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in both the tables and figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms WL and BL refer to word length (WL) and bit length (BL).
- Tx and Rx refer to the transmit and receive sections of the SSI.
- For internal frame sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

Table 67. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS as shown in both the tables and figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- **Tx** and **Rx** refer to the transmit and receive sections of the SSI.
- The terms WL and BL refer to word length (WL) and bit length (BL).
- For internal frame sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in both the tables and figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- Tx and Rx refer to the transmit and receive sections of the SSI.
- The terms WL and BL refer to word length (WL) and bit length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.9.10 UART I/O Configuration and Timing Parameters

The following sections describe the UART I/O configuration and timing parameters.

4.9.10.1 UART RS-232 I/O Configuration in Different Modes

Table 70 shows the UART I/O configuration based on which mode is enabled.

Table 70. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
RTS	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
CTS	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
TXD_MUX	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
RXD_MUX	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.9.10.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

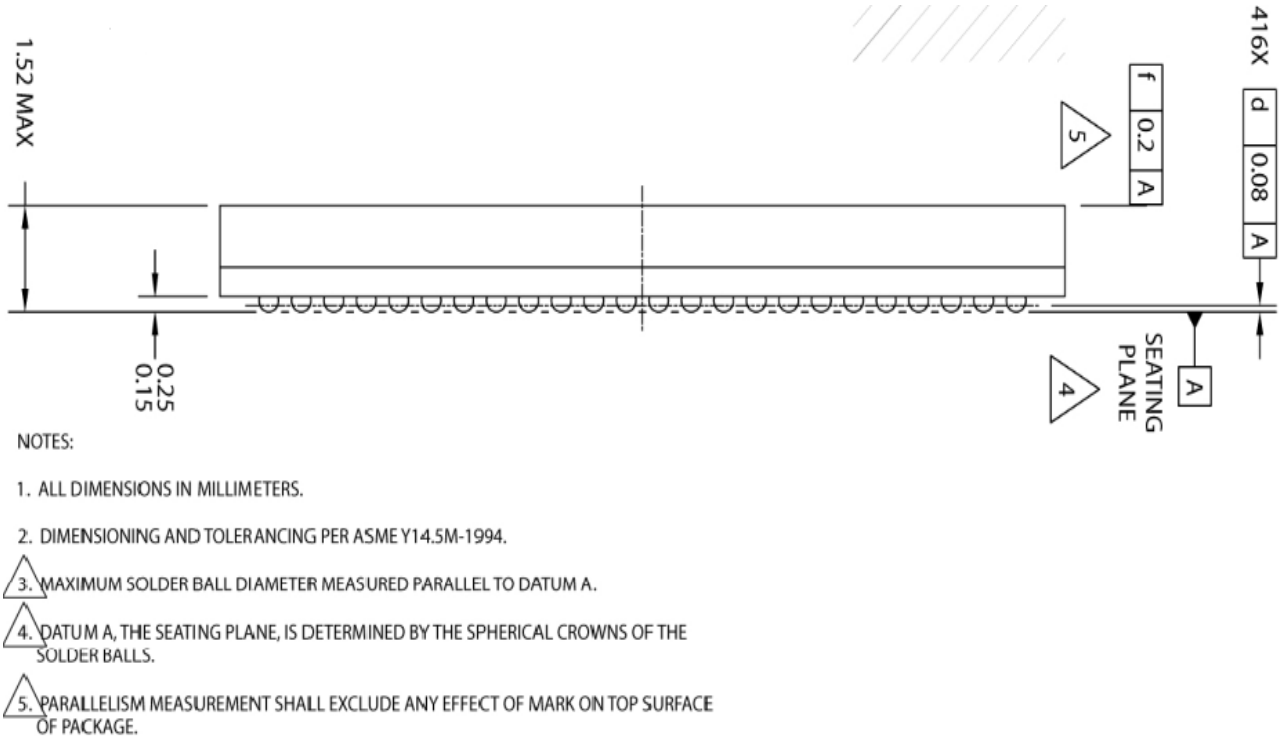

Figure 61. 416 MAPBGA 13x13 mm Package Side View

The following notes apply to Figure 59, Figure 60, and Figure 61:

- Unless otherwise specified dimensions are in millimeters.
- All dimensions and tolerances conform to ASME Y14.5M-1994.
- Parallelism measurement shall exclude any effect of mark on top surface of package.

5.2 13 x 13 mm, 0.5 mm Pitch, 416 Pin PoPBGA Package Information

This section contains the outline drawing, signal assignment map, ground, power, reference ID (by ball grid location) for the 13 x 13 mm, 0.5 mm pitch, 416 pin PoPBGA package.

5.2.1 416 PoPBGA 13 x 13 mm Package Views

Figure shows the top view of the 416 PoPBGA 13 x 13 package, Figure 63 shows the side view of the package, and Figure 64 shows the bottom view of the package.

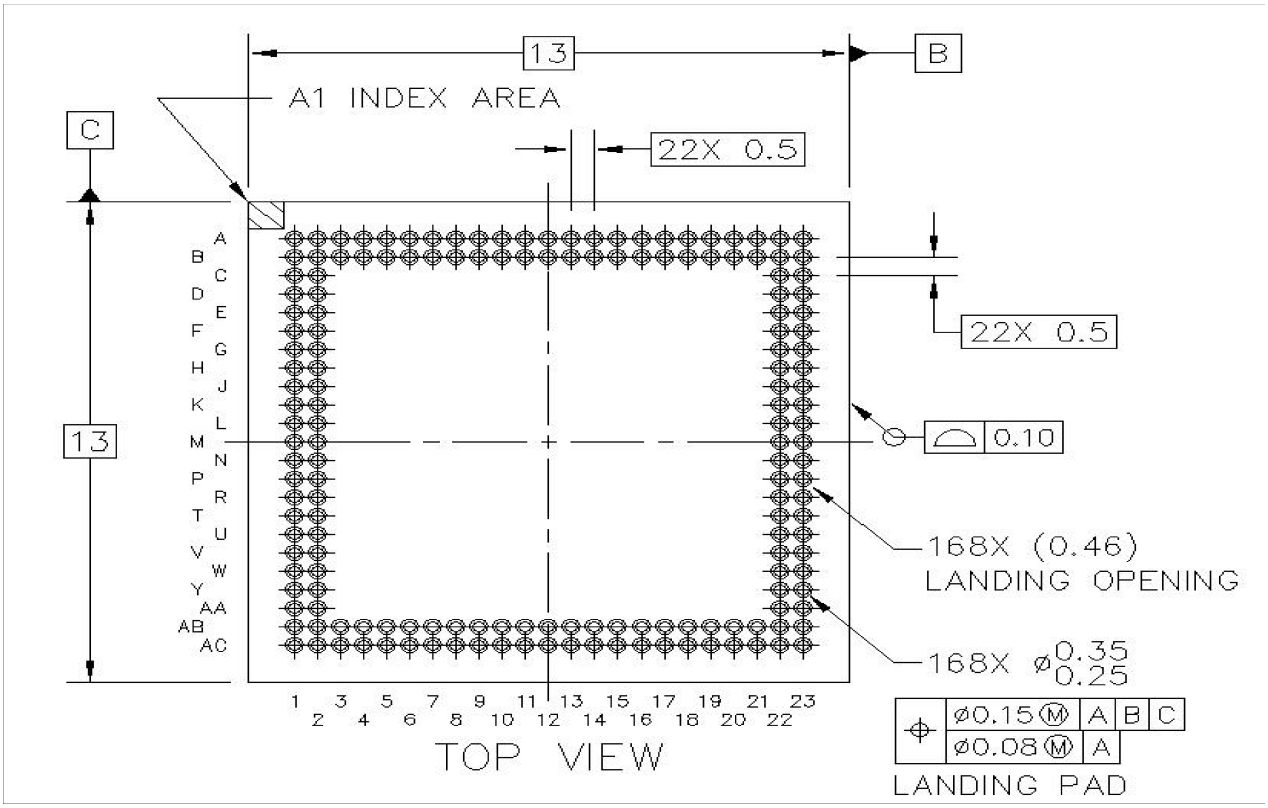

Figure 62. 416 PoPBGA 13 x 13 mm Package Top View

- All dimensions and tolerances conform to ASME Y14.5M-1994.
- Parallelism measurement shall exclude any effect of mark on top surface of package.

5.2.2 416 PoPBGA 13 x 13 mm, 0.5 Pitch Ball Map

Table 81 shows the 416 PoPBGA 13 x 13 mm ball map.

Table 81. 416 PoPBGA 13 x 13 mm Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A	VSS	UART1_RXD	UART1_TXD	I2C3_SCL	I2C2_SCL	I2C1_SCL	KEY_ROW3	KEY_ROW0	KEY_COL0	KEY_COL1	EIM_WAIT	EIM_BCLK	EIM_DA14	EIM_DA10	EIM_DA13	EIM_DA12	EIM_DA9	EIM_DA8	POP_EMMC_RST	POP_LPDDR2_1.8V	NVCC_EMI_DRAM	EIM_DA3	EIM_DA4	VSS
B	UART2_TXD	UART2_CTS	UART1_RTS	UART1_CTS	I2C3_SDA	I2C2_SDA	I2C1_SDA	KEY_ROW1	KEY_COL2	KEY_COL3	EIM_RDY	EIM_OE	EIM_LBA	EIM_RW	EIM_DA15	EIM_DA11	EIM_DA7	EIM_DA6	POP_LPDDR2_1.8V	POP_LPDDR2_1.8V	NVCC_EMI_DRAM	EIM_DA5	EIM_DA0	EIM_CS0
C	UART2_RXD	UART2_RTS	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	EIM_DA2	EIM_DA1
D	SD2_D0	SD2_D1	NC	UART3_TXD	UART4_RXD	UART4_TXD	KEY_ROW2	EPITO	WDOG	PWM2	PWM1	OWIRE	EIM_CRE	EIM_EB1	EIM_EB0	EIM_CS2	EIM_CS1	EPDC_SDCE5	POP_NAND_VCC	POP_NAND_VCC	NVCC_EMI_DRAM	NC	NVCC_EMI_DRAM	NVCC_EMI_DRAM
E	SD2_CLK	SD2_D5	NC	UART3_RXD	NVCC_EMI_DRAM	NVCC_EMI_DRAM	NVCC_EMI_DRAM	VSS	VSS	DRAM_D31	DRAM_D30	DRAM_D29	DRAM_D28	DRAM_D26	DRAM_D25	DRAM_SDQS3	VSS	VSS	DRAM_D15	DRAM_D14	VSS	NC	EPDC_PWRCOM	EPDC_PWRCTRL0
F	SD2_D2	SD2_D3	NC	SD2_D7	NVCC_EMI_DRAM	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	DRAM_D13	VSS	NC	EPDC_PWRCTRL2	EPDC_PWRSTAT

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
DISP_D6	AA15	AD16	U12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D7	Y15	AC19	V13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D8	AA16	AD17	W15	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D9	Y16	AC20	V15	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_RD	AD13	AA20	V12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_RESET	AC14	AA19	T14	NVCC_LCD	HVIO	ALT1	IN	Keeper
DISP_RS	AC13	AD23	Y12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_WR	AD12	AD20	V10	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DRAM_A0	W20	V7	T17	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A1	W21	Y7	T18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A10	K20	—	J19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A11	J20	—	H19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A12	H20	—	E19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A13	F21	—	F19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A14	F20	—	—	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A2	Y20	Y8	U18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A3	Y21	Y9	V18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A4	AA20	Y10	R17	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A5	P20	P7	K19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A6	P21	L5	L19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A7	N20	K5	K20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A8	N21	J5	L20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A9	L21	H5	G19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_CALIBRATION	L20	P4	F20	NVCC_EMI_DRAM	DRAMCALIB	—	—	—
DRAM_CAS	J21	—	G20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	Keeper
DRAM_CS0	T21	U5	P17	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	Keeper
DRAM_CS1	U21	U7	P18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	Keeper
DRAM_D0	Y24	V16	R20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D1	Y23	Y17	R19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
JTAG_TDI	AA4	AA4	U8	NVCC_JTAG	GPIO	ALT0	IN	47K PU
JTAG_TDO	U7	V4	T9	NVCC_JTAG	GPIO	ALT0	OUT-LO	Keeper
JTAG_TMS	Y4	Y4	R9	NVCC_JTAG	GPIO	ALT0	IN	47K PU
JTAG_TRSTB	AA5	AA5	U7	NVCC_JTAG	GPIO	ALT0	IN	47K PU
KEY_COL0	B1	A9	B1	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_COL1	B2	A10	B2	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_COL2	C1	B9	C1	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_COL3	C2	B10	C2	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW0	D1	A8	D1	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW1	D2	B8	D2	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW2	D4	D7	C3	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW3	E4	A7	D3	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
OWIRE	G7	D12	E5	NVCC_MISC	HVIO	ALT1	IN	Keeper
PMIC_ON_REQ	W1	W1	Y3	NVCC_SRTC	GPIO	ALT0	OUT-LO	—
PMIC_STBY_REQ	W2	W2	Y2	NVCC_SRTC	GPIO	ALT0	OUT-LO	—
POR_B	AD2	AD2	Y5	NVCC_RESET	LVIO	ALT0	IN	100K PU
PWM1	F5	D11	E4	NVCC_MISC	HVIO	ALT1	IN	Keeper
PWM2	F4	D10	E3	NVCC_MISC	HVIO	ALT1	IN	Keeper
RESET_IN_B	AC1	AC1	W3	NVCC_RESET	LVIO	ALT0	IN	100K PU
SD1_CLK	P1	M1	R1	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_CMD	R1	N1	P4	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D0	R2	P2	R2	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D1	P2	N2	P1	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D2	R4	M2	P3	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D3	R5	R4	P2	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD2_CD	T4	J4	T1	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_CLK	U1	E1	T3	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_CMD	V5	G1	V1	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D0	T1	D1	R3	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D1	T2	D2	U1	NVCC_SD2	HVIO	ALT1	IN	Keeper

6 Revision History

Table 86 provides a revision history for this data sheet.

Table 86. i.MX50 Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 7	10/2013	• Added new part number information for parts with 1 GHz core frequencies: — MCIMX508CVK1B — MCIMX508CVM1B — MCIMX507CVM1B — MCIMX507CVK1B Updated sections: — Section 1, “Introduction” — Table 1, “Ordering Information” — Table 11, “i.MX50 Operating Ranges” — Table 15, “Maximum Supply Current Consumption—ARM CLK = 1 GHz” (added)
Rev. 6	07/2013	• In Table 11, “i.MX50 Operating Ranges,” added VCC Stop mode ranges.
Rev. 5	05/2013	• In Table 11, “i.MX50 Operating Ranges,” changed VCC peripheral supply (LPM) minimum voltage from 0.9 V to 1 V, and changed nominal voltage from 0.95 V to 1.05 V.
Rev. 4	01/2013	• In Table 1, "Ordering Information," on page 7, added new part number information for MCIMX507CVK8B. • In Figure 27, "DTACK Read Access," on page 67, updated timing of EIM_DTACK.
Rev. 3	10/2012	• In Table 11, "i.MX50 Operating Ranges," on page 24: —Changed DDR clock rate for reduced performance mode (RPM) of VCC from 100 MHz to 133 MHz —Changed DDR clock rate for high performance mode (HPM) of VCC from 200 MHz to 266 MHz
Rev. 2	05/2012	• In Table 1, "Ordering Information," on page 7, added the following new part numbers: MCIMX508CZK8B, MCIMX503CVK8B, MCIMX503EVM8B, MCIMX502CVK8B, and MCIMX502EVM8B. • In Table 1, "Ordering Information," on page 7, added a new column, $T_{junction}$. • In Table 3, "Package Feature Comparison," on page 9, added a new row for 416 PoPBGA package. • Updated Figure 1, "i.MX50 System Block Diagram," on page 10 by removing “LDOx3” and “DC-DC 1.2V.” • In Table 5, "Special Signal Considerations," on page 17, updated details for the following signals: DRAM_OPEN/DRAM_OPENFB and DRAM_SDODT0/DRAM_SDODT1 • In Table 5, "Special Signal Considerations," on page 17, added new rows for the following signals: POP_EMMC_RST, POP_LPDDR2_ZQ0/ZQ1, POP_LPDDR2_1.8V, and POP_NAND_VCC. • Added Section 4.1.2.1, “13 x 13 mm MAPBGA Package Thermal Resistance Data.” • Added Section 4.1.2.2, “13 x 13 mm PoPBGA Package Thermal Resistance Data.” • Added Section 4.1.2.3, “17 x 17 mm MAPBGA Package Thermal Resistance Data.” • In Table 11, "i.MX50 Operating Ranges," on page 24, added footnotes for USB_OTG_VDDA25 and USB_OTG_VDDA33. • In Table 78, "VBUS Comparators Thresholds," on page 101, changed VBUS input max current to 350 µA. • Added Section 5.2, “13 x 13 mm, 0.5 mm Pitch, 416 Pin PoPBGA Package Information.” • In Table 85, "Alphabetical List of Signal Assignments," on page 124: —Added a new column “416 PoPBGA Ball Number” —Changed “USB_H1_VDDA” to “USB_H1_VDDA25, USB_H1_VDDA33” —Changed “USB_OTG_VDDA” to “USB_OTG_VDDA25, USB_OTG_VDDA33” • Replace mDDR with LPDDR1 throughout the document.