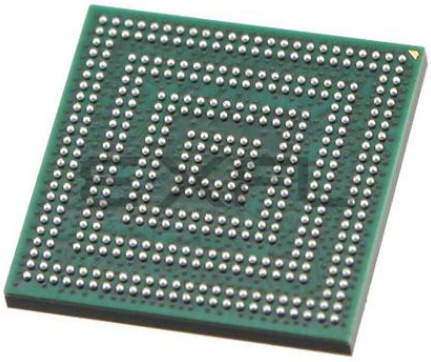


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Boot Security, Cryptography, Secure JTAG
Package / Case	416-LFBGA
Supplier Device Package	416-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx503cvk8br2

Table 4. i.MX50 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SDMA	Smart Direct Memory Access	Master Connectivity Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by offloading various cores in dynamic data routing. The SDMA features list is as follows: • Powered by a 16-bit instruction-set micro-RISC engine • Multi-channel DMA supports up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM Cortex-A8 and SDMA • Very fast context-switching with two-level priority-based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle uni-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers for EMI • Support of byte-swapping and CRC calculations • A library of scripts and API is available
SJC	Secure JTAG Controller	System Control Peripherals	The Secure JTAG Controller provides a mechanism for regulating JTAG access, preventing unauthorized JTAG usage while allowing JTAG access for manufacturing tests and software debugging. The i.MX50 JTAG port provides debug access to several hardware blocks including the ARM processor and the system bus, therefore, it must be accessible for initial laboratory bring-up, manufacturing tests and troubleshooting, and for software debugging by authorized entities. However, if the JTAG port is left unsecured it provides a method for executing unauthorized program code, getting control over secure applications, and running code in privileged modes. The Secure JTAG controller provides three different security modes that can be selected through an e-fuse configuration to prevent unauthorized JTAG access.
SPBA	Shared Peripheral Bus Arbiter	System Control Peripherals	SPBA (Shared Peripheral Bus Arbiter) is a two-to-one IP bus interface (IP bus) arbiter.
SRTC	Secure Real Time Clock	Security Peripherals	The SRTC incorporates a special System State Retention Register (SSRR) that stores system parameters during system shutdown modes. This register and all SRTC counters are powered by dedicated supply rail NVCC_SRTC. The NVCC_SRTC can be energized separately even if all other supply rails are shut down. This register is helpful for storing warm boot parameters. The SSRR also stores the system security state. In case of a security violation, the SSRR marks the event (security violation indication).

Table 7. Absolute Maximum Ratings (continued)

Parameter Description	Symbol	Min	Max	Unit
ESD damage immunity: Human Body Model (HBM) Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	V
Storage temperature range	$T_{STORAGE}$	–40	125	°C

1 The term OVDD in this section refers to the associated supply rail of an input or output. The maximum range can be superseded by the DC tables.

4.1.2 Thermal Resistance Data

4.1.2.1 13 x 13 mm MAPBGA Package Thermal Resistance Data

Table 8 provides thermal resistance data for a 13 x 13 mm MAPBGA package.

Table 8. 13 x 13 mm MAPBGA Package Thermal Resistance Data

Rating	Board	Symbol	Value	Unit
Junction to Ambient (natural convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	51	°C/W
Junction to Ambient (natural convection)[1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	28	°C/W
Junction to Ambient (at 200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	40	°C/W
Junction to Ambient (at 200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	24	°C/W
Junction to Board[4]	—	$R_{\theta JB}$	14	°C/W
Junction to Case[5]	—	$R_{\theta JC}$	9	°C/W
Junction to Package Top (natural convection)[6]	—	Ψ_{JT}	2	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per JEDEC JESD51-2 with the single layer board horizontal. The thermal test board meets JESD51-9 specification.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by using the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 18. GPIO DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	MIN	Typ	MAX	Units
High-level output current (1.1-1.3V ovdd)	I Ioh	Voh=0.8*OVDD Low Drive Medium Drive High Drive Max Drive	 -0.85 -1.7 -2.5 -3.4	—	—	 mA
Low-level output current (1.1-1.3V ovdd)	I Iol	Vol=0.2*OVDD Low Drive Medium Drive High Drive Max Drive	 0.9 1.9 2.9 3.8	—	—	 mA
High-level output current (1.65-3.1V ovdd)	I Ioh	Voh=0.8*OVDD Low Drive Medium Drive High Drive Max Drive	 -2.1 -4.2 -6.3 -8.4	—	—	 mA
Low-level output current (1.65-3.1V ovdd)	I Iol	Vol=0.2*OVDD Low Drive Medium Drive High Drive Max Drive	 2.1 4.2 6.3 8.4	—	—	 mA
High-Level DC input voltage [1]	VIH	—	0.7*OVDD	—	OVDD	V
Low-Level DC input voltage	VIL	—	0V	—	0.3*OVDD	V
Input Hysteresis	VHYS	OVDD=1.875 OVDD=2.775	0.25	0.34 0.45	—	V
Schmitt trigger VT+ [2]	VT+	—	0.5*OVDD	—	—	V
Schmitt trigger VT-	VT-	—	—	—	0.5*OVDD	V
Pull-up resistor (22 KΩ PU)	Rpu	Vi=OVDD/2	20	24	28	KΩ
Pull-up resistor (47 KΩ PU)	Rpu	Vi=OVDD/2	43	51	59	KΩ
Pull-up resistor (100 KΩ PU)	Rpu	Vi=OVDD/2	91	108	125	KΩ
Pull-down resistor (100 KΩ PD)	Rpd	Vi=OVDD/2	91	108	126	KΩ
Input current (no pull-up/down)	IIN	VI = 0 VI=OVDD	—	1.7	250 120	nA
Input current (22 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	161 0.12	μA
Input current (47 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	76 0.12	μA
Input current (100 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	36 0.12	μA

4.3.3 Low Power DDR2 I/O DC Parameters

The LPDDR2 interface fully complies with JEDEC standard release April, 2008. The parameters in Table 20 are guaranteed per the operating ranges in Table 11, unless otherwise noted.

Table 20. LPDDR2 I/O DC Electrical Parameters

DC Electrical Characteristics	Symbol	Test Conditions	MIN	TYP	MAX	Units
High-level output voltage	Voh	—	0.9*ovdd	—	—	V
Low-level output voltage	Vol	—	—	—	0.1*ovdd	V
Input reference voltage	Vref	—	0.49*ovdd	0.5*ovdd	0.51*ovdd	—
DC input high voltage	Vih(dc)	—	Vref+0.13	—	ovdd	V
DC input low voltage	Vil(dc)	—	ovss	—	Vref-0.13	V
Differential input logic high[1]	Vih(diff)	—	0.26	—	—	V
Differential input logic low[1]	Vil(diff)	—	—	—	-0.26	V
Input current (no pull-up/down)	Iin	VI = 0 VI=ovdd	—	0.02 1.5	12.8 290	nA
Tri-state I/O supply current[2]	Icc-ovdd	VI = ovdd or 0	—	1.85	400	nA
Tri-state 2.5 V predrivers supply current[2]	Icc-vdd2p5	VI = ovdd or 0	—	5	700	nA
Tri-state core supply current[2]	Icc-vddi	VI = ovdd or 0	—	3	700	nA
Pullup/Pulldown impedance mismatch[2]	—	—	-15	—	+15	%
240 Ω unit calibration resolution	—	—	—	—	10	Ω

1 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

2 Typ condition: typ model, 1.2V, and 25 °C. Max condition: BCS model, 1.3V, and 125 °C. Min condition: WCS model, 1.14V, and -40 °C.

4.3.4 Low Power DDR1 I/O DC Parameters

The LPDDR1 interface fully complies with JEDEC standard release April, 2008. The parameters in Table 21 are guaranteed per the operating ranges in Table 11, unless otherwise noted.

Table 21. LPDDR1 Mode DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	MIN	TYP	MAX	Units
High-level output voltage	Voh	Ioh=-0.1mA	0.9*ovdd	—	—	V
Low-level output voltage	Vol	Iol=0.1mA	—	—	0.1*ovdd	V
DC input high voltage (data pins)	Vihd(dc)	—	0.7*ovdd	—	ovdd+0.3	V
DC input low voltage (data pins)	Vild(dc)	—	-0.3	—	0.3*ovdd	V
DC input voltage[1] (clk pins)	Vin(dc)	—	-0.3	—	ovdd+0.3	V
DC input differential voltage[2]	Vid(dc)	—	0.4*ovdd	—	ovdd+0.6	V
Input current[3] (no pull-up/down)	Iin	VI = 0 VI=ovdd	—	0.07 2	5 360	nA
Tri-state I/O supply current[3]	Icc-ovdd	VI = ovdd or 0	—	2.3	480	nA
Tri-state 2.5V predrivers supply current[3]	Icc-vdd2p5	VI = ovdd or 0	—	5.3	680	nA
Tri-state core supply current[3]	Icc-vddi	VI = ovdd or 0	—	3.1	720	nA

4.4.3 HVIO Output Buffer Impedance

Table 26 shows the HVIO output buffer impedance of the i.MX50 processor.

Table 26. HVIO Output Buffer Impedance

Parameter	Symbol	Test Conditions	Min		Typ		Max		Unit
			OVDD 1.95 V	OVDD 3.3 V	OVDD 1.875 V	OVDD 3.30V	OVDD 1.65 V	OVDD 2.68 V	
Output driver impedance	Rpu	Low drive strength, Ztl = 150 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω	113.5 56.2 37.8	103.8 51.9 35.1	130.6 66 45.9	133 69.2 41	219.4 109.7 73.1	212.2 111.1 71.8	Ω
Output driver impedance	Rpd	Low drive strength, Ztl =1 50 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω	78.5 39.7 26.8	70 34.5 23	113.6 56.8 38.3	102 50 33.3	230.8 115.4 76.9	179.5 89.8 60.7	Ω

NOTE

Output driver impedance is measured with *long* transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 3).

4.5.7 DDR2 I/O AC Parameters

Table 33 shows the AC parameters for DDR2 I/O.

Table 33. DDR2 I/O AC Parameters

Parameter	Symbol	Min	Max	Unit
AC input logic high	Vih(ac)	Vref+0.25	-	V
AC input logic low	Vil(ac)	-	Vref-0.25	
AC differential input voltage[1]	Vid(ac)	0.5	ovdd	
AC Input differential cross point voltage[2]	Vix(ac)	0.5*ovdd -0.175	0.5*ovdd + 0.175	
AC output differential cross point voltage [3]	Vox(ac)	0.5*ovdd -0.125	0.5*ovdd+ 0.125	
Output propagation delay high to low	t_{POHLD}		3.5	ns
Output propagation delay low to high	t_{POLHD}		3.5	
Input propagation delay high to low	t_{PIHLD}		1.5	
Input propagation delay low to high	t_{PILHD}		1.5	
Single output slew rate	tsr	0.4	2	V/ns

[1]Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac)-Vil(ac)

[2]The typical value of Vix(ac) is expected to be about 0.5*OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

[3]The typical value of Vox(ac) is expected to be about 0.5*OVDD and Vox(ac) is expected to track variation in OVDD. Vox(ac) indicates the voltage at which differential output signal must cross.

Table 39. DPLL Electrical Parameters (continued)

Parameter	Test Conditions/Remarks	Min	Typ	Max	Unit
Frequency lock time[4] (FOL mode or non-integer MF)	—	—	—	398	T_{dpdref}
Phase lock time	—	—	—	100	µs
Frequency jitter[5] (peak value)	—	—	0.02	0.04	T_{dck}
Phase jitter (peak value)	FPL mode, integer and fractional MF	—	2.0	3.5	ns
Power dissipation	f_{dck} = 300 MHz @ avdd = 1.8 V, dvdd = 1.2 V f_{dck} = 650 MHz @ avdd = 1.8 V, dvdd = 1.2 V	—	—	0.65 (avdd) 0.92 (dvdd) 1.98 (avdd) 1.8 (dvdd)	mW

1 Device input range cannot exceed the electrical specifications of the CAMP, see Table 38.

2 The values specified here are internal to DPLL. Inside the DPLL, a 1 is added to the value specified by the user. Therefore, the user has to enter a value 1 less than the desired value at the inputs of DPLL for PDF and MFD.

3 The maximum total multiplication factor (MFI + MFN/MFD) allowed is 15. Therefore, if the MFI value is 15, MFN value must be zero.

4 T_{dpdref} is the time period of the reference clock after predivider. According to the specification, the maximum lock time in FOL mode is 398 cycles of divided reference clock when DPLL starts after full reset.

5 T_{dck} is the time period of the output clock, dpdck_2.

4.6.5 General Purpose Media Interface (GPMI) Parameters

The i.MX50 GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous timing mode, Source Synchronous timing mode and Samsung Toggle timing mode separately described in the following paragraphs.

4.6.5.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The Maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 8, Figure 9, Figure 10 and Figure 11 depict the relative timing between GPMI signals at the module level for different

operations under Asynchronous mode. Table 40 describes the timing parameters (NF1–NF17) that are shown in the figures.

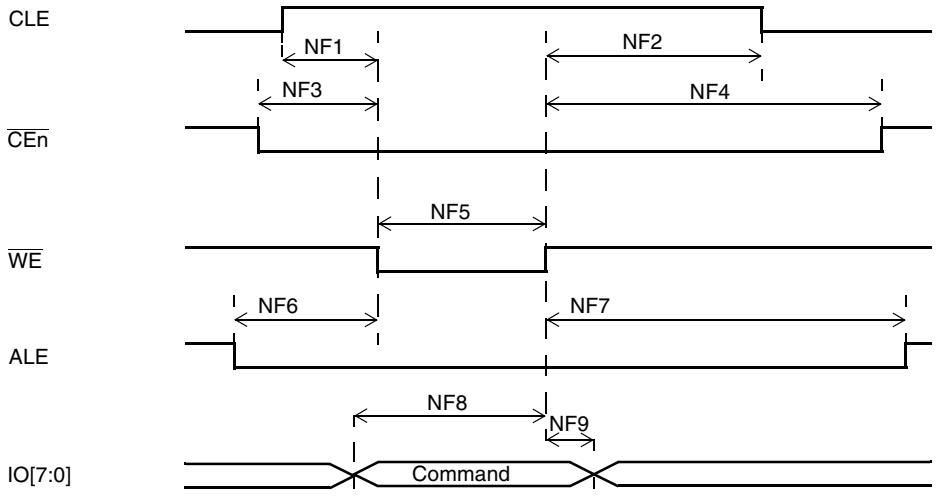


Figure 8. Command Latch Cycle Timing Diagram

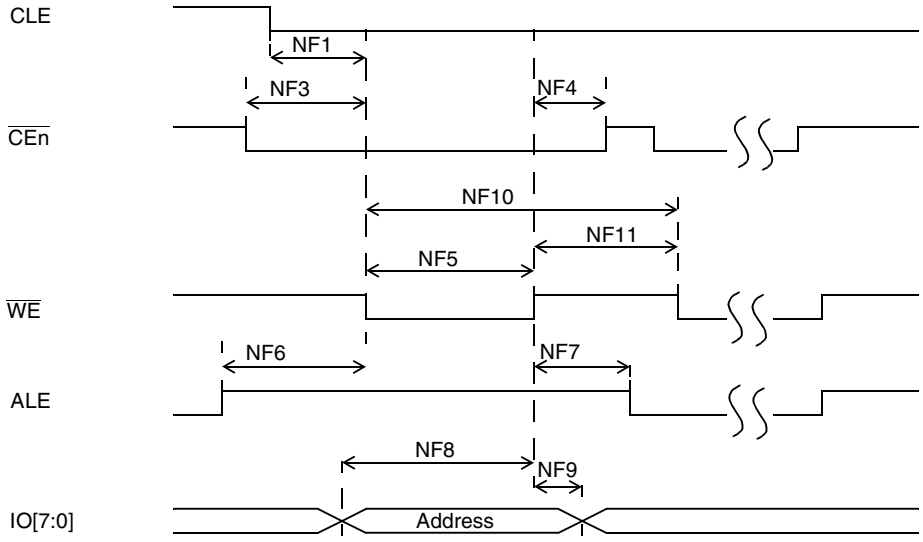


Figure 9. Address Latch Cycle Timing Diagram

Table 40. Asynchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T[2] = GPMI Clock Cycle[3]		Example Timing for GPMI Clock ≈ 100MHz T = 10ns		Unit
			Min.	Max.	Min.	Max.	
NF5	$\overline{WE}$ pulse width	tWP	DS*T		10		ns
NF6	ALE setup time	tALS	(AS+1)*T	—	10	—	ns
NF7	ALE hold time	tALH	(DH+1)*T	—	20	—	ns
NF8	Data setup time	tDS	DS*T	—	10	—	ns
NF9	Data hold time	tDH	DH*T	—	10	—	ns
NF10	Write cycle time	tWC	(DS+DH)*T		20		ns
NF11	$\overline{WE}$ hold time	tWH	DH*T		10		ns
NF12	Ready to $\overline{RE}$ low	tRR	(AS+1)*T	—	10	—	ns
NF13	$\overline{RE}$ pulse width	tRP	DS*T	—	10	—	ns
NF14	READ cycle time	tRC	(DS+DH)*T	—	20	—	ns
NF15	$\overline{RE}$ high hold time	tREH	DH*T		10	—	ns
NF16	Data setup on read	tDSR	N/A		10	—	ns
NF17	Data hold on read	tDHR	N/A		10	—	ns

1 GPMI's Async Mode output timing could be controlled by module's internal register, say HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers' setting. In the above table, we use AS/DS/DH representing these settings each.

2 T represents for the GPMI clock period.

3 AS minimum value could be 0, while DS/DH minimum value is 1.

4.6.5.2 Source Synchronous Mode AC Timing (ONFI 2.x Compatible)

The following diagrams show the write and read timing of Source Synchronous Mode.

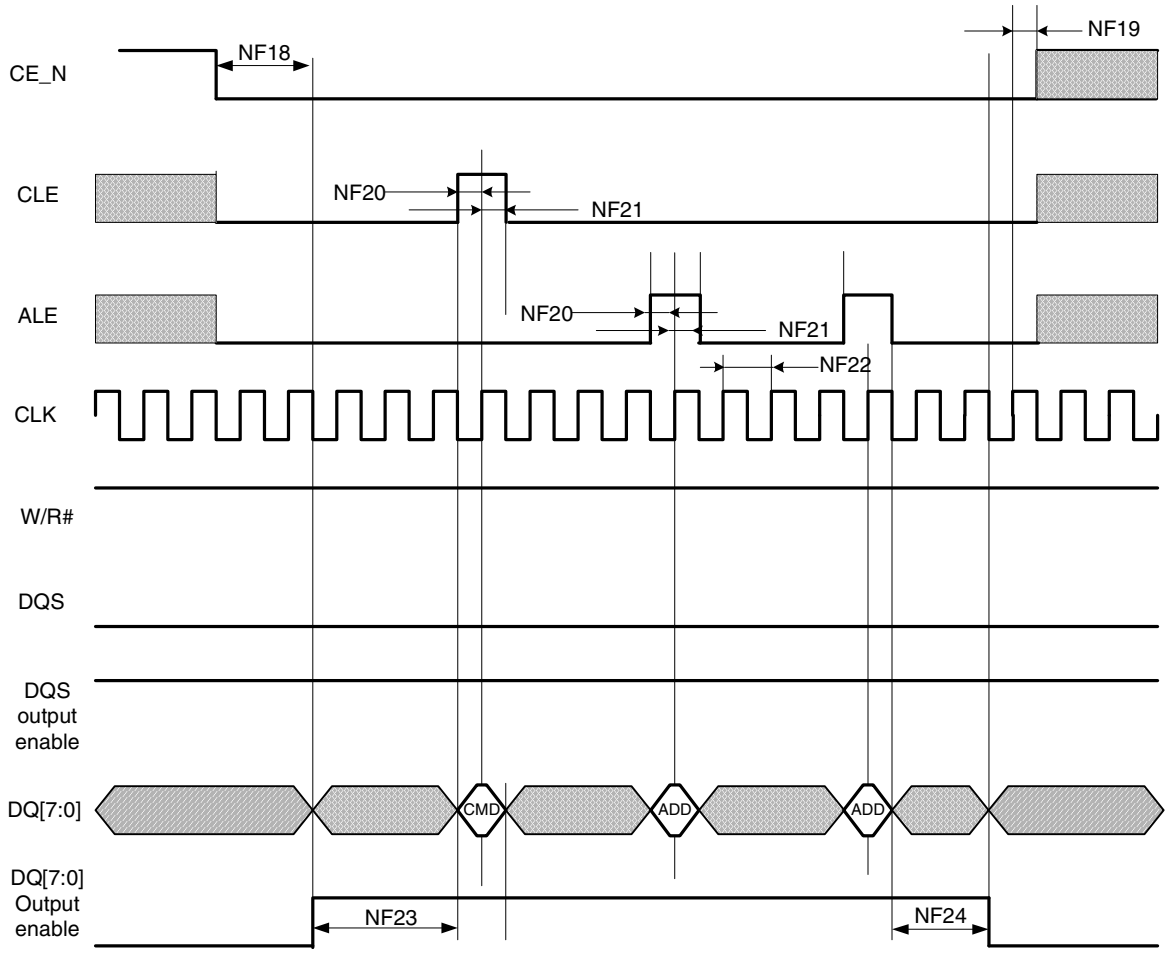


Figure 12. Source Synchronous Mode Command and Address Timing Diagram

Table 41. Source Synchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF24	postamble delay	t_{POST}	POST_DELAY*t_{CK}	—	ns
NF25	CLE and ALE setup time	t_{CALS}	0.5*t_{CK}	—	ns
NF26	CLE and ALE hold time	t_{CALH}	0.5*t_{CK}	—	ns
NF27	Data input to first DQS latching transition	t_{DQSS}	t_{CK}	—	ns

1 GPMI's sync mode output timing could be controlled by module's internal register, say HW_GPMI_TIMING2_CE_DELAY, HW_GPMI_TIMING_PREAMBLE_DELAY, and HW_GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers' setting. In the above table, we use CE_DELAY/PRE_DELAY/POST_DELAY representing these settings each.

4.6.5.3 Samsung Toggle Mode AC Timing

4.6.5.3.1 Command and Address Timing

NOTE

Samsung Toggle Mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. Please refer to the above chapter for details.

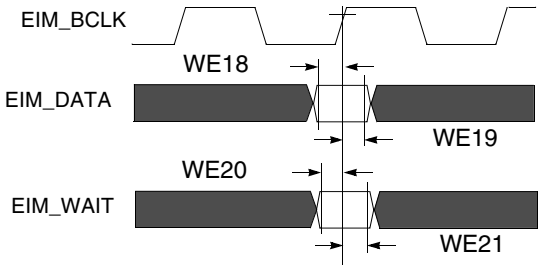
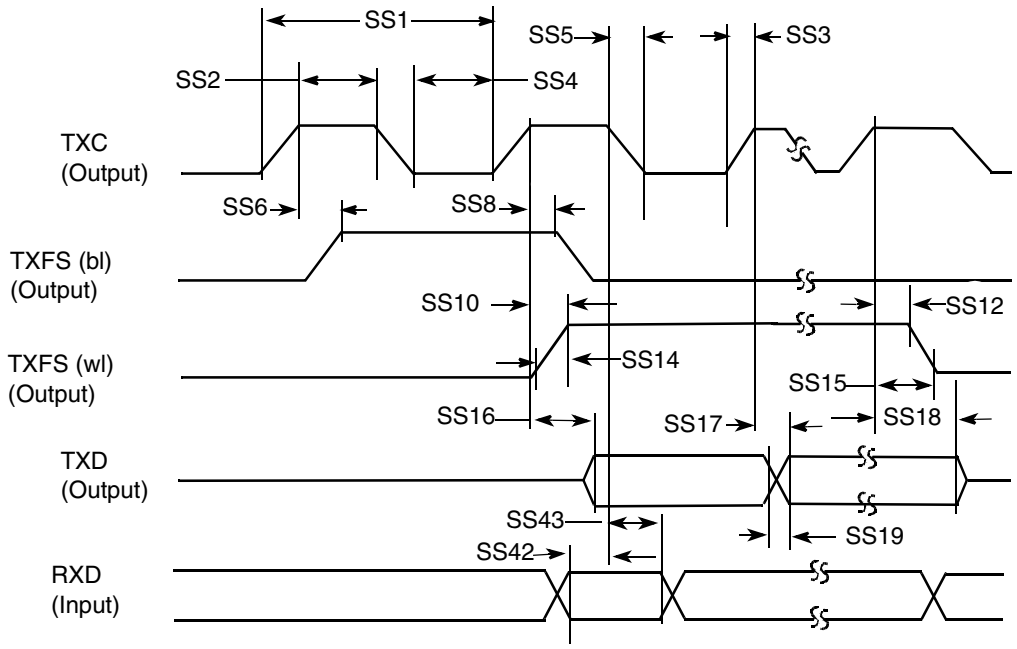


Figure 18. EIM Inputs Timing Diagram

4.9.9.1 SSI Transmitter Timing with Internal Clock

Figure 51 depicts the SSI transmitter internal clock timing and Table 66 lists the timing parameters for the SSI transmitter internal clock.



Note: SRXD input in synchronous mode only

Figure 51. SSI Transmitter Internal Clock Timing Diagram

Table 66. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6.0	ns
SS15	(Tx/Rx) Internal FS fall time	—	6.0	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns

Table 66. SSI Transmitter Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns
SS19	STXD rise/fall time	—	6.0	ns
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0.0	—	ns
SS52	Loading	—	25.0	pF

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in both the tables and figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms WL and BL refer to word length (WL) and bit length (BL).
- Tx and Rx refer to the transmit and receive sections of the SSI.
- For internal frame sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

5.1.2 416 MAPBGA 13 x 13 mm, 0.5 mm Pitch Ball Map

Table 79 shows the 416 MAPBGA 13 x 13 mm, 0.5 mm pitch ball map.

Table 79. 416 MAPBGA 13x13 mm, 0.5 mm Pitch Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
A	VSS	EIM_RDY	EIM_CRE	EIM_EB0	EIM_BCLK	EIM_DA12	EIM_DA8	EIM_DA4	EIM_DA0	EPDC_SDSHR	EPDC_GDCLK	EPDC_GDRL	EPDC_SDCLK	EPDC_D12	EPDC_D8	EPDC_D4	EPDC_D0	VSS	DRAM_D30	DRAM_D29	NVCC_EMI_DRAM	DRAM_D26	DRAM_D25	VSS	A
B	KEY_COL0	KEY_COL1	EIM_OE	EIM_EB1	EIM_RW	EIM_DA13	EIM_DA9	EIM_DA5	EIM_DA1	EIM_CS0	EPDC_GDOE	EPDC_GDSP	EPDC_SDCLKN	EPDC_D13	EPDC_D9	EPDC_D5	EPDC_D1	VSS	DRAM_D31	DRAM_D28	NVCC_EMI_DRAM	DRAM_D27	DRAM_D24	DRAM_DQM3	B
C	KEY_COL2	KEY_COL3	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	DRAM_SDQS3	DRAM_SDQS3_B	C
D	KEY_ROW0	KEY_ROW1	NC	KEY_ROW2	EIM_WAIT	EIM_DA14	EIM_DA10	EIM_DA6	EIM_DA2	EIM_CS1	EPDC_SDCE4	EPDC_SDCE2	EPDC_SDCE0	EPDC_D14	EPDC_D10	EPDC_D6	EPDC_D2	EPDC_SDLE	EPDC_SDOED	EPDC_VCOM1	NVCC_EMI_DRAM	NC	NVCC_EMI_DRAM	NVCC_EMI_DRAM	D
E	I2C1_SCL	I2C1_SDA	NC	KEY_ROW3	EIM_LBA	EIM_DA15	EIM_DA11	EIM_DA7	EIM_DA3	EIM_CS2	EPDC_SDCE5	EPDC_SDCE3	EPDC_SDCE1	EPDC_D15	EPDC_D11	EPDC_D7	EPDC_D3	EPDC_SDOE	EPDC_SDOEZ	EPDC_BDR0	EPDC_BDR1	NC	DRAM_D15	DRAM_D14	E
F	I2C2_SCL	I2C2_SDA	NC	PWM2	PWM1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	DRAM_A14	DRAM_A13	NC	DRAM_D12	DRAM_D13	F
G	I2C3_SCL	I2C3_SDA	NC	EPITO	WDOG	NC	OWIRE	VDDGP	VDDGP	VDDGP	EPDC_PWRCOM	EPDC_PWRCTRL0	EPDC_PWRCTRL1	EPDC_PWRCTRL2	EPDC_PWRCTRL3	EPDC_PWRSTAT	EPDC_VCOM0	DRAM_SDODT0	NC	VSS	VSS	NC	VSS	DRAM_D10	G

Table 79. 416 MAPBGA 13x13 mm, 0.5 mm Pitch Ball Map (continued)

P	N	M	L	K	J	H
SD1_CLK	ECSPI1_SCLK	CSPI_SCLK	UART2_RXD	UART2_TXD	UART1_RXD	UART1_TXD
SD1_D1	ECSPI1_MOSI	CSPI_MOSI	UART2_RTS	UART2_CTS	UART1_RTS	UART1_CTS
NC	NC	NC	NC	NC	NC	NC
ECSPI2_SCLK	ECSPI2_SS0	CSPI_SS0	UART3_RXD	UART3_TXD	SSI_TXC	SSI_TXFS
ECSPI2_MOSI	ECSPI2_MISO	CSPI_MISO	UART4_RXD	UART4_TXD	SSI_RXD	SSI_TXD
NC	NC	NC	NC	NC	NC	NC
ECSPI1_SS0	ECSPI1_MISO	NVCC_EIM	NVCC_EIM	VDDGP	SSI_RXC	SSI_RXFS
NVCC_MISC	NVCC_KEYPAD	NVCC_EIM	VDDGP	VDDGP	VDDGP	VDDGP
NC	NC	NC	NC	NC	NC	VDDGP
NVCC_EPDC	NVCC_EPDC	NVCC_EPDC	VDDGP	VDDGP	NC	VDDGP
VSS	VSS	VSS	VDDGP	VDDGP	NC	VDDGP
VSS	NC	NC	VSS	VSS	NC	VSS
VSS	NC	NC	VSS	VSS	NC	VSS
VSS	VSS	VSS	VSS	VCC	NC	VCC
VDDAL1	VSS	VSS	VCC	VCC	NC	VCC
NC	NC	NC	NC	NC	NC	VCC
VDDA	VSS	VSS	VSS	VCC	VCC	VCC
DRAM_SDWE	DRAM_SDBA2	VSS	DRAM_SDBA1	DRAM_SDBA0	DRAM_OPEN	DRAM_OPENFB
NC	NC	NC	NC	NC	NC	NC
DRAM_A5	DRAM_A7	VSS	DRAM_CALIBRATION	DRAM_A10	DRAM_A11	DRAM_A12
DRAM_A6	DRAM_A8	VSS	DRAM_A9	NVCC_EMI_DRAM	DRAM_CAS	DRAM_RAS
NC	NC	NC	NC	NC	NC	NC
DRAM_SDQS0	VDDO25	VREF	DRAM_SDQS1	NVCC_EMI_DRAM	DRAM_D8	DRAM_D11
DRAM_SDQS0_B	DRAM_SDCLK_0	DRAM_SDCLK_0_B	DRAM_SDQS1_B	NVCC_EMI_DRAM	DRAM_DQM1	DRAM_D9
P	N	M	L	K	J	H

Table 79. 416 MAPBGA 13x13 mm, 0.5 mm Pitch Ball Map (continued)

AA	Y	W	V	U	T	R
NVCC_SRTC	CKIL	PMIC_ON_REQ	SD2_D2	SD2_CLK	SD2_D0	SD1_CMD
NGND_SRTC	ECKIL	PMIC_STBY_REQ	SD2_D3	SD2_D5	SD2_D1	SD1_D0
NC	NC	NC	NC	NC	NC	NC
JTAG_TDI	JTAG_TMS	JTAG_TCK	SD2_D4	SD2_D6	SD2_CD	SD1_D2
JTAG_TRSTB	VDD_DCDCO	GND_DCDC	SD2_CMD	SD2_D7	SD2_WP	SD1_D3
CKIH	VDD_DCDCI	NC	NC	NC	NC	NC
GND_KEL	USB_OTG_GPANAIO	NC	JTAG_MOD	JTAG_TDO	NVCC_SD1	NVCC_SPI
USB_OTG_RREFEXT	USB_OTG_ID	NC	NVCC_RESET	NVCC_SD2	NVCC_UART	NVCC_SSI
VSS	USB_OTG_VBUS	NC	NVCC_NANDF	NVCC_JTAG	NC	NC
USB_H1_RREFEXT	USB_H1_VBUS	NC	NVCC_NANDF	NVCC_EPDC	NC	NVCC_EPDC
VSS	USB_H1_GPANAIO	NC	CHGR_DET_B	NVCC_LCD	NC	VSS
DISP_D0	DISP_D1	NC	DISP_D11	VSS	NC	VSS
DISP_D2	DISP_D3	NC	DISP_D12	VSS	NC	VSS
DISP_D4	DISP_D5	NC	DISP_D13	VSS	NC	VSS
DISP_D6	DISP_D7	NC	DISP_D14	VSS	NC	VDDAL1
DISP_D8	DISP_D9	NC	DISP_D15	VSS	NC	NC
SD3_D3	DISP_D10	NC	VSS	VSS	VSS	VDDA
SD3_D4	SD3_D5	NC	VSS	VSS	VSS	DRAM_SDODT1
SD3_D6	SD3_D7	NC	NC	NC	NC	NC
DRAM_A4	DRAM_A2	DRAM_A0	VSS	DRAM_SDCKE	DRAM_SDCLK_1	DRAM_SDCLK_1_B
NVCC_EMI_DRAM	DRAM_A3	DRAM_A1	VSS	DRAM_CS1	DRAM_CS0	NVCC_EMI_DRAM
NC	NC	NC	NC	NC	NC	NC
NVCC_EMI_DRAM	DRAM_D1	DRAM_D2	VSS	DRAM_D5	DRAM_D6	NVCC_EMI_DRAM
NVCC_EMI_DRAM	DRAM_D0	DRAM_D3	DRAM_D4	DRAM_D7	DRAM_DQM0	NVCC_EMI_DRAM
AA	Y	W	V	U	T	R

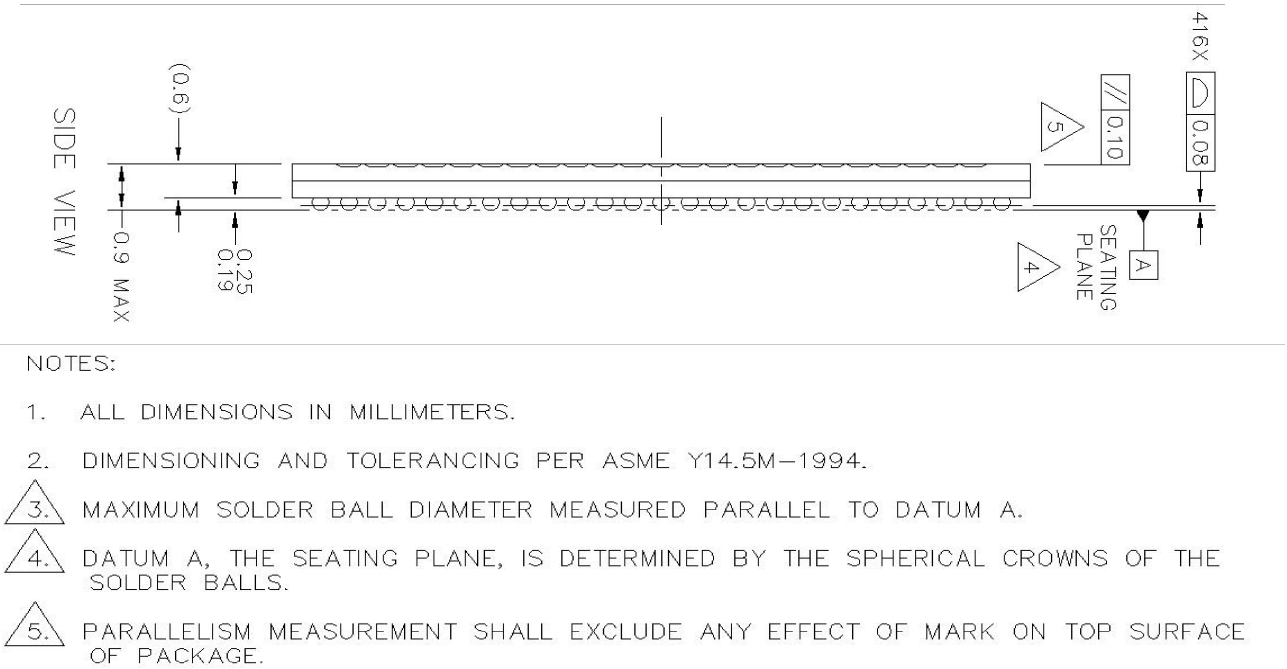


Figure 63. 416 PoPBGA 13 x 13 Package Side View

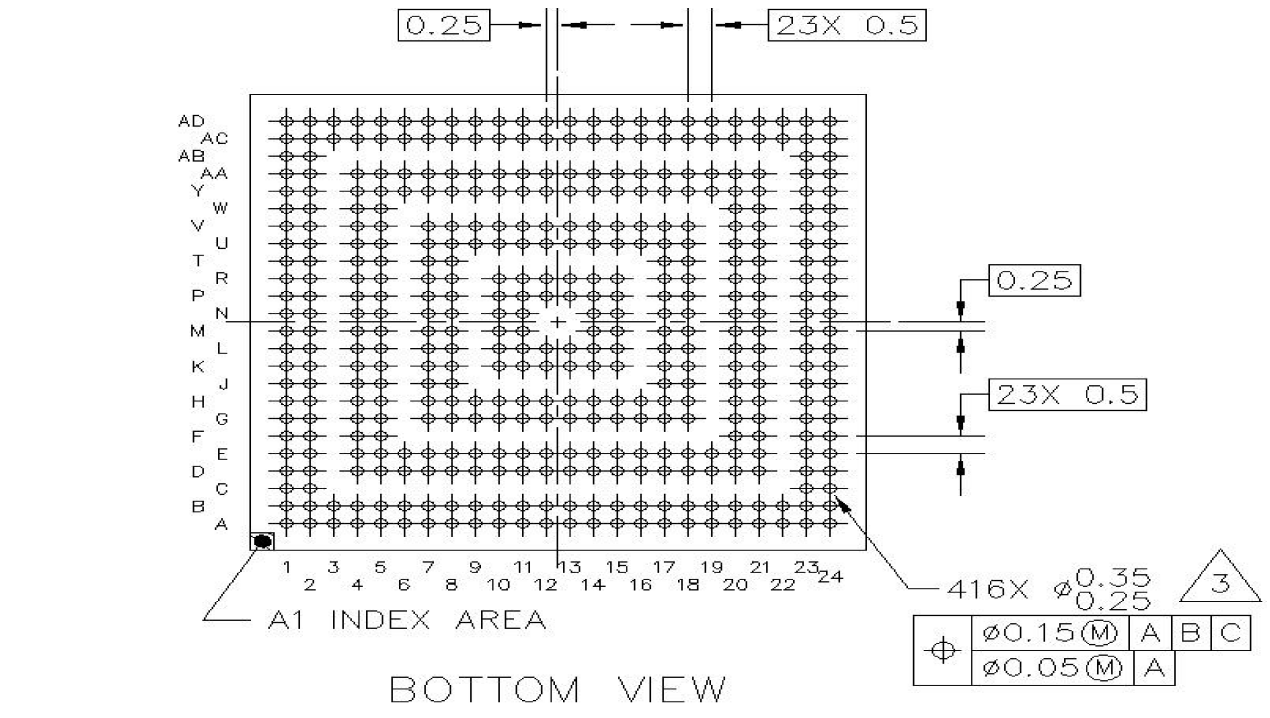


Figure 64. 416 PoPBGA 13 x 13 mm Package Bottom View

The following notes apply to Figure , Figure 63, and Figure 64:

- Unless otherwise specified dimensions are in millimeters.

Table 83. 400 MAPBGA 17 x 17 mm Ball Map (continued)

Y	W	V	U
NC	SD2_D7	SD2_CMD	SD2_D1
PMIC_STBY_REQ	SD2_D2	SD2_D4	SD2_D5
PMIC_ON_REQ	RESET_IN_B	BOOT_MODE0	BOOT_MODE1
CKIL	ECKIL	CKIH	TEST_MODE
POR_B	VSS	VDD2P5	VDD3P0
XTAL	EXTAL	VDD1P8	VDD1P2
USB_OTG_ID	USB_OTG_RREFEXT	USB_OTG_GPANAIO	JTAG_TRSTB
USB_OTG_DP	USB_OTG_DN	USB_OTG_VBUS	JTAG_TDI
USB_H1_VDDA25	USB_OTG_VDDA25	USB_H1_VBUS	USB_H1_RREFEXT
USB_H1_DP	USB_H1_DN	DISP_WR	USB_H1_GPANAIO
USB_OTG_VDDA33	USB_H1_VDDA33	DISP_D0	DISP_BUSY
DISP_RS	DISP_D2	DISP_RD	DISP_D6
DISP_D4	DISP_D3	DISP_D7	DISP_D5
SD3_CLK	DISP_D11	DISP_D12	DISP_D14
DISP_D15	DISP_D8	DISP_D9	SD3_D3
DISP_D10	SD3_WP	SD3_D1	SD3_CMD
SD3_D0	SD3_D4	SD3_D6	SD3_D5
DRAM_D17	DRAM_D21	DRAM_A3	DRAM_A2
DRAM_D16	DRAM_D19	DRAM_D18	DRAM_D23
NC	DRAM_D20	DRAM_D22	DRAM_DQM2

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
ECSPI1_SCLK	N1	M4	N2	NVCC_SPI	HVIO	ALT1	IN	Keeper
ECSPI1_SS0	P7	L4	N3	NVCC_SPI	HVIO	ALT1	IN	Keeper
ECSPI2_MISO	N5	L2	L4	NVCC_SPI	HVIO	ALT1	IN	Keeper
ECSPI2_MOSI	P5	K2	N1	NVCC_SPI	HVIO	ALT1	IN	Keeper
ECSPI2_SCLK	P4	L1	N4	NVCC_SPI	HVIO	ALT1	IN	Keeper
ECSPI2_SS0	N4	K1	M2	NVCC_SPI	HVIO	ALT1	IN	Keeper
EIM_BCLK	A5	A12	A5	NVCC_EIM	HVIO	ALT0	OUT-LO	100K PU
EIM_CRE	A3	D13	A3	NVCC_EIM	HVIO	ALT0	OUT-LO	100K PU
EIM_CS0	B10	B24	B11	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU
EIM_CS1	D10	D17	C9	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU
EIM_CS2	E10	D16	D9	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU
EIM_DA0	A9	B23	B10	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA1	B9	C24	B9	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA10	D7	A14	C6	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA11	E7	B16	D6	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA12	A6	A16	A6	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA13	B6	A15	B6	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA14	D6	A13	C5	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA15	E6	B15	D5	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA2	D9	C23	C8	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA3	E9	A22	D8	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA4	A8	A23	A9	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA5	B8	B22	B8	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA6	D8	B18	C7	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA7	E8	B17	D7	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA8	A7	A18	A7	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_DA9	B7	A17	B7	NVCC_EIM	HVIO	ALT0	IN	100K PU
EIM_EB0	A4	D15	A4	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU
EIM_EB1	B4	D14	B4	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU
EIM_LBA	E5	B13	D4	NVCC_EIM	HVIO	ALT0	OUT-HI	100K PU