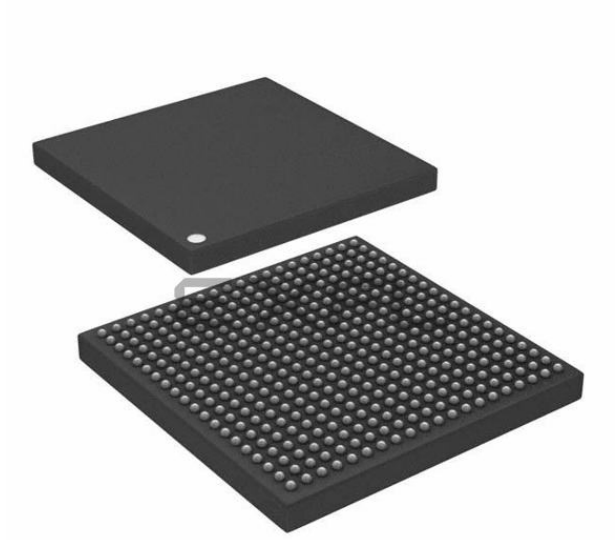

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Boot Security, Cryptography, Secure JTAG
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx503cvm8br2

Table 5. Special Signal Considerations (continued)

Signal Name	Remarks
DRAM_OPEN, DRAM_OPENFB (for 416 MAPBGA and 400 MAPBGA)	These pins are the echo gating output and feedback pins used by the DRAM PHY to bound a window around the DQS transition. For an application using a single DRAM device, these pins should be routed so that the trace length (DRAM_OPEN + DRAM_OPENFB) = trace length (DRAM_SDCLK0 + DRAM_SDQS0). For an application using two DRAM devices, they should be routed so that the trace length (DRAM_OPEN + DRAM_OPENFB) = trace length (AVG(DRAM_SDCLK0+DRAM_SDCLK1) + AVG (DRAM_SDQS0_to_Device0 + DRAM_SDQS0_to_Device1)). This connection is required for LPDDR1, LPDDR2, and DDR2. For the i.MX50 PoP package, these signals are connected on the substrate.
DRAM_SDODT0 (for 416 MAPBGA and 400 MAPBGA), DRAM_SDODT1 (for 416 MAPBGA only)	These pins are the On-die termination outputs from the i.MX50. For DDR2, these pins should be connected to the DDR2 DRAM ODT pins. For LPDDR1 and LPDDR2, these pins should be left floating. Note that both SDODT pins are removed on the 416 PoPBGA package, and only SDODT0 exists on the 400 MAPBGA package.
DRAM_CALIBRATION	This pin is the ZQ calibration used to calibrate DRAM Ron and ODT. For LPDDR2, this pin should be connected to ground through a 240 Ω 1% resistor. For DDR2 and LPDDR1, this pin should be connected to ground through a 300 Ω 1% resistor.
JTAG_MOD	This input has an internal 100K pull-up, by default. Note that JTAG_MOD is referenced as SJC_MOD in the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM) - both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. If JTAG port is not needed, the internal pull-up can be disabled in order to reduce supply current to the pin.
JTAG_TCK	This input has an internal 100K pull-down. This pin is in the NVCC_JTAG domain.
JTAG_TDI	This input has an internal 47K pull-up to NVCC_JTAG. This pin is in the NVCC_JTAG domain.
JTAG_TDO	This is a 3-state output with an internal gate keeper enable to prevent a floating condition. An external pull-up or pull-down resistor on JTAG_TDO is detrimental and should be avoided. This pin is in the NVCC_JTAG domain.
JTAG_TMS	This input has an internal 47K pull-up to NVCC_JTAG. This pin is in the NVCC_JTAG domain.
JTAG_TRSTB	This input has an internal 47K pull-up to NVCC_JTAG. This pin is in the NVCC_JTAG domain.
NC	These signals are No Connect (NC) and should be floated by the user.
LOW_BATT_GPIO	If the LOW_BATT_GPIO (UART4_TXD) is asserted at power up, the i.MX50 will boot up at a lower ARM clock frequency to reduce system power. The actual ARM clock frequency used when LOW_BATT_GPIO is asserted is determined by the BT_LPB_FREQ[1:0] pins (220 MHz to 55.3 MHz). The polarity of the LOW_BATT_GPIO is active high by default, but may be set to active low by setting the LOW_BATT_GPIO_LEVEL OTP bit. See the “System Boot” chapter of the Reference Manual for more details. Note that this is not a dedicated pin: LOW_BATT_GPIO appears on the UART4_TXD pin.
PMIC_STBY_REQ	This output may be driven high when the i.MX50 enters the STOP mode to notify the PMIC to enter its low power standby state. This output is in the NVCC_SRTC domain.
PMIC_ON_REQ	This output from the i.MX50 can instruct the PMIC to turn on when the i.MX50 only has NVCC_SRTC power. This may be useful for an alarm application, as it allows the i.MX50 to turn off all blocks except for the RTC and then power on again at a specified time. This output is in the NVCC_SRTC domain.

Table 5. Special Signal Considerations (continued)

Signal Name	Remarks
PMIC_RDY	This input may be used by a PMIC to signal to the i.MX50 that the PMIC supply outputs are at operating levels when resuming from STOP mode. The PMIC_RDY input is pin muxed on ALT3 of the I2C3_SCL pin and is in the NVCC_MISC domain.
POP_EMMC_RST (416 PoPBGA Only)	This pin is the PoP eMMC 4.4 Reset pin. The customer may connect this on their PCB to any free GPIO, or just leave floating for non-4.4 eMMC. This pin does not connect to the i.MX50 die.
POP_LPDDR2_ZQ0/ZQ1 (416 PoPBGA Only)	These pins connect to the PoP LPDDR2 DRAM ZQ pins and should be connected on the customer PCB to a 240 Ω 1% resistor to ground if used. These pins do not connect to the i.MX50 die.
POP_LPDDR2_1.8V (416 PoPBGA Only)	These pins are the 1.8 V supply for the PoP LPDDR2 DRAM. These pins do not connect to the i.MX50 die.
POP_NAND_VCC (416 PoPBGA Only)	This is the 3.3V I/O and memory supply for the PoP eMMC. Note that most eMMC can operate with a 1.8V I/O or a 3.3V I/O voltage. However, because we tied the eMMC memory and I/O domains together, you can't use the 1.8 V I/O option for the PoP eMMC, only 3.3 V I/O.
POR_B	This POWER-ON RESET input is a cold reset negative logic input that resets all modules and logic in the IC. The POR_B pin should have an external 68 K pull-up to NVCC_RESET and a 1 μF capacitor to ground. **Note:** The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail is at its working voltage.
RESET_IN_B	This warm reset negative logic input resets all modules and logic except for the following: • Test logic (JTAG, IOMUXC, DAP) • SRTC • Cold reset logic of WDOG—Some WDOG logic is only reset by POR_B. See WDOG chapter in the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM) for details.
SSI_EXT1_CLK, SSI_EXT2_CLK	The SSI_EXT1_CLK and SSI_EXT2_CLK outputs are recommended for generating a clock output from the i.MX50. Use of the CKO1 and CKO2 clock outputs is not recommended, as the large number of combinational logic muxes on those signals will impact jitter and duty-cycle. Note that these two clock outputs do not have dedicated pins: SSI_EXT1_CLK is IOMUX ALT3 on the OWIRE pin, and SSI_EXT2_CLK is IOMUX ALT3 of the EPITO pin.
TEST_MODE	TEST_MODE is for Freescale factory use only. This signal is internally connected to an on-chip pull-down device. The user must either float this signal or tie it to GND.
USB_H1_GPANAIO, USB_OTG_GPANAIO	These signals are reserved for Freescale manufacturing use only. Users should float these outputs.
USB_H1_RREFEXT, USB_OTG_RREFEXT	These signals determine the reference current for the USB PHY bandgap reference. An external 6.04 kΩ 1% resistor to GND is required. This resistor should be connected through a short (low impedance connection) and placed away from other noisy regions. If USB_H1 is not used, the H1 RREFEXT resistor may be eliminated and the pin left floating. If USB_OTG is not used, the OTG RREFEXT resistor may be eliminated and the pin left floating.

4.1 Chip-Level Conditions

This section provides the chip-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX50 Chip-Level Conditions

For these characteristics, see	Topic appears ...
Absolute Maximum Ratings	on page 21
13 x 13 mm MAPBGA Package Thermal Resistance Data	on page 22
13 x 13 mm PoPBGA Package Thermal Resistance Data	on page 23
17 x 17 mm MAPBGA Package Thermal Resistance Data	on page 23
Operating Ranges	on page 24
Operating Frequencies	on page 26
Supply Current	on page 26

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 7 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Table 11 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 7. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Peripheral core supply voltage	VCC	–0.3	1.5	V
ARM core supply voltage	VDDGP	–0.3	1.35	V
Bandgap and 480 MHz PLL supply	VDD3P0	–0.5	3.6	V
PLL digital supplies	VDD1P2	–0.3	1.35	V
PLL analog supplies	VDD1P8	–0.3	2.25	V
Efuse, 24 MHz oscillator, 32 kHz oscillator mux supply	VDD2P5	–0.5	2.85	V
Memory array supply	VDDA/VDDAL1	–0.5	1.35	V
Supply voltage (HVIO)	Supplies denoted as I/O supply	–0.5	3.6	V
Supply voltage (GPIO, LVIO)	Supplies denoted as I/O supply	–0.5	3.3	V
Input/output voltage range	V_{in}/V_{out}	–0.5	OVDD + 0.3[1]	V
USB VBUS DC Transient (t<30ms, duty cycle < 0.05%)	VBUS	 — —	 6.00 7.00	V

Table 15. Maximum Supply Current Consumption—ARM CLK = 1 GHz

Condition	Supply	Voltage (V)	Current (mA)	Power (mW)
• T_a = 70°C • ARM core in Run mode • ARM CLK = 1GHz • SYS CLK = 266 MHz • AHB CLK = 133 MHz • DDR CLK = 266 MHz • All voltages operating at maximum levels • External (MHz) crystal and on-chip oscillator enabled • All modules enabled	VDDGP	1.35	1000	1350
	VCC	1.275	220	280.5
	VDDA/VDDAL1	1.35	40	54
	VDD1P2	1.3	15	19.5
	VDD1P8	1.95	3	5.9
	VDD2P5[1]	2.75	2	5.5
	VDD3P0	3.3	2	6.6
	NVCC_EMI_DRAM	1.95	8.3	16.17
	VDD_DCDCi	1.95	0.021	0.041
	USB_OTG_VDDA33 + USB_H1_VDDA33	3.6	10.8	38.8
	VDDO25 + USB_OTG_VDDA25 + USB_H1_VDDA25	2.75	12.45	34.239
	NVCC_RESET	3.1	0.226	0.701
	NVCC_SRTC	1.3	0.0035	0.0045
	Total	—	—	1812

1 During eFuse programming, the maximum current on VDD2P5 will exceed these values. See Table 13 on page 26 for the maximum VDD2P5 current during eFuse programming.

Table 16. Stop Mode Current and Power Consumption [1]

Supply	Voltage (V)	Current (mA)	
		Typical, T_a = 25°C	Max, T_a = 25°C
VDDGP	0.85	0.057	0.198
VCC	0.95	0.544	1.890
VDDA/VDDAL1	0.95	0.071	0.247

1 The typical power, at Ta = 25°C, will be < 1 mW, including all supplies. Total max power, at Ta=25°C, will not exceed 2.5 mW, including all supplies.

4.1.5.1 Conditions for Stop Mode Current and Power Consumption

- ARM core in STOP mode and power gated
- VDDGP, VCC, and VDDA/VDDAL1 voltages at suspend levels
- VDD3P0, VDD2P5, VDD1P8, and VDD1P2 powered off
- USB_VDDA25 and USB_VDDA33 powered off

4.5 I/O AC Parameters

The load circuit and output transition time waveforms are shown in Figure 4 and Figure 5. The AC electrical characteristics for slow and fast I/O are presented in the Table 27 and Table 28, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bit in the IOMUX control registers.

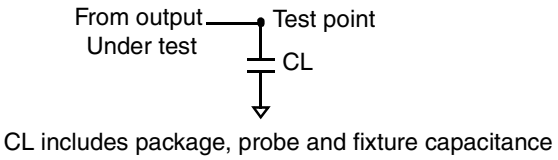

Figure 4. Load Circuit for Output

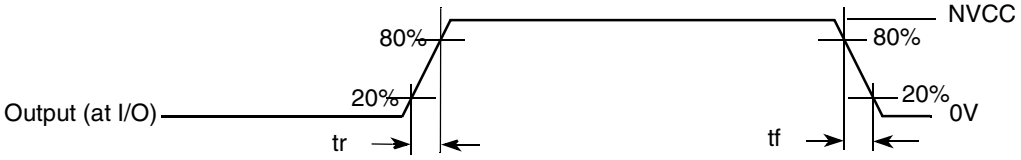

Figure 5. Output Transition Time Waveform

4.5.1 GPIO I/O Slow AC Parameters

Table 27 shows the AC parameters for GPIO slow I/O.

Table 27. GPIO I/O Slow AC Parameters

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF			1.91/1.52 3.07/2.65	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF			2.22/1.81 3.81/3.42	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF			2.88/2.42 5.43/5.02	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF			4.94/4.50 10.55/9.70	ns
Output Pad Slew Rate (Max Drive)[1]	tps	15 pF 35 pF	0.5/0.65 0.32/0.37			V/ns
Output Pad Slew Rate (High Drive)	tps	15 pF 35 pF	0.43/0.54 0.26/0.41			V/ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0.34/0.41 0.18/0.2			V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0.20/0.22 0.09/0.1			V/ns
Output Pad di/dt (Max Drive)	tdit				30	mA/ns

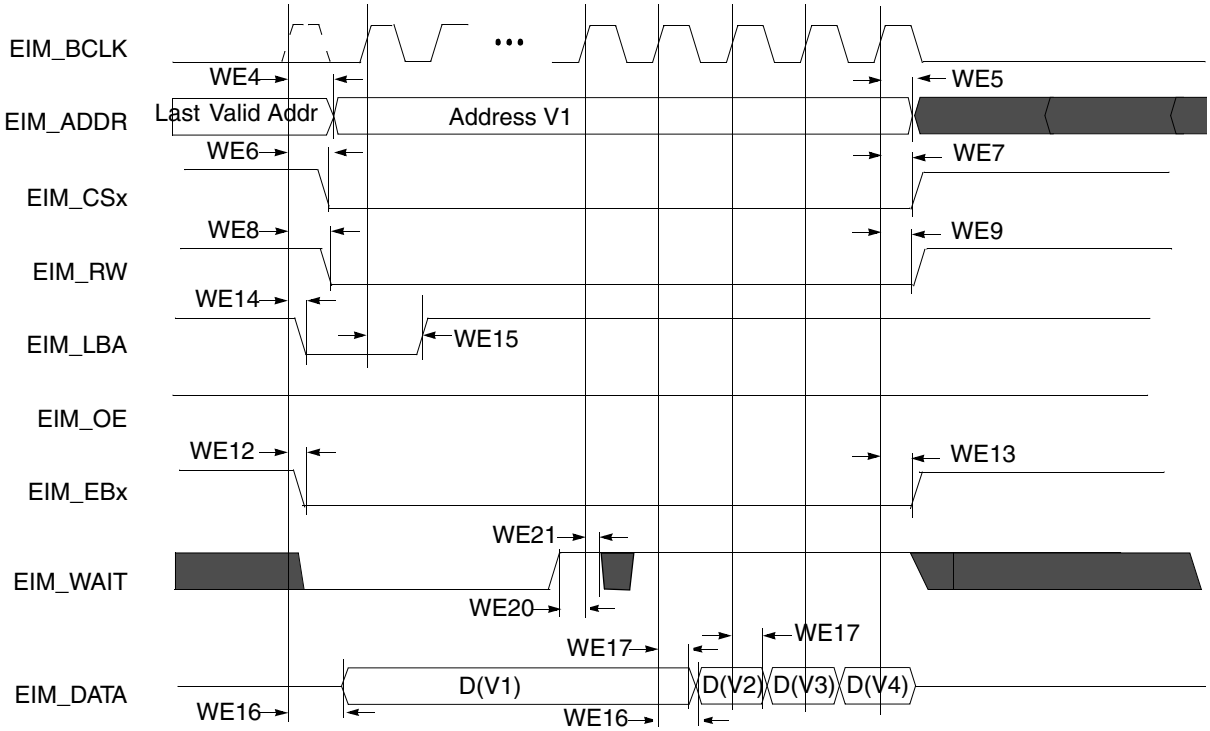

Figure 22. Synchronous Memory, Burst Write, BCS=1, WSC=4, SRD=1, and BCD=0

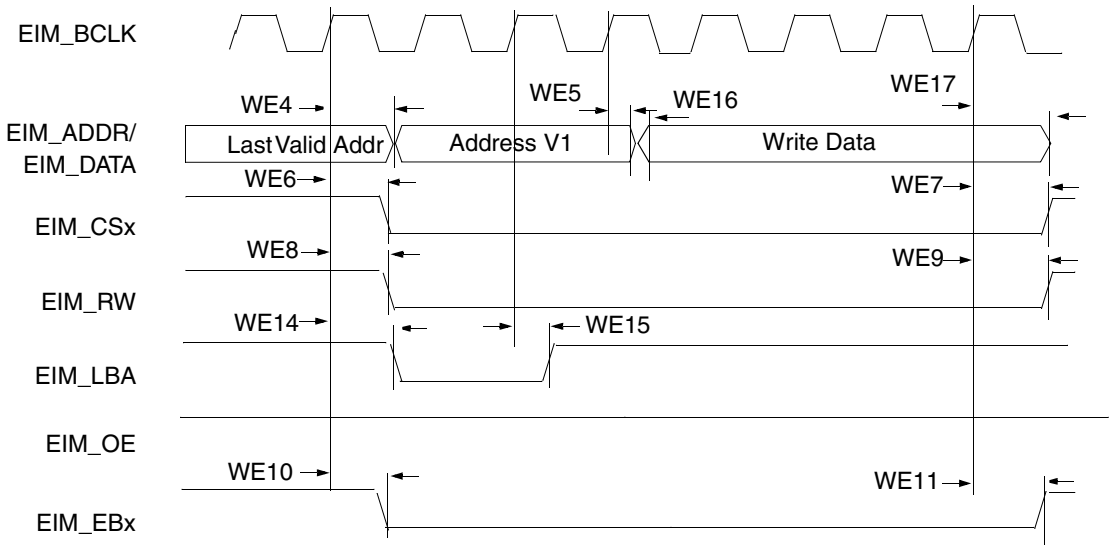

Figure 23. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6, ADVA=1, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode, the 16 MSBs are driven on the data bus.

Table 44. EIM Asynchronous Timing Parameters Table Relative Chip Select (continued)

ID	Parameter	Determination by Synchronous Measured Parameters [1]	Min	Max	Unit
WE34	EIM_RW invalid to EIM_CSx invalid	WE7 – WE9 + (WEN – CSN)	—	3 – (WEN_CSN)	ns
WE35	EIM_CSx valid to EIM_OE valid	WE10 – WE6 + (OEA – CSA)	—	3 + (OEA – CSA)	ns
WE36	EIM_OE invalid to EIM_CSx invalid	WE7 – WE11 + (OEN – CSN)	—	3 – (OEN – CSN)	ns
WE37	EIM_CSx valid to EIM_EBx valid (Read access)	WE12 – WE6 + (RBEA – CSA)	—	3 + (RBEA[4] – CSA)	ns
WE38	EIM_EBx invalid to EIM_CSx invalid (Read access)	WE7 – WE13 + (RBEN – CSN)	—	3 – (RBEN[5] – CSN)	ns
WE39	EIM_CSx valid to EIM_LBA valid	WE14 – WE6 + (ADV – CSA)	—	3 + (ADVA – CSA)	ns
WE40	EIM_LBA invalid to EIM_CSx invalid (ADVL is asserted)	WE7 – WE15 – CSN	—	3 – CSN	ns
WE41	EIM_CSx valid to Output Data valid	WE16 – WE6 – WCSA	—	3 – WCSA	ns
WE42	Output Data invalid to EIM_CSx invalid	WE17 – WE7 – CSN	—	3 – CSN	ns
WE43	Input Data valid to EIM_CSx invalid	MAXCO + MAXDI	MAXCO[6] + MAXDI[7]	—	ns
WE44	EIM_CSx invalid to Input Data invalid	0	0	—	ns
WE45	EIM_CSx valid to EIM_EBx valid (Write access)	WE12 – WE6 + (WBEA – CSA)	—	3 + (WBEA – CSA)	ns
WE46	EIM_EBx invalid to EIM_CSx invalid (Write access)	WE7 – WE13 + (WBEN – CSN)	—	–3 + (WBEN – CSN)	ns
WE47	EIM_DTACK valid to EIM_CSx invalid	MAXCO + MAXDTI	MAXCO[6] + MAXDTI[8]	—	ns
WE48	EIM_CSx invalid to EIM_DTACK invalid	0	0	—	ns

1 Parameters WE4–WE21 value, see in the Table 44.

2 EIM_CSx Assertion. This bit field determines when EIM_CSx signal is asserted during read/write cycles.

3 EIM_CSx Negation. This bit field determines when EIM_CSx signal is negated during read/write cycles.

4 EIM_EBx Assertion. This bit field determines when EIM_EBx signal is asserted during read cycles.

5 EIM_EBx Negation. This bit field determines when EIM_EBx signal is negated during read cycles.

6 Output maximum delay from internal driving the FFs to chip outputs. The maximum delay between all memory controls (EIM_ADDR, EIM_CSx, EIM_OE, EIM_RW, EIM_EBx, and EIM_LBA).

7 Maximum delay from chip input data to internal FFs. The maximum delay between all data input pins.

8 DTACK maximum delay from chip input data to internal FF.

4.8 DRAM Timing Parameters

This section includes descriptions of the electrical specifications of DRAM MC module which interfaces external DDR2, LPDDR1, and LPDDR2 memory devices.

NOTE

DDR6 and DDR7 can be adjusted by the parameter -DLL_WR_DELAY-;

The ideal case is that SDCLK is center aligned to the DRAM_A[9:0] data valid window;

For this table, HW_DRAM_PHY23[14:8] (DLL_WR_DELAY) = 0x10;

4.8.3 DRAM Data Output Timing

The DRAM data output timing is defined for all DDR types: DDR2, LPDDR1, and LPDDR2.

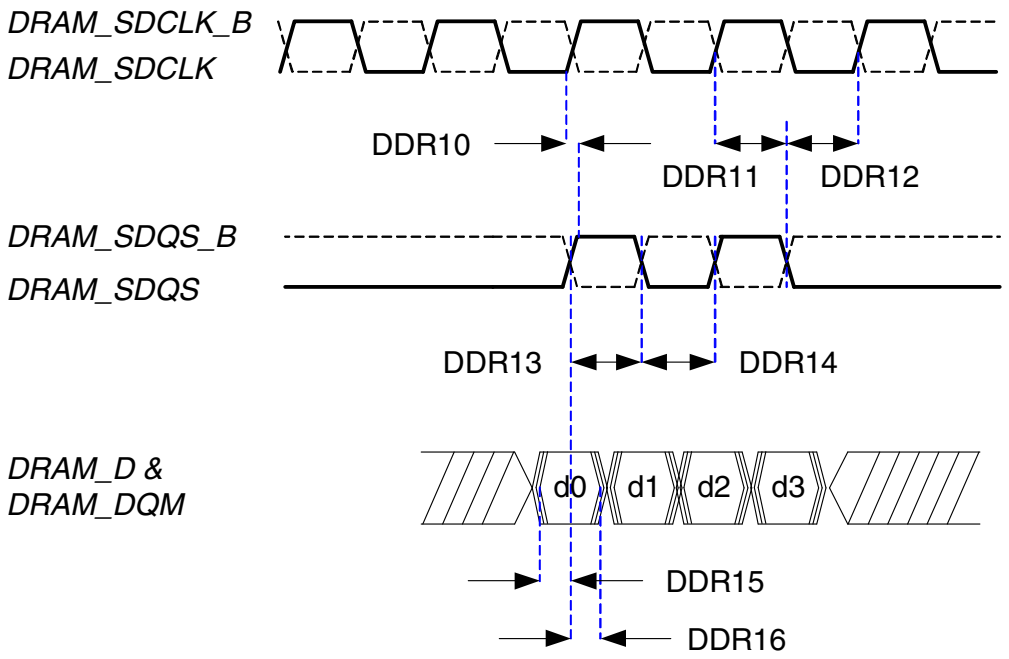

Figure 30. DRAM Data Output Timing

Table 47. DDR Output AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR10	Positive DQS latching edge to associated CK edge	tDQSS	-0.3	0.3	ns
DDR11	DQS falling edge from CK rising edge—hold time	tDSH	0.5 tCK - 0.3	0.5 tCK + 0.3	ns
DDR12	DQS falling edge to CK rising edge—setup time	tDSS	0.5 tCK - 0.3	0.5 tCK + 0.3	ns
DDR13	DQS output high pulse width	tDQSH	0.48 tCK	0.52 tCK	ns
DDR14	DQS output low pulse width	tDQSL	0.48 tCK	0.52 tCK	ns
DDR15 CK >= 200 MHz	DQ & DQM output setup time relative to DQS	tDS	0.5 tCK - 1.3	—	ns

4.9.3 Enhanced Secured Digital Host Controller (eSDHCv2/v3) and uSDHC AC Timing

This section describes the electrical information of the eSDHCv2/v3 and the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4 (Dual Date Rate) timing.

4.9.3.1 SD/eMMC4.3 (Single Data Rate) eSDHCv3 and uSDHC AC Timing

Figure 36 depicts the timing of SD/eMMC4.3, and Table 54 lists the SD/eMMC4.3 timing characteristics.

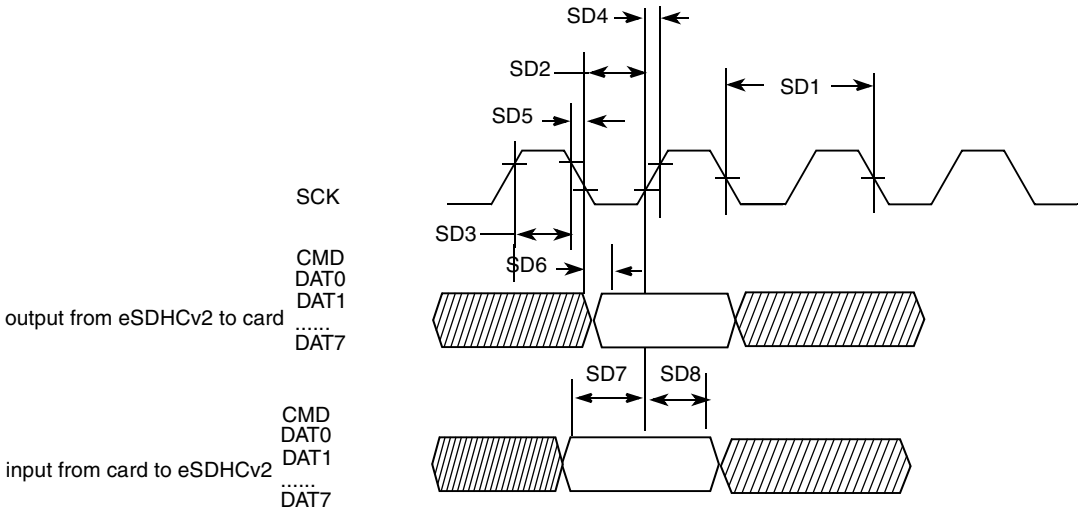

Figure 36. SD/eMMC4.3 Timing

Table 54. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns

Table 59. I²C Module Timing Parameters (continued)

ID	Parameter	Standard Mode Supply Voltage = 1.65 V–1.95 V, 2.7 V–3.3 V		Fast Mode Supply Voltage = 2.7 V–3.3 V		Unit
		Min	Max	Min	Max	
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal.

3 A Fast-mode I²C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2CLK line is released.

4 C_b = total capacitance of one bus line in pF.

4.9.6 One-Wire (OWIRE) Timing Parameters

Figure 42 depicts the RPP timing, and Table 60 lists the RPP timing parameters.

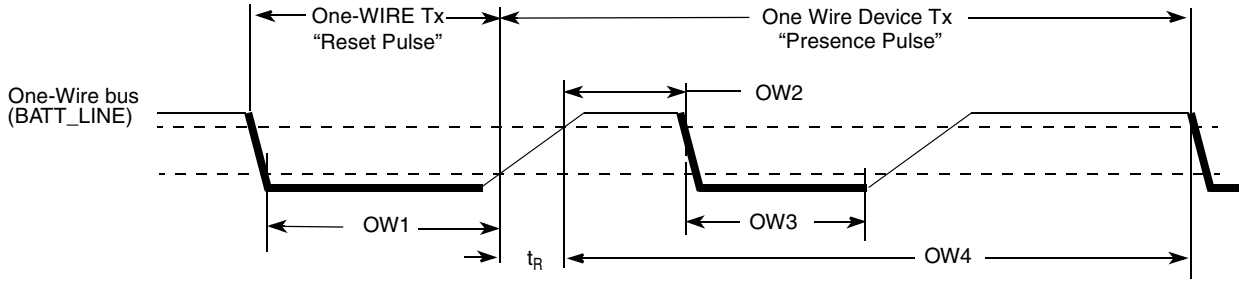

Figure 42. Reset and Presence Pulses (RPP) Timing Diagram

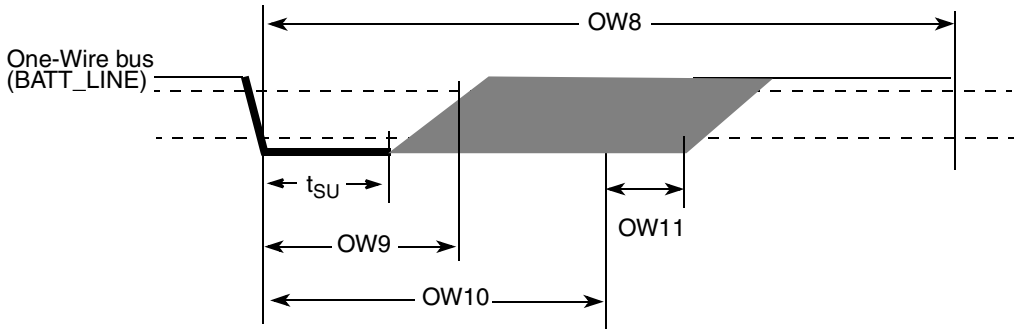

Figure 45. Read Sequence Timing Diagram

Table 62. WR1 /RD Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Unit
OW7	Write 1 Low Time	t_{LOW1}	1	5	15	µs
OW8	Transmission Time Slot	t_{SLOT}	60	117	120	µs
—	Read Data Setup	t_{SU}	—	—	1	µs
OW9	Read Low Time	t_{LOWR}	1	5	15	µs
OW10	Read Data Valid	t_{RDV}	—	15	—	µs
OW11	Release Time	$t_{RELEASE}$	0	—	45	µs

4.9.7 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 46 depicts the timing of the PWM, and Table 63 lists the PWM timing parameters.

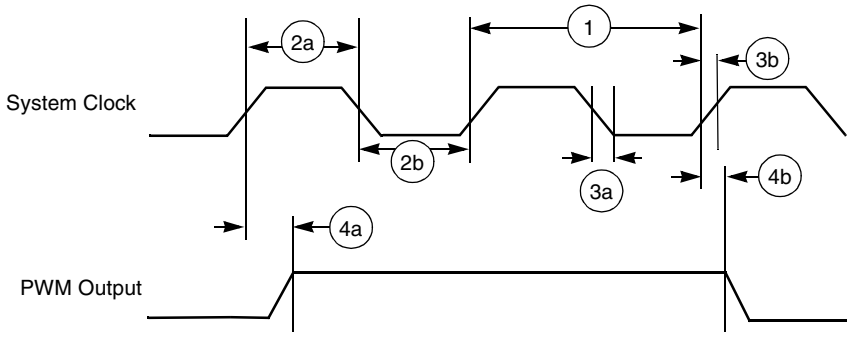

Figure 46. PWM Timing

Table 67. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS as shown in both the tables and figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- **Tx** and **Rx** refer to the transmit and receive sections of the SSI.
- The terms WL and BL refer to word length (WL) and bit length (BL).
- For internal frame sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

Table 79. 416 MAPBGA 13x13 mm, 0.5 mm Pitch Ball Map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
AB	BOOT_MODE0	BOOT_MODE1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	DRAM_SDQS2	DRAM_SDQS2_B	AB
AC	RESET_IN_B	TEST_MODE	GND3P0	GND2P5	EXTAL	GND1P2	GND1P8	USB_OTG_DN	USB_OTG_VDDA25_1	USB_H1_DN	USB_H1_VDDA33	DISP_BUSY	DISP_RS	DISP_RESET	SD3_D0	SD3_D1	SD3_D2	VSS	DRAM_D16	DRAM_D18	NVCC_EMI_DRAM	DRAM_D20	DRAM_D22	DRAM_DQM2	AC
AD	VSS	POR_B	VDD3P0	VDD2P5	XTAL	VDD1P2	VDD1P8	USB_OTG_DP	USB_H1_VDDA25_1	USB_H1_DP	USB_OTG_VDDA33	DISP_WR	DISP_RD	DISP_CS	SD3_WP	SD3_CLK	SD3_CMD	VSS	DRAM_D17	DRAM_D19	NVCC_EMI_DRAM	DRAM_D21	DRAM_D23	VSS	AD

5.1.3 416 MAPBGA 13 x 13 Power Rails

Table 80. 416 MAPBGA 13x13 Ground, Power, Sense, and Reference Contact Signals

Pin Name	Ball Number	Comments
GND_DCDC	W5	—
NVCC_EIM	L7, M7, M8	—
NVCC_EMI_DRAM	A21, AA21, AA23, AA24, AC21, AD21, B21, D21, D23, D24, K21, K23, K24, R21, R23, R24	—
NVCC_EPDC	M10, N10, P10, R10, U10	—
NVCC_JTAG	U9	—
NVCC_KEYPAD	N8	—
NVCC_LCD	U11	—
NVCC_MISC	P8	—
NVCC_NANDF	V9, V10	—
NVCC_RESET	V8	—
NVCC_SD1	T7	—
NVCC_SD2	U8	—
NVCC_SPI	R7	—

Table 80. 416 MAPBGA 13x13 Ground, Power, Sense, and Reference Contact Signals (continued)

NVCC_SRTC	AA1	—
NVCC_SSI	R8	—
NVCC_UART	T8	—
USB_H1_VDDA25	AD9	Note that on the 416 MAPBGA package, USB_OTG_VDDA25 and USB_H1_VDDA25 are shorted together on the substrate.
USB_H1_VDDA33	AC11	Note that on the 416 MAPBGA package, USB_OTG_VDDA33 and USB_H1_VDDA33 are shorted together on the substrate.
USB_OTG_VDDA25	AC9	Note that on the 416 MAPBGA package, USB_OTG_VDDA25 and USB_H1_VDDA25 are shorted together on the substrate.
USB_OTG_VDDA33	AD11	Note that on the 416 MAPBGA package, USB_OTG_VDDA33 and USB_H1_VDDA33 are shorted together on the substrate.
VCC	H14, H15, H16, H17, J17, K14, K15, K17, L15	—
VDD_DCDCI	Y6	—
VDD_DCDCO	Y5	—
VDD1P2	AD6	—
VDD1P8	AD7	—
VDD2P5	AD4	—
VDD3P0	AD3	—
VDDA	P17, R17	—
VDDAL1	P15, R15	—
VDDGP	G10, G8, G9, H10, H11, H8, H9, J8, K10, K11, K7, K8, L10, L11, L8	—
VDDO25	N23	—
VSS	A1, A18, A24, AA11, AA2, AA9, AC18, AC3, AC4, AC6, AC7, AD1, AD18, AD24, B18, G20, G21, G23, H12, H13, K12, K13, L12, L13, L14, L17, M11, M14, M15, M17, M18, M20, M21, N11, N14, N15, N17, P11, P12, P13, P14, R11, R12, R13, R14, T17, T18, U12, U13, U14, U15, U16, U17, U18, V17, V18, V20, V21, V23	—

Table 81. 416 PoPBGA 13 x 13 mm Ball Map (continued)

AA	NVCC_SRTC	VSS	NC	JTAG_TDI	JTAG_TRSTB	CKIH	GND_KEL	USB_OTG_RREFEXT	VSS	USB_H1_RREFEXT	VSS	USB_OTG_ID	USB_OTG_VBUS	USB_OTG_GPANAIO	CHGR_DET_B	USB_H1_VBUS	USB_H1_GPANAIO	VSS	DISP_RESET	DISP_RD	DISP_BUSY	NC	POP_LPDDR2_ZQ1	POP_LPDDR2_ZQ0
AB	BOOT_MODE0	BOOT_MODE1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	DISP_D14	DISP_D5
AC	RESET_IN_B	TEST_MODE	VSS	VSS	EXTAL	VSS	VSS	USB_OTG_DN	USB_VDDA25	USB_H1_DN	USB_VDDA33	SSI_TXFS	SSI_TXC	SSI_RXD	DISP_D3	DISP_D1	DISP_D0	VSS	DISP_D7	DISP_D9	DISP_CS	DISP_D12	DISP_D13	DISP_D4
AD	VSS	POR_B	VDD3P0	VDD2P5	XTAL	VDD1P2	VDD1P8	USB_OTG_DP	USB_VDDA25	USB_H1_DP	USB_VDDA33	SSI_RXC	SSI_RXFS	SSI_TXD	DISP_D2	DISP_D6	DISP_	VSS	DISP_D11	DISP_WR	DISP_D15	DISP_D10	DISP_RS	VSS

5.2.3 416 PoPBGA 13 x 13 mm Power Rails

Table 82 shows the device connection list for ground, power, sense, and reference contact signals. Table 85 displays an alpha-sorted list of the signal assignments including power rails and associated power supplies.

Table 82. 416 PoPBGA 13 x 13 mm Ground, Power, Sense, and Reference Contact Signals

Pin Name	Ball Number	Comments
GND_DCDC	W5	—
NVCC_EIM	N7 M7 M8	—
NVCC_EMI_DRAM	A21, B21, D21, D23, D24, E5, E6, E7, F5, G5, G7, K20, L20, M20, N20, P20, R20, V18, V20, W20, Y18, Y19, Y20	These are the 1.2V supply to both the i.MX50 DRAM controller as well as the PoP LPDDR2.
NVCC_EPDC	M10, N10, P10, R10, U10	—
NVCC_JTAG	U9	—
NVCC_KEYPAD	N8	—
NVCC_LCD	U11	—
NVCC_MISC	P8	—
NVCC_NANDF	V9, V10	—

5.3.1 400 MAPBGA 17 x 17 mm Package Views

Figure 65 shows the top view of the 17 x 17 mm package, Figure 66 shows the bottom view of the package, and Figure 67 shows the side view of the package.

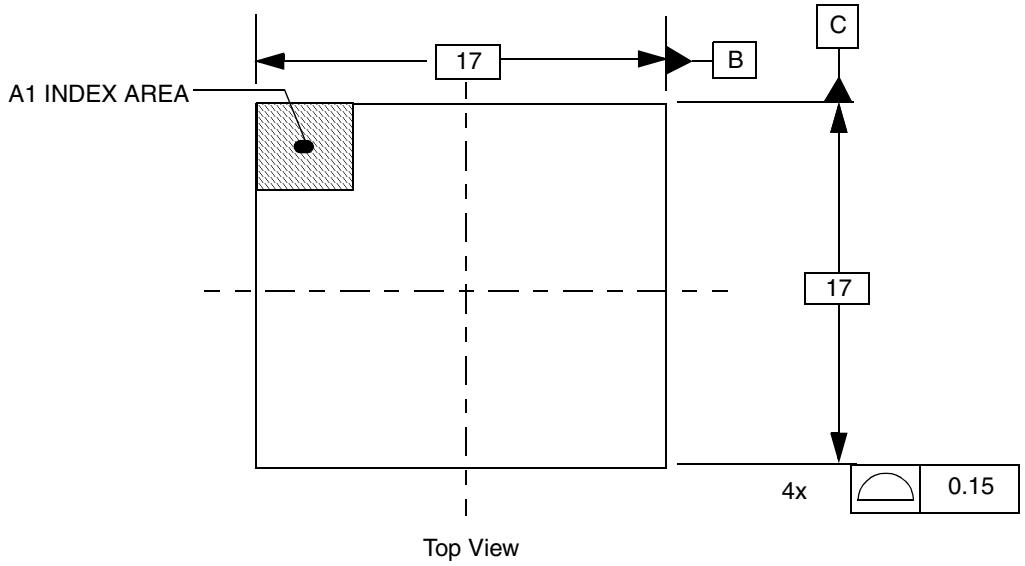

Figure 65. 400 MAPBGA 17x17 mm Package Top view

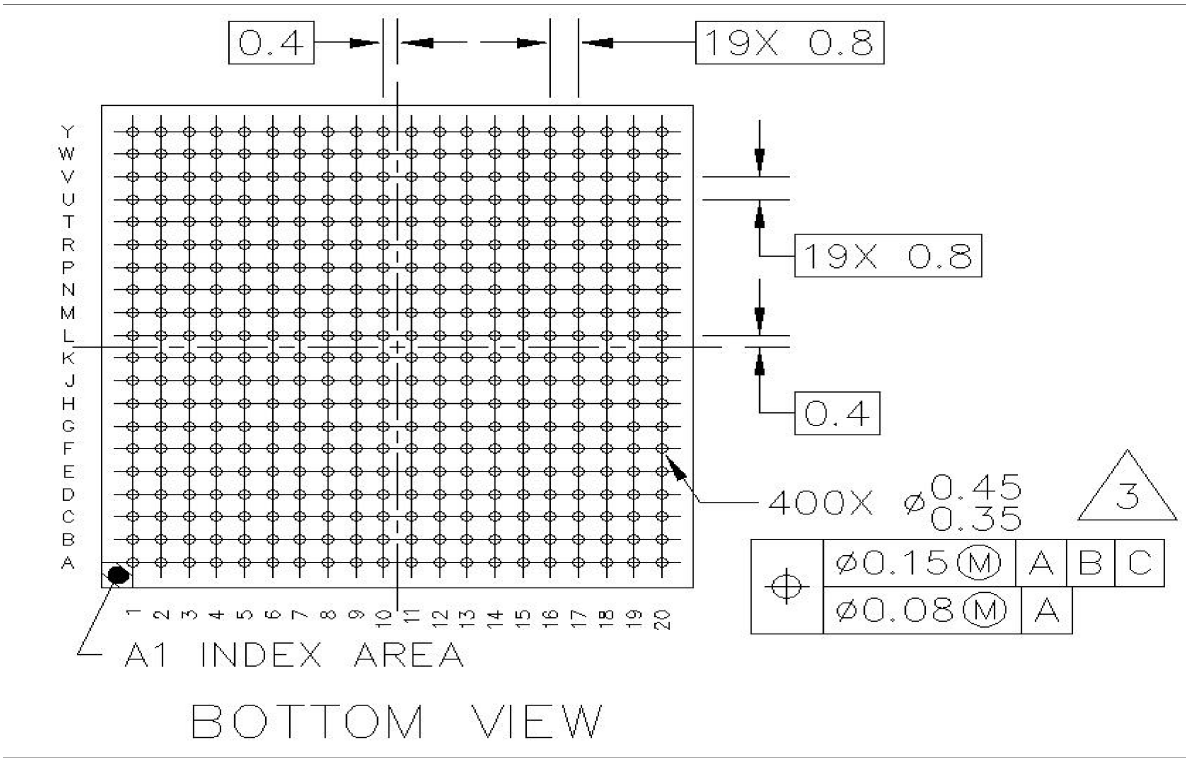

Figure 66. 400 MAPBGA 17x17 mm Package Bottom View

Table 84. 400 MAPBGA 17x17 Ground, Power, Sense, and Reference Contact Signals (continued)

VDD_DCDCI	R7
VDD_DCDCO	T6
GND_DCDC	R6

5.4 Signal Assignments

Table 85. Alphabetical List of Signal Assignments

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
BOOT_MODE0	AB1	AB1	V3	NVCC_RESET	LVIO	ALT0	IN	100K PU
BOOT_MODE1	AB2	AB2	U3	NVCC_RESET	LVIO	ALT0	IN	100K PU
CHGR_DET_B	V11	AA15	T10	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG25	—	OUT-OD	—
CKIH	AA6	AA6	V4	NVCC_JTAG	ANALOG	—	—	—
CKIL	Y1	Y1	Y4	NVCC_SRTC	ANALOG	—	—	—
CSPI_MISO	M5	H2	K4	NVCC_SPI	HVIO	ALT1	IN	Keeper
CSPI_MOSI	M2	J1	L3	NVCC_SPI	HVIO	ALT1	IN	Keeper
CSPI_SCLK	M1	H1	M1	NVCC_SPI	HVIO	ALT1	IN	Keeper
CSPI_SS0	M4	J2	J4	NVCC_SPI	HVIO	ALT1	IN	Keeper
DISP_BUSY	AC12	AA21	U11	NVCC_LCD	HVIO	ALT1	IN	Keeper
DISP_CS	AD14	AC21	T12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D0	AA12	AC17	V11	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D1	Y12	AC16	T11	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D10	Y17	AD22	Y16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D11	V12	AD19	W14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D12	V13	AC22	V14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D13	V14	AC23	T13	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D14	V15	AB23	U14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D15	V16	AD21	Y15	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D2	AA13	AD15	W12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D3	Y13	AC15	W13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D4	AA14	AC24	Y13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D5	Y14	AB24	U13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
EPDC_PWRCTRL2	G14	F23	E12	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_PWRCTRL3	G15	L21	F15	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_PWRSTAT	G16	F24	C12	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE0	D13	N24	B12	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE1	E13	P24	A12	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE2	D12	H21	C11	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE3	E12	J21	E8	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE4	D11	K21	D10	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE5	E11	D18	E6	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCLK	A13	K24	B13	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCLKN	B13	L24	D12	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDLE	D18	M24	C15	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDOE	E18	V21	C13	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDOED	D19	R23	G16	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDOEZ	E19	U21	F16	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDSHR	A10	H23	A8	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_VCOM0	G17	H24	B14	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_VCOM1	D20	W21	G15	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPITO	G4	D8	F5	NVCC_MISC	HVIO	ALT1	IN	Keeper
EXTAL	AC5	AC5	W6	VDD2P5	ANALOG	—	—	—
GND_KEL	AA7	AA7	T7	VDD2P5	ANALOG	—	—	—
I2C1_SCL	E1	A6	E1	NVCC_MISC	HVIO	ALT1	IN	Keeper
I2C1_SDA	E2	B7	E2	NVCC_MISC	HVIO	ALT1	IN	Keeper
I2C2_SCL	F1	A5	F1	NVCC_MISC	HVIO	ALT1	IN	Keeper
I2C2_SDA	F2	B6	F2	NVCC_MISC	HVIO	ALT1	IN	Keeper
I2C3_SCL	G1	A4	G1	NVCC_MISC	HVIO	ALT1	IN	Keeper
I2C3_SDA	G2	B5	G2	NVCC_MISC	HVIO	ALT1	IN	Keeper
JTAG_MOD	V7	V5	T8	NVCC_JTAG	GPIO	ALT0	IN	100K PU
JTAG_TCK	W4	W4	R8	NVCC_JTAG	GPIO	ALT0	IN	100K PD

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
SD2_D2	V1	F1	W2	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D3	V2	F2	T4	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D4	V4	G2	V2	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D5	U2	E2	U2	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D6	U4	H4	R4	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D7	U5	F4	W1	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_WP	T5	G4	T2	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD3_CLK	AD16	T1	Y14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_CMD	AD17	T2	U16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D0	AC15	V1	Y17	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D1	AC16	V2	V16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D2	AC17	R1	T16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D3	AA17	U2	U15	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D4	AA18	P1	W17	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D5	Y18	U1	U17	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D6	AA19	R2	V17	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D7	Y19	U4	T15	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_WP	AD15	T4	W16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SSI_RXC	J7	AD12	H4	NVCC_SSI	HVIO	ALT1	IN	Keeper
SSI_RXD	J5	AC14	F3	NVCC_SSI	HVIO	ALT1	IN	Keeper
SSI_RXFS	H7	AD13	G5	NVCC_SSI	HVIO	ALT1	IN	Keeper
SSI_TXC	J4	AC13	G3	NVCC_SSI	HVIO	ALT1	IN	Keeper
SSI_TXD	H5	AD14	G4	NVCC_SSI	HVIO	ALT1	IN	Keeper
SSI_TXFS	H4	AC12	H3	NVCC_SSI	HVIO	ALT1	IN	Keeper
TEST_MODE	AC2	AC2	U4	NVCC_RESET	LVIO	ALT0	IN	100K PD
UART1_CTS	H2	B4	J1	NVCC_UART	HVIO	ALT1	IN	Keeper
UART1_RTS	J2	B3	K2	NVCC_UART	HVIO	ALT1	IN	Keeper
UART1_RXD	J1	A2	K1	NVCC_UART	HVIO	ALT1	IN	Keeper
UART1_TXD	H1	A3	H1	NVCC_UART	HVIO	ALT1	IN	Keeper
UART2_CTS	K2	B2		NVCC_UART	HVIO	ALT1	IN	Keeper