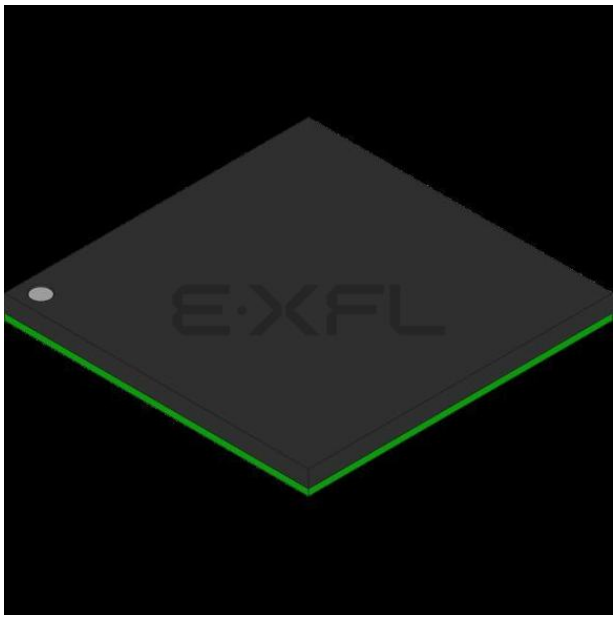

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3V
Operating Temperature	-20°C ~ 70°C (TA)
Security Features	Boot Security, Cryptography, Secure JTAG
Package / Case	400-LFBGA
Supplier Device Package	400-PBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx503evm8b

GPU2Dv1	Graphics Processing Unit-2D, ver. 1	Display Peripherals	The GPU2Dv1 provides hardware acceleration for 2D graphic algorithms with sufficient processor power to run desk-top quality interactive graphics applications on displays up to HD1080 resolution.
I^2C-1 I^2C-2 I^2C-3	I^2C Interface	Connectivity Peripherals	I^2C provides serial interface for controlling peripheral devices. Data rates of up to 400 kbps are supported.
OCOTP Controller	On-chip OTP controller	Security Peripherals	The on-chip one-time -programmable (OCOTP) ROM serves the functions of hardware and software capability bits, Freescale operations and unique-ID, the customer-programmable cryptography key, and storage of various ROM and general purpose configuration bits.
IOMUXC	IOMUX Control	Slave Connectivity Peripherals	This module enables flexible I/O multiplexing. Each I/O pad has default as well as several alternate functions. The alternate functions are software configurable.
KPP	Keypad Port	Slave Connectivity Peripherals	The KPP supports an 8×8 external keypad matrix. The KPP features are as follows: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
OWIRE	One-Wire Interface	Slave Connectivity Peripherals	

SDMA	Smart Direct Memory Access	Master Connectivity Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by offloading various cores in dynamic data routing. The SDMA features list is as follows: • Powered by a 16-bit instruction-set micro-RISC engine • Multi-channel DMA supports up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM Cortex-A8 and SDMA • Very fast context-switching with two-level priority-based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle uni-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers for EMI • Support of byte-swapping and CRC calculations • A library of scripts and API is available
SJC	Secure JTAG Controller	System Control Peripherals	The Secure JTAG Controller provides a mechanism for regulating JTAG

Table 7. Absolute Maximum Ratings (continued)

Parameter Description	Symbol	Min	Max	Unit
ESD damage immunity: Human Body Model (HBM) Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	V
Storage temperature range	$T_{STORAGE}$	–40	125	^{o}C

1 The term OVDD in this section refers to the associated supply rail of an input or output. The maximum range can be superseded by the DC tables.

4.1.2 Thermal Resistance Data

4.1.2.1 13 x 13 mm MAPBGA Package Thermal Resistance Data

Table 8 provides thermal resistance data for a 13 x 13 mm MAPBGA package.

Table 8. 13 x 13 mm MAPBGA Package Thermal Resistance Data

Rating	Board	Symbol	Value	Unit
Junction to Ambient (natural convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	51	°C/W
Junction to Ambient (natural convection)[1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	28	°C/W
Junction to Ambient (at 200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	40	°C/W
Junction to Ambient (at 200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	24	°C/W
Junction to Board[4]	—	$R_{\theta JB}$	14	°C/W
Junction to Case[5]	—	$R_{\theta JC}$	9	°C/W
Junction to Package Top (natural convection)[6]	—	Ψ_{JT}	2	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per JEDEC JESD51-2 with the single layer board horizontal. The thermal test board meets JESD51-9 specification.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by using the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 14 shows the maximum supply current consumption of the i.MX50 for PMIC specification purposes.

Table 14. Maximum Supply Current Consumption—ARM CLK = 800 MHz

Condition	Supply	Voltage (V)	Current (mA)	Power (mW)
• T_a = 70°C • ARM core in Run mode • ARM CLK = 800 MHz • SYS CLK = 266 MHz • AHB CLK = 133 MHz • DDR CLK = 266 MHz • All voltages operating at maximum levels • External (MHz) crystal and on-chip oscillator enabled • All modules enabled	VDDGP	1.15	628	723
	VCC	1.275	185	236
	VDDA/VDDAL1	1.275	40	51
	VDD1P2	1.3	5.92	7.70
	VDD1P8	1.95	1.53	2.99
	VDD2P5[1]	2.75	1.13	3.11
	VDD3P0	3.3	1.61	5.32
	NVCC_EMI_DRAM	1.95	8.3	16.17
	VDD_DCDCI	1.95	0.021	0.041
	USB_OTG_VDDA33 + USB_H1_VDDA33	3.6	10.8	38.8
	VDDO25 + USB_OTG_VDDA25 + USB_H1_VDDA25	2.75	12.45	34.239
	NVCC_RESET	3.1	0.226	0.701
	NVCC_SRTC	1.3	0.0035	0.0045
	Total	—	—	1120

1 During eFuse programming, the maximum current on VDD2P5 will exceed these values. See Table 13 on page 26 for the maximum VDD2P5 current during eFuse programming.

4.2.1 Power-Up Sequence

Figure 2 shows the power-up sequence.

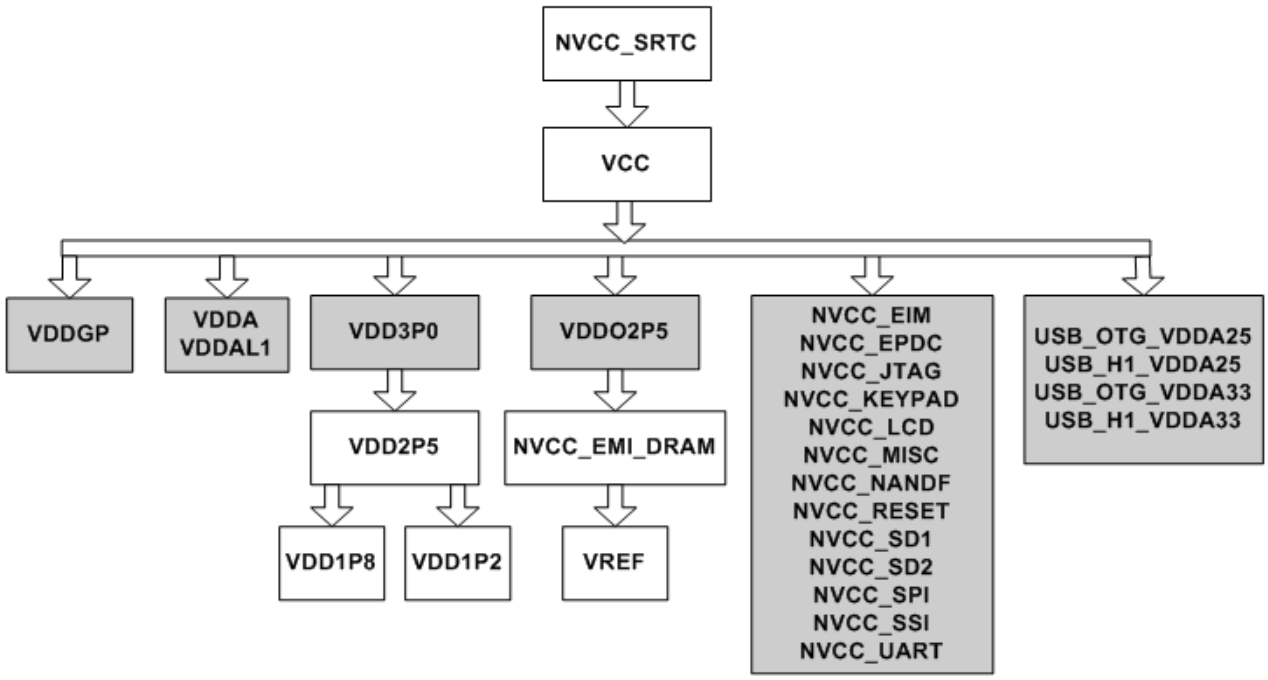

Figure 2. Power-Up Sequence

NOTE

1) The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail is at its working voltage.

2) No power-up sequence dependencies exist between the supplies shown shaded in gray.

4.2.2 Power-Down Sequence

The power-down sequence is recommended to be the opposite of the power-up sequence. In other words, the same power supply constraints exist while powering off as while powering on.

4.2.3 Resume Sequence

When the i.MX50 is resuming from STOP mode, there are some special sequencing considerations. The resume timing is determined by the following internal counters:

1. STBY_COUNT. This register is in the CCM block and may be set to a maximum of 16 x 32 kHz cycles, or 500 µsec.

4.4.3 HVIO Output Buffer Impedance

Table 26 shows the HVIO output buffer impedance of the i.MX50 processor.

Table 26. HVIO Output Buffer Impedance

Parameter	Symbol	Test Conditions	Min		Typ		Max		Unit
			OVDD 1.95 V	OVDD 3.3 V	OVDD 1.875 V	OVDD 3.30V	OVDD 1.65 V	OVDD 2.68 V	
Output driver impedance	Rpu	Low drive strength, Ztl = 150 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω	113.5 56.2 37.8	103.8 51.9 35.1	130.6 66 45.9	133 69.2 41	219.4 109.7 73.1	212.2 111.1 71.8	Ω
Output driver impedance	Rpd	Low drive strength, Ztl =1 50 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω	78.5 39.7 26.8	70 34.5 23	113.6 56.8 38.3	102 50 33.3	230.8 115.4 76.9	179.5 89.8 60.7	Ω

NOTE

Output driver impedance is measured with *long* transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 3).

Table 43. EIM Bus Timing Parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	EIM_BCLK Cycle time[2]	t	—	2t	—	3t	—	4t	—
WE2	EIM_BCLK Low Level Width	0.4t	—	0.8t	—	1.2t	—	1.6t	—
WE3	EIM_BCLK High Level Width	0.4t	—	0.8t	—	1.2t	—	1.6t	—
WE4	Clock rise to address valid[3]	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE5	Clock rise to address invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE6	Clock rise to EIM_CSx valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE7	Clock rise to EIM_CSx invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE8	Clock rise to EIM_RW valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE9	Clock rise to EIM_RW invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE10	Clock rise to EIM_OE valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE11	Clock rise to EIM_OE invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE12	Clock rise to EIM_EBx valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE13	Clock rise to EIM_EBx invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE14	Clock rise to EIM_LBA valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE15	Clock rise to EIM_LBA invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE16	Clock rise to Output Data valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	2t – 1.25	2t + 1.75
WE17	Clock rise to Output Data Invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	2t – 1.25	2t + 1.75
WE18	Input Data setup time to Clock rise	2	—	2	—	2	—	2	—
WE19	Input Data hold time from Clock rise	2.5	—	2.5	—	2.5	—	2.5	—
WE20	EIM_WAIT setup time to Clock rise	2	—	2	—	2	—	2	—
WE21	EIM_WAIT hold time from Clock rise	2.5	—	2.5	—	2.5	—	2.5	—

1 *t* is axi_clk cycle time. The maximum allowed axi_clk frequency is 133 MHz, whereas the maximum allowed EIM_BCLK frequency is 66.5 MHz. As a result, if BCD = 0, axi_clk must be ≤ 66.5 MHz. If BCD = 1, then 133 MHz is allowed for axi_clk, resulting in a EIM_BCLK of 66.5 MHz. When the clock branch to EIM is decreased to 66.5 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM) for a detailed clock tree description.

4.8.2 DRAM Command and Address Output Timing—LPDDR2

The following diagrams and tables specify the timings related to the address and command pins, which interface LPDDR2 memory devices.

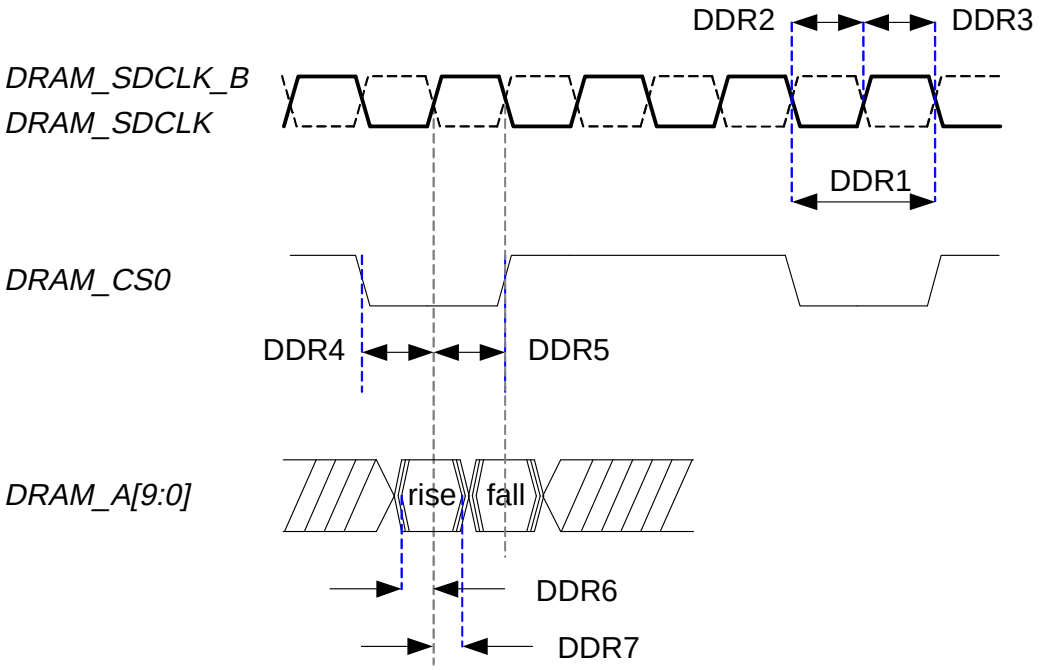

Figure 29. DRAM Command/Address Output Timing—LPDDR2

Table 46. EMI Command/Address AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR1	CK cycle time	tCK	3.75	—	ns
DDR2	CK high level width	tCH	0.48 tCK	0.52 tCK	ns
DDR3	CK low level width	tCL	0.48 tCK	0.52 tCK	ns
DDR4	Control output setup time	tIS	0.5 tCK - 0.3	—	ns
DDR5	Control output hold time	tIH	0.5 tCK - 0.3	—	ns
DDR6 CK >= 200 MHz	Address output setup time	tIS	0.5 tCK - 1.3	—	ns
DDR7 CK >= 200 MHz	Address output hold time	tIH	0.5 tCK - 1.3	—	ns
DDR6 CK < 200 MHz	Address output setup time	tIS	1	—	ns
DDR7 CK < 200 MHz	Address output hold time	tIH	1	—	ns

4.9.2.3 eCSPI Master Mode Timing

Figure 34 depicts the timing of eCSPI in master mode and Table 52 lists the eCSPI master mode timing characteristics.

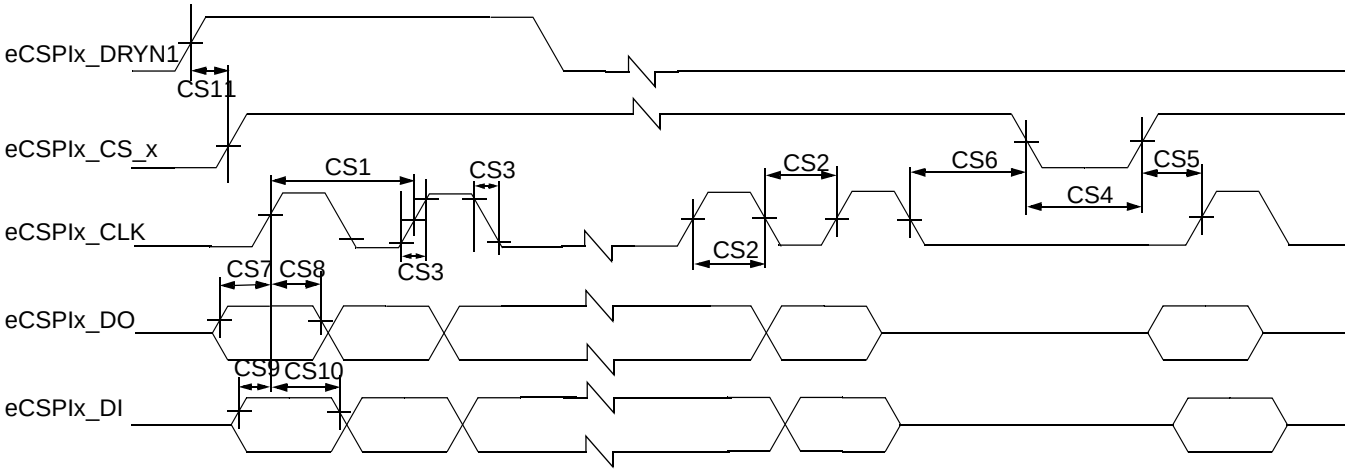

Figure 34. eCSPI Master Mode Timing Diagram

Table 52. eCSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	eCSPIx_CLK Cycle Time–Read eCSPIx_CLK Cycle Time–Write	t_{clk}	60 15	—	ns
CS2	eCSPIx_CLK High or Low Time	t_{SW}	6	—	ns
CS3	eCSPIx_CLK Rise or Fall	$t_{RISE/FALL}$	—	—	ns
CS4	eCSPIx_CS_x pulse width	t_{CSLH}	15	—	ns
CS5	eCSPIx_CS_x Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	eCSPIx_CS_x Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	eCSPIx_DO Setup Time	t_{Smosi}	5	—	ns
CS8	eCSPIx_DO Hold Time	t_{Hmosi}	5	—	ns
CS9	eCSPIx_DI Setup Time	t_{Smiso}	5	—	ns
CS10	eCSPIx_DI Hold Time	t_{Hmiso}	5	—	ns
CS11	eCSPIx_DRYN Setup Time	t_{SDRY}	5	—	ns

4.9.2.4 eCSPI Slave Mode Timing

Figure 35 depicts the timing of eCSPI in slave mode and Table 53 lists the eCSPI slave mode timing characteristics.

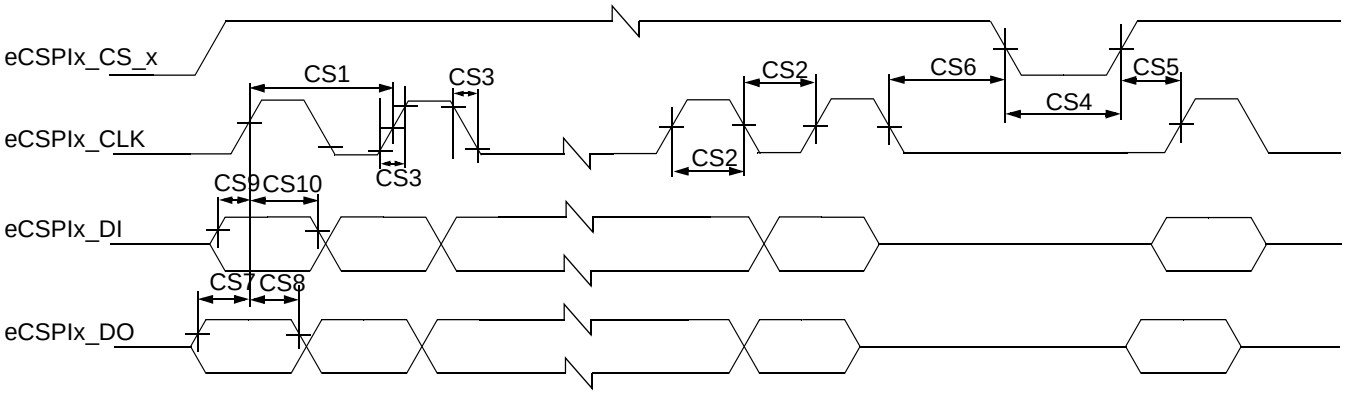

Figure 35. eCSPI Slave Mode Timing Diagram

Table 53. eCSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	eCSPIx_CLK Cycle Time–Read eCSPIx_CLK Cycle Time–Write	t_{clk}	60 15	—	ns
CS2	eCSPIx_CLK High or Low Time	t_{SW}	6	—	ns
CS3	eCSPIx_CLK Rise or Fall	$t_{RISE/FALL}$	—	—	ns
CS4	eCSPIx_CS_x pulse width	t_{CSLH}	15	—	ns
CS5	eCSPIx_CS_x Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	eCSPIx_CS_x Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	eCSPIx_DO Setup Time	t_{Smosi}	5	—	ns
CS8	eCSPIx_DO Hold Time	t_{Hmosi}	5	—	ns
CS9	eCSPIx_DI Setup Time	t_{Smiso}	5	—	ns
CS10	eCSPIx_DI Hold Time	t_{Hmiso}	5	—	ns

Table 54. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
eSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	eSDHC Output Delay	t_{OD}	–2	2	ns
eSDHC Input/Card Outputs CMD, DAT (Reference to CLK)					
SD7	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	eSDHC Input Hold Time[4]	t_{IH}	2.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.9.3.2 eMMC4.4 (Dual Data Rate) eSDHCv3 and uSDHC AC Timing

Figure 37 depicts the timing of eMMC4.4, and Table 55 lists the eMMC4.4 timing characteristics. Be aware that only DAT0-7 is sampled on both edges of clock (not applicable to CMD).

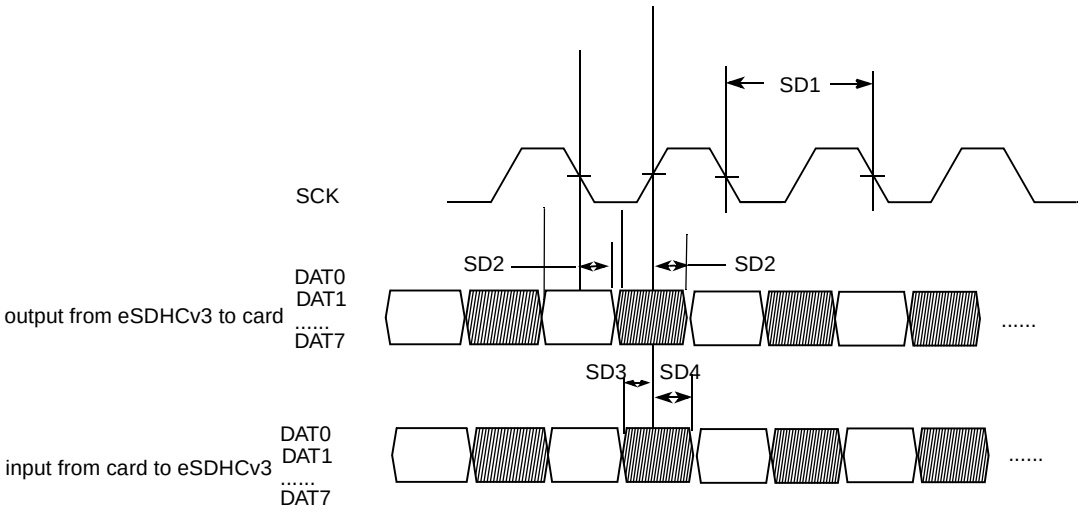

Figure 37. eMMC4.4 Timing

Table 55. eMMC4.4 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}	0	52	MHz
eSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					

Table 59. I²C Module Timing Parameters (continued)

ID	Parameter	Standard Mode Supply Voltage = 1.65 V–1.95 V, 2.7 V–3.3 V		Fast Mode Supply Voltage = 2.7 V–3.3 V		Unit
		Min	Max	Min	Max	
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal.

3 A Fast-mode I²C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2CLK line is released.

4 C_b = total capacitance of one bus line in pF.

4.9.6 One-Wire (OWIRE) Timing Parameters

Figure 42 depicts the RPP timing, and Table 60 lists the RPP timing parameters.

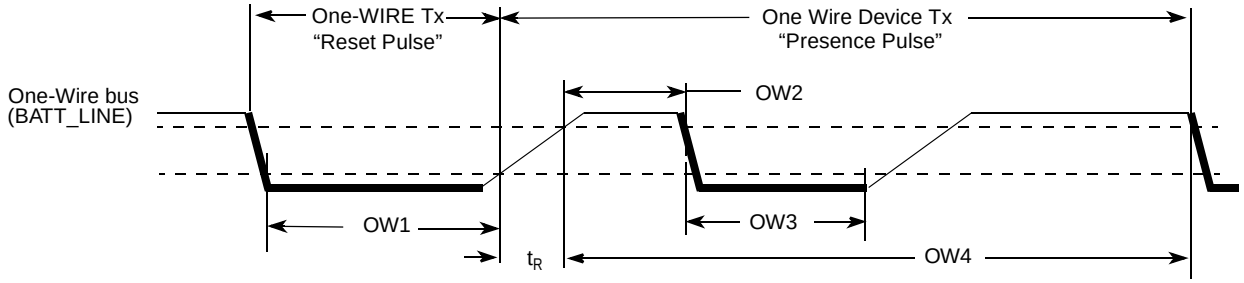

Figure 42. Reset and Presence Pulses (RPP) Timing Diagram

Table 63. PWM Output Timing Parameter

Ref. No.	Parameter	Min	Max	Unit
1	System CLK frequency[1]	0	ipg_clk	MHz
2a	Clock high time	12.29	—	ns
2b	Clock low time	9.91	—	ns
3a	Clock fall time	—	0.5	ns
3b	Clock rise time	—	0.5	ns
4a	Output delay time	—	9.37	ns
4b	Output setup time	8.71	—	ns

[1] CL of PWMO = 30 pF

4.9.8 Secure JTAG Controller (SJC) Timing Parameters

Figure 47 depicts the SJC test clock input timing. Figure 48 depicts the SJC boundary scan timing. Figure 49 depicts the SJC test access port. Figure 50 depicts the TRST timing. The signal parameters are listed in Table 64.

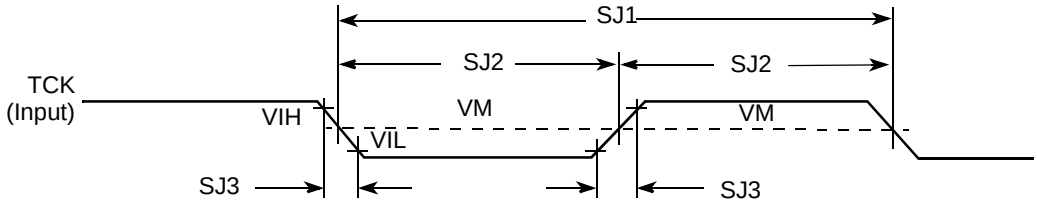

Figure 47. Test Clock Input Timing Diagram

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number: IMX50CEC
Rev. 7
10/2013

freescale™