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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	DDR2, LPDDR, LPDDR2
Graphics Acceleration	Yes
Display & Interface Controllers	EPDC, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Boot Security, Cryptography, Secure JTAG
Package / Case	416-LFBGA
Supplier Device Package	416-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx507cvk8b

- Pixel Processing Pipeline (ePXP)

  The ePXP is a high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma mapping, and rotation. The ePXP is enhanced with features specifically for grayscale applications working in conjunction with the electrophoretic display controller to form a full grayscale display solution. In addition, the ePXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated LCD controller (eLCDIF).
- Graphics acceleration

  The i.MX50 provides a 2D graphics accelerator with performance up to 200 Mpix/s.

1.1.5 Multilevel Memory System

The multilevel memory system of the i.MX50 is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The i.MX50 supports many types of external memory devices, including DDR2, LPDDR2, LPDDR1, NOR Flash, PSRAM, Cellular RAM, NAND Flash (MLC and SLC) and OneNAND™, and managed NAND including eMMC up to rev. 4.4.

1.1.6 Smart Speed™ Technology

The i.MX50 device has power management throughout the SOC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart Speed technology enables the designer to deliver a feature-rich product that requires levels of power that are far less than industry expectations.

1.1.7 Interface Flexibility

The i.MX50 supports connection to a variety of interfaces, including an LCD controller for displays, two high-speed USB on-the-go-capable PHYs, multiple expansion card ports (high-speed MMC/SDIO host and others), 10/100 Ethernet controller, and a variety of other popular interfaces (for example, UART, I^2C, and I^2S serial audio).

1.1.8 Advanced Security

The i.MX50 delivers hardware-enabled security features, such as High-Assurance Boot 4 (HAB4) for signed/authenticated firmware images, basic DRM support with random private keys and AES encryption/decryption, and storage and programmability of on-chip fuses.

1.2 Features

The i.MX50 applications processor is based on the ARM Cortex-A8 platform and has the following features:

- MMU, L1 instruction cache, and L1 data cache
- Unified L2 cache
- 800 MHz or 1 GHz target frequency of the core (including NEON, VFPv3, and L1 cache)

Table 5. Special Signal Considerations (continued)

Signal Name	Remarks
PMIC_RDY	This input may be used by a PMIC to signal to the i.MX50 that the PMIC supply outputs are at operating levels when resuming from STOP mode. The PMIC_RDY input is pin muxed on ALT3 of the I2C3_SCL pin and is in the NVCC_MISC domain.
POP_EMMC_RST (416 PoPBGA Only)	This pin is the PoP eMMC 4.4 Reset pin. The customer may connect this on their PCB to any free GPIO, or just leave floating for non-4.4 eMMC. This pin does not connect to the i.MX50 die.
POP_LPDDR2_ZQ0/ZQ1 (416 PoPBGA Only)	These pins connect to the PoP LPDDR2 DRAM ZQ pins and should be connected on the customer PCB to a 240 Ω 1% resistor to ground if used. These pins do not connect to the i.MX50 die.
POP_LPDDR2_1.8V (416 PoPBGA Only)	These pins are the 1.8 V supply for the PoP LPDDR2 DRAM. These pins do not connect to the i.MX50 die.
POP_NAND_VCC (416 PoPBGA Only)	This is the 3.3V I/O and memory supply for the PoP eMMC. Note that most eMMC can operate with a 1.8V I/O or a 3.3V I/O voltage. However, because we tied the eMMC memory and I/O domains together, you can't use the 1.8 V I/O option for the PoP eMMC, only 3.3 V I/O.
POR_B	This POWER-ON RESET input is a cold reset negative logic input that resets all modules and logic in the IC. The POR_B pin should have an external 68 K pull-up to NVCC_RESET and a 1 μF capacitor to ground. **Note:** The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail is at its working voltage.
RESET_IN_B	This warm reset negative logic input resets all modules and logic except for the following: • Test logic (JTAG, IOMUXC, DAP) • SRTC • Cold reset logic of WDOG—Some WDOG logic is only reset by POR_B. See WDOG chapter in the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM) for details.
SSI_EXT1_CLK, SSI_EXT2_CLK	The SSI_EXT1_CLK and SSI_EXT2_CLK outputs are recommended for generating a clock output from the i.MX50. Use of the CKO1 and CKO2 clock outputs is not recommended, as the large number of combinational logic muxes on those signals will impact jitter and duty-cycle. Note that these two clock outputs do not have dedicated pins: SSI_EXT1_CLK is IOMUX ALT3 on the OWIRE pin, and SSI_EXT2_CLK is IOMUX ALT3 of the EPITO pin.
TEST_MODE	TEST_MODE is for Freescale factory use only. This signal is internally connected to an on-chip pull-down device. The user must either float this signal or tie it to GND.
USB_H1_GPANAIO, USB_OTG_GPANAIO	These signals are reserved for Freescale manufacturing use only. Users should float these outputs.
USB_H1_RREFEXT, USB_OTG_RREFEXT	These signals determine the reference current for the USB PHY bandgap reference. An external 6.04 kΩ 1% resistor to GND is required. This resistor should be connected through a short (low impedance connection) and placed away from other noisy regions. If USB_H1 is not used, the H1 RREFEXT resistor may be eliminated and the pin left floating. If USB_OTG is not used, the OTG RREFEXT resistor may be eliminated and the pin left floating.

4.4.1 GPIO Output Buffer Impedance

Table 24 shows the GPIO output buffer impedance of the i.MX50 processor.

Table 24. GPIO Output Buffer Impedance

Parameter	Symbol	Test Conditions	Min	Typ		Max	Unit
				OVDD 2.775 V	OVDD 1.875V		
Output driver impedance	Rpu	Low drive strength, Ztl = 150 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω Max drive strength, Ztl = 37.5 Ω	80 40 27 20	104 52 35 26	150 75 51 38	250 125 83 62	Ω
Output driver impedance	Rpd	Low drive strength, Ztl = 150 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω Max drive strength, Ztl = 37.5 Ω	64 32 21 16	88 44 30 22	134 66 44 34	243 122 81 61	Ω

4.4.2 LVIO Output Buffer Impedance

Table 25 shows the LVIO output buffer impedance of the i.MX50 processor.

Table 25. LVIO Output Buffer Impedance

Parameter	Symbol	Test Conditions	Min	Typ		Max	Unit
				OVDD 2.775 V	OVDD 1.875V		
Output driver impedance	Rpu	Low drive strength, Ztl = 150 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω Max drive strength, Ztl = 37.5 Ω	80 40 27 20	104 52 35 26	150 75 51 38	250 125 83 62	Ω
Output driver impedance	Rpd	Low drive strength, Ztl = 150 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω Max drive strength, Ztl = 37.5 Ω	64 32 21 16	88 44 30 22	134 66 44 34	243 122 81 61	Ω

4.5.8 LPDDR1 I/O AC Parameters

Table 34 shows the AC parameters for LPDDR1 I/O.

Table 34. LPDDR1 I/O AC Parameters

Parameter	Symbol	Min	Max	Unit
AC input logic high	Vihd(ac)	0.8*ovdd	ovdd+0.3	V
AC input logic low	Vild(ac)	-0.3	0.2*ovdd	
AC input differential voltage[1]	Vid(ac)	0.6*ovdd	ovdd+0.6	
AC input differential crosspoint voltage[2]	Vix(ac)	0.4*ovdd	0.6*ovdd	
Output propagation delay high to low	tPOHLD		2.5	ns
Output propagation delay low to high	tPOLHD		2.5	
Input propagation delay high to low	tPIHLD		1.5	
Input propagation delay low to high	tPILHD		1.5	
Single output slew rate	tsr	0.3	2.5	V/ns

[1]Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac)-Vil(ac)

[2]The typical value of Vix(ac) is expected to be about 0.5*ovdd. and Vix(ac) is expected to track variation of ovdd. Vix(ac) indicates the voltage at which differential input signal must cross.

4.5.9 LPDDR2 I/O AC Parameters

Table 35 shows the AC parameters for LPDDR2 I/O.

Table 35. LPDDR2 I/O AC Parameters

Parameter	Symbol	Min	Max	Unit
AC input logic high	Vih(ac)	Vref+0.22	ovdd	V
AC input logic low	Vil(ac)	ovss	Vref-0.22	
AC differential input high voltage[1]	Vidh(ac)	0.44	-	
AC differential input low voltage	Vidhl(ac)	-	0.44	
AC input differential cross point voltage (relative to ovdd / 2)[2]	Vix(ac)	-0.12	0.12	
Over/undershoot peak	Vpeak		0.35	ns
Over/undershoot area (above OVDD or below OVSS)	Varea		0.6 (at 266 MHz)	V-ns
Output propagation delay high to low	tPOHLD		3.5	ns
Output propagation delay low to high	tPOLHD		3.5	
Input propagation delay high to low	tPIHLD		1.5	
Input propagation delay low to high	tPILHD		1.5	

Table 37. WDOG_RST_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC5	Duration of WDOG_RST_B Assertion	1	—	T_{CKIL}

NOTE

CKIL is approximately 32 kHz. T_{CKIL} is one period or approximately 30 µs.

4.6.3 Clock Amplifier Parameters (CKIH)

The input to clock amplifier (CAMP) is internally ac-coupled allowing direct interface to a square wave or sinusoidal frequency source. No external series capacitors are required.

Table 38 shows the electrical parameters of CAMP.

Table 38. CAMP Electrical Parameters (CKIH)

Parameter	Min	Typ	Max	Unit
Input frequency	8.0	—	40.0	MHz
VIL (for square wave input)	0	—	0.3	V
VIH (for square wave input)	(VCC[1] – 0.25)	—	3	V
Sinusoidal input amplitude	0.4 [2]	—	VDD	Vp-p
Output duty cycle	45	50	55	%

1 VCC is the supply voltage of CAMP.

2 This value of the sinusoidal input is determined during characterization.

4.6.4 DPLL Electrical Parameters

Table 39 shows the electrical parameters of digital phase-locked loop (DPLL).

Table 39. DPLL Electrical Parameters

Parameter	Test Conditions/Remarks	Min	Typ	Max	Unit
Reference clock frequency range[1]	—	10	—	100	MHz
Reference clock frequency range after pre-divider	—	10	—	40	MHz
Output clock frequency range (dpdck_2)	—	300	—	1025	MHz
Pre-division factor[2]	—	1	—	16	—
Multiplication factor integer part	—	5	—	15	—
Multiplication factor numerator[3]	Should be less than denominator	–67108862	—	67108862	—
Multiplication factor denominator[2]	—	1	—	67108863	—
Output duty cycle	—	48.5	50	51.5	%

Table 40. Asynchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T[2] = GPMI Clock Cycle[3]		Example Timing for GPMI Clock ≈ 100MHz T = 10ns		Unit
			Min.	Max.	Min.	Max.	
NF5	$\overline{WE}$ pulse width	tWP	DS*T		10		ns
NF6	ALE setup time	tALS	(AS+1)*T	—	10	—	ns
NF7	ALE hold time	tALH	(DH+1)*T	—	20	—	ns
NF8	Data setup time	tDS	DS*T	—	10	—	ns
NF9	Data hold time	tDH	DH*T	—	10	—	ns
NF10	Write cycle time	tWC	(DS+DH)*T		20		ns
NF11	$\overline{WE}$ hold time	tWH	DH*T		10		ns
NF12	Ready to $\overline{RE}$ low	tRR	(AS+1)*T	—	10	—	ns
NF13	$\overline{RE}$ pulse width	tRP	DS*T	—	10	—	ns
NF14	READ cycle time	tRC	(DS+DH)*T	—	20	—	ns
NF15	$\overline{RE}$ high hold time	tREH	DH*T		10	—	ns
NF16	Data setup on read	tDSR	N/A		10	—	ns
NF17	Data hold on read	tDHR	N/A		10	—	ns

1 GPMI's Async Mode output timing could be controlled by module's internal register, say HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers' setting. In the above table, we use AS/DS/DH representing these settings each.

2 T represents for the GPMI clock period.

3 AS minimum value could be 0, while DS/DH minimum value is 1.

Table 41. Source Synchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF24	postamble delay	t_{POST}	POST_DELAY*t_{CK}	—	ns
NF25	CLE and ALE setup time	t_{CALS}	0.5*t_{CK}	—	ns
NF26	CLE and ALE hold time	t_{CALH}	0.5*t_{CK}	—	ns
NF27	Data input to first DQS latching transition	t_{DQSS}	t_{CK}	—	ns

1 GPMI's sync mode output timing could be controlled by module's internal register, say HW_GPMI_TIMING2_CE_DELAY, HW_GPMI_TIMING_PREAMBLE_DELAY, and HW_GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers' setting. In the above table, we use CE_DELAY/PRE_DELAY/POST_DELAY representing these settings each.

4.6.5.3 Samsung Toggle Mode AC Timing

4.6.5.3.1 Command and Address Timing

NOTE

Samsung Toggle Mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. Please refer to the above chapter for details.

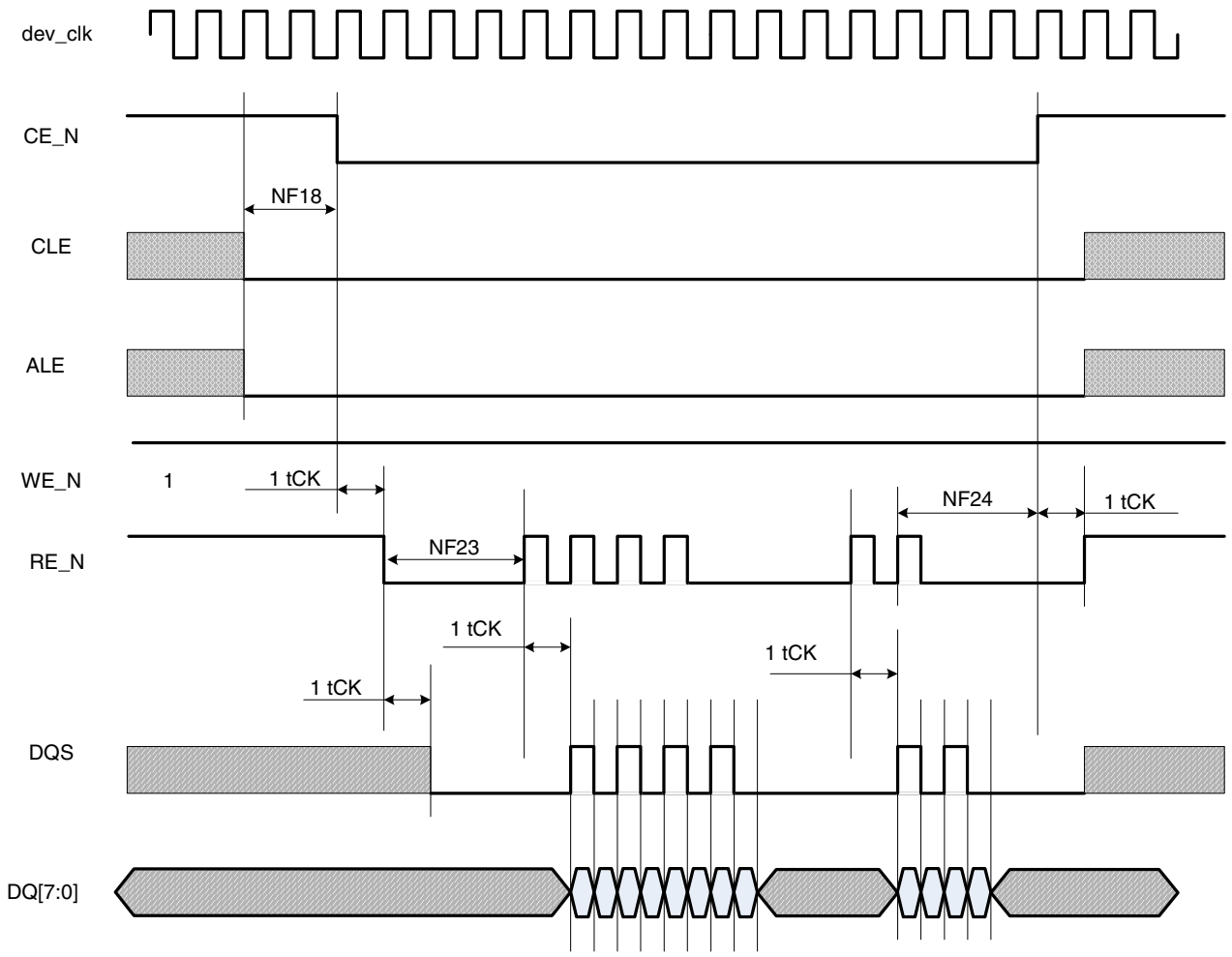

Figure 16. Samsung Toggle Mode Data Read Timing

Table 42. Samsung Toggle Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	CE# access time	t_{CE}	CE_DELAY*t_{CK}	—	ns
NF19	CE# hold time	t_{CH}	0.5 *t_{CK}	—	ns
NF20	Command/address DQ setup time	t_{CAS}	0.5*t_{CK}	—	ns
NF21	Command/address DQ hold time	t_{CAH}	0.5*t_{CK}	—	ns
NF22	clock period	t_{CK}	7.5	—	ns

Table 43. EIM Bus Timing Parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	EIM_BCLK Cycle time[2]	t	—	2t	—	3t	—	4t	—
WE2	EIM_BCLK Low Level Width	0.4t	—	0.8t	—	1.2t	—	1.6t	—
WE3	EIM_BCLK High Level Width	0.4t	—	0.8t	—	1.2t	—	1.6t	—
WE4	Clock rise to address valid[3]	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE5	Clock rise to address invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE6	Clock rise to EIM_CSx valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE7	Clock rise to EIM_CSx invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE8	Clock rise to EIM_RW valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE9	Clock rise to EIM_RW invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE10	Clock rise to EIM_OE valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE11	Clock rise to EIM_OE invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE12	Clock rise to EIM_EBx valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE13	Clock rise to EIM_EBx invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE14	Clock rise to EIM_LBA valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE15	Clock rise to EIM_LBA invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE16	Clock rise to Output Data valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	2t – 1.25	2t + 1.75
WE17	Clock rise to Output Data Invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	2t – 1.25	2t + 1.75
WE18	Input Data setup time to Clock rise	2	—	2	—	2	—	2	—
WE19	Input Data hold time from Clock rise	2.5	—	2.5	—	2.5	—	2.5	—
WE20	EIM_WAIT setup time to Clock rise	2	—	2	—	2	—	2	—
WE21	EIM_WAIT hold time from Clock rise	2.5	—	2.5	—	2.5	—	2.5	—

1 *t* is axi_clk cycle time. The maximum allowed axi_clk frequency is 133 MHz, whereas the maximum allowed EIM_BCLK frequency is 66.5 MHz. As a result, if BCD = 0, axi_clk must be ≤ 66.5 MHz. If BCD = 1, then 133 MHz is allowed for axi_clk, resulting in a EIM_BCLK of 66.5 MHz. When the clock branch to EIM is decreased to 66.5 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM) for a detailed clock tree description.

NOTE

DDR6 and DDR7 can be adjusted by the parameter -DLL_WR_DELAY-;

The ideal case is that SDCLK is center aligned to the DRAM_A[9:0] data valid window;

For this table, HW_DRAM_PHY23[14:8] (DLL_WR_DELAY) = 0x10;

4.8.3 DRAM Data Output Timing

The DRAM data output timing is defined for all DDR types: DDR2, LPDDR1, and LPDDR2.

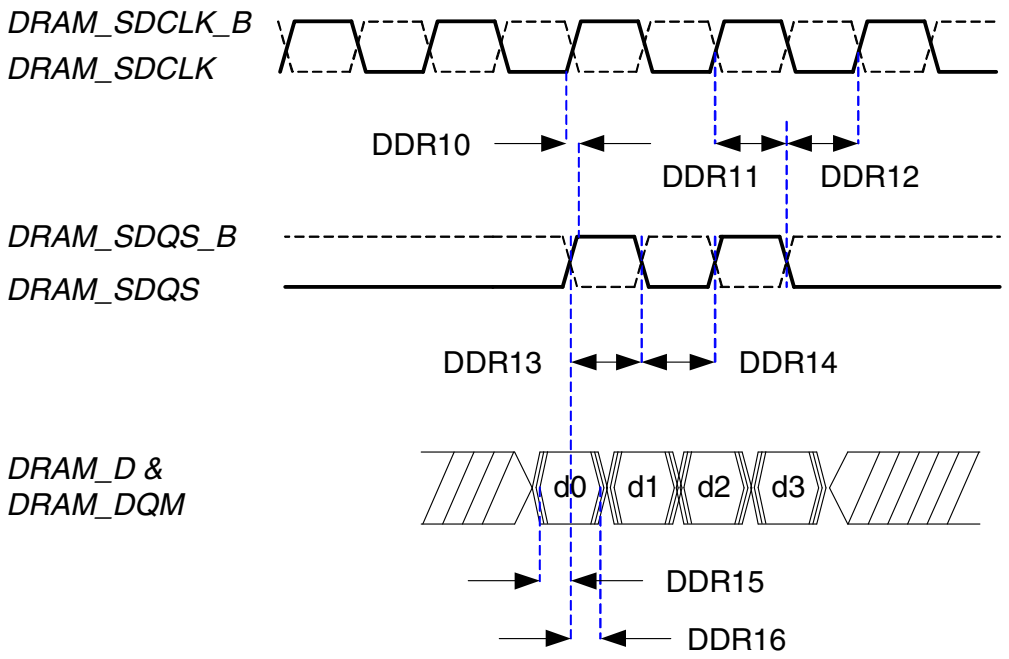

Figure 30. DRAM Data Output Timing

Table 47. DDR Output AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR10	Positive DQS latching edge to associated CK edge	tDQSS	-0.3	0.3	ns
DDR11	DQS falling edge from CK rising edge—hold time	tDSH	0.5 tCK - 0.3	0.5 tCK + 0.3	ns
DDR12	DQS falling edge to CK rising edge—setup time	tDSS	0.5 tCK - 0.3	0.5 tCK + 0.3	ns
DDR13	DQS output high pulse width	tDQSH	0.48 tCK	0.52 tCK	ns
DDR14	DQS output low pulse width	tDQSL	0.48 tCK	0.52 tCK	ns
DDR15 CK >= 200 MHz	DQ & DQM output setup time relative to DQS	tDS	0.5 tCK - 1.3	—	ns

Table 48. DDR2 Input AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR21	DQS to DQ input skew	tDQSQ	—	0.65	ns
DDR22	DQS to DQ input hold time	tQH	0.45 tCK -0.85	—	ns

NOTE

The timing parameter DDR20(tDQSCK) is not strictly required by this DRAM MC design.

4.9 External Peripheral Interfaces

The following sections provide information on external peripheral interfaces.

4.9.1 AUDMUX Timing Parameters

The AUDMUX provides programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is hence governed by the SSI module.

4.9.2 CSPI and eCSPI Timing Parameters

This section describes the timing parameters of the CSPI and eCSPI modules. The CSPI and eCSPI have separate timing parameters for master and slave modes. The nomenclature used with the CSPI/eCSPI modules and the respective routing of these signals is shown in Table 49.

Table 49. CSPI Nomenclature and Routing

Module	I/O Access
eCSPI1	GPIO, KPP, DISP0_DAT, CSI0_DAT, and EIM_D through IOMUX
eCSPI2	DISP0_DAT, CSI0_DAT, and EIM through IOMUX
CSPI	DISP0_DAT, EIM_A/D, SD1, and SD2 through IOMUX

4.9.10.3.1 UART IrDA Mode Transmitter

Figure 57 depicts the UART IrDA mode transmit timing with 8 data bit/1 stop bit format. Table 73 lists the transmit timing characteristics.

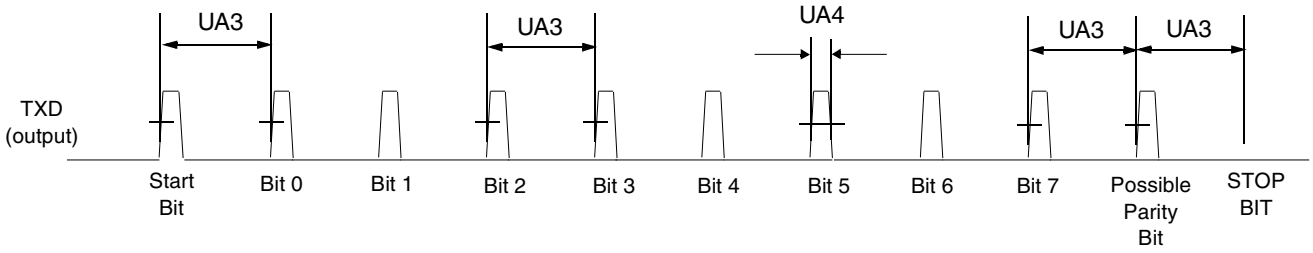

Figure 57. UART IrDA Mode Transmit Timing Diagram

Table 73. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16)*(1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16)*(1/F_{baud\_rate}) + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.9.10.3.2 UART IrDA Mode Receiver

Figure 58 depicts the UART IrDA mode receive timing with 8 data bit/1 stop bit format. Table 74 lists the receive timing characteristics.

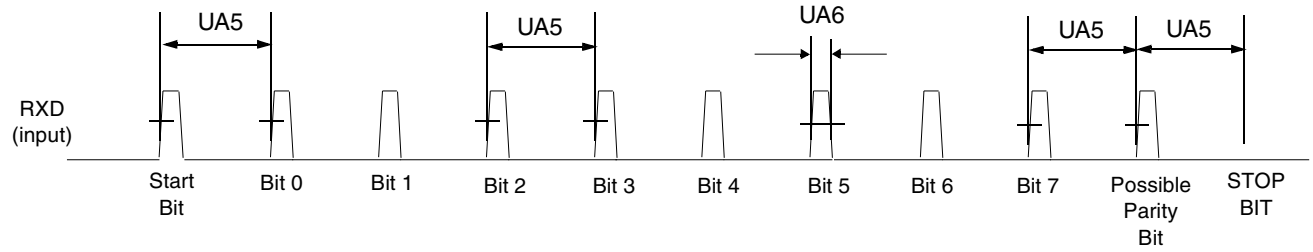

Figure 58. UART IrDA Mode Receive Timing Diagram

Table 74. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$ [2] – $1/(16*F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16*F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16)*(1/F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16*F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16*F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

5.1.1 Case 416 MAPBGA, 13 x 13 mm, 0.5 mm Pitch Package Views

Figure 59 shows the top view of the 13 x 13 mm package, Figure 60 shows the bottom view (416 soldier balls) of the 13 x 13 mm package, and Figure 61 shows the side view of the 13 x 13 mm package.

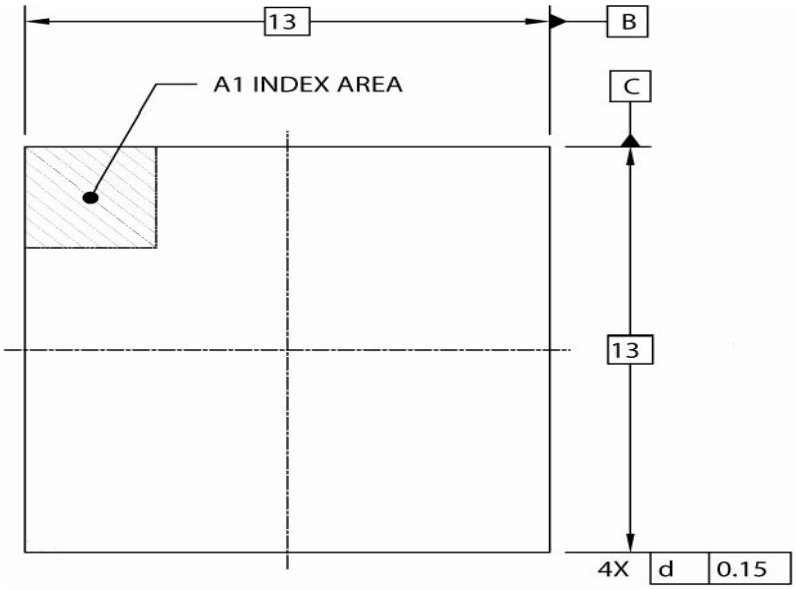

Figure 59. 416 MAPBGA 13x13 mm Package Top View

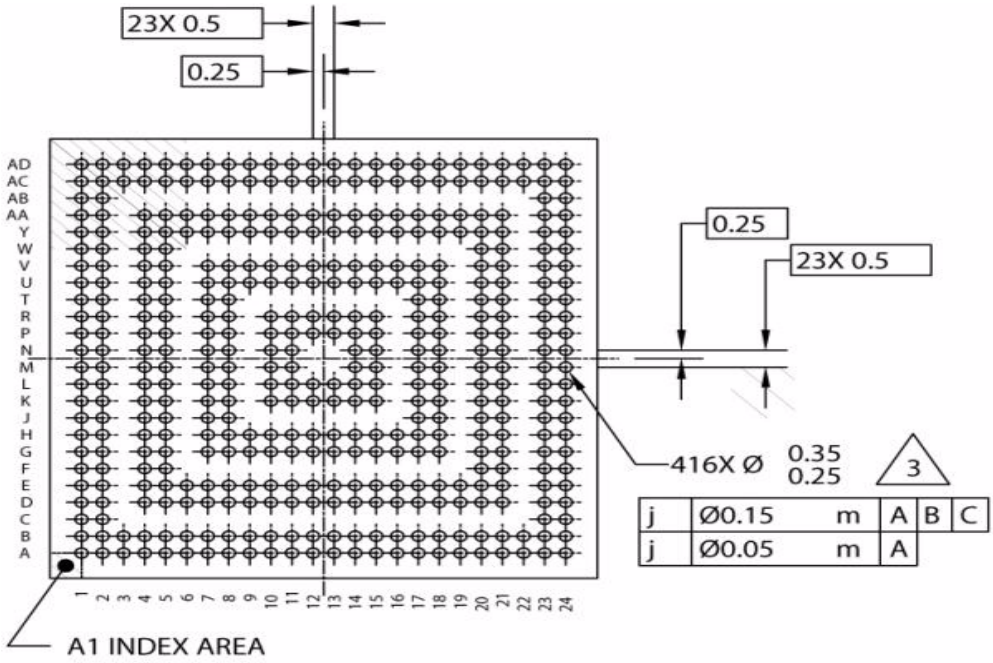

Figure 60. 416 MAPBGA 13x13 mm Package Bottom View

Table 79. 416 MAPBGA 13x13 mm, 0.5 mm Pitch Ball Map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
AB	BOOT_MODE0	BOOT_MODE1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	DRAM_SDQS2	DRAM_SDQS2_B	AB
AC	RESET_IN_B	TEST_MODE	GND3P0	GND2P5	EXTAL	GND1P2	GND1P8	USB_OTG_DN	USB_OTG_VDDA25_1	USB_H1_DN	USB_H1_VDDA33	DISP_BUSY	DISP_RS	DISP_RESET	SD3_D0	SD3_D1	SD3_D2	VSS	DRAM_D16	DRAM_D18	NVCC_EMI_DRAM	DRAM_D20	DRAM_D22	DRAM_DQM2	AC
AD	VSS	POR_B	VDD3P0	VDD2P5	XTAL	VDD1P2	VDD1P8	USB_OTG_DP	USB_H1_VDDA25_1	USB_H1_DP	USB_OTG_VDDA33	DISP_WR	DISP_RD	DISP_CS	SD3_WP	SD3_CLK	SD3_CMD	VSS	DRAM_D17	DRAM_D19	NVCC_EMI_DRAM	DRAM_D21	DRAM_D23	VSS	AD

5.1.3 416 MAPBGA 13 x 13 Power Rails

Table 80. 416 MAPBGA 13x13 Ground, Power, Sense, and Reference Contact Signals

Pin Name	Ball Number	Comments
GND_DCDC	W5	—
NVCC_EIM	L7, M7, M8	—
NVCC_EMI_DRAM	A21, AA21, AA23, AA24, AC21, AD21, B21, D21, D23, D24, K21, K23, K24, R21, R23, R24	—
NVCC_EPDC	M10, N10, P10, R10, U10	—
NVCC_JTAG	U9	—
NVCC_KEYPAD	N8	—
NVCC_LCD	U11	—
NVCC_MISC	P8	—
NVCC_NANDF	V9, V10	—
NVCC_RESET	V8	—
NVCC_SD1	T7	—
NVCC_SD2	U8	—
NVCC_SPI	R7	—

Table 80. 416 MAPBGA 13x13 Ground, Power, Sense, and Reference Contact Signals (continued)

NVCC_SRTC	AA1	—
NVCC_SSI	R8	—
NVCC_UART	T8	—
USB_H1_VDDA25	AD9	Note that on the 416 MAPBGA package, USB_OTG_VDDA25 and USB_H1_VDDA25 are shorted together on the substrate.
USB_H1_VDDA33	AC11	Note that on the 416 MAPBGA package, USB_OTG_VDDA33 and USB_H1_VDDA33 are shorted together on the substrate.
USB_OTG_VDDA25	AC9	Note that on the 416 MAPBGA package, USB_OTG_VDDA25 and USB_H1_VDDA25 are shorted together on the substrate.
USB_OTG_VDDA33	AD11	Note that on the 416 MAPBGA package, USB_OTG_VDDA33 and USB_H1_VDDA33 are shorted together on the substrate.
VCC	H14, H15, H16, H17, J17, K14, K15, K17, L15	—
VDD_DCDCI	Y6	—
VDD_DCDCO	Y5	—
VDD1P2	AD6	—
VDD1P8	AD7	—
VDD2P5	AD4	—
VDD3P0	AD3	—
VDDA	P17, R17	—
VDDAL1	P15, R15	—
VDDGP	G10, G8, G9, H10, H11, H8, H9, J8, K10, K11, K7, K8, L10, L11, L8	—
VDDO25	N23	—
VSS	A1, A18, A24, AA11, AA2, AA9, AC18, AC3, AC4, AC6, AC7, AD1, AD18, AD24, B18, G20, G21, G23, H12, H13, K12, K13, L12, L13, L14, L17, M11, M14, M15, M17, M18, M20, M21, N11, N14, N15, N17, P11, P12, P13, P14, R11, R12, R13, R14, T17, T18, U12, U13, U14, U15, U16, U17, U18, V17, V18, V20, V21, V23	—

Table 82. 416 PoPBGA 13 x 13 mm Ground, Power, Sense, and Reference Contact Signals (continued)

NVCC_RESET	V8	—
NVCC_SD1	T7	—
NVCC_SD2	U8	—
NVCC_SPI	R7	—
NVCC_SRTC	AA1	—
NVCC_SSI	R8	—
NVCC_UART	T8	—
POP_EMMC_RST	A19	This is PoP eMMC 4.4 NAND Reset input pin. This pin does not connect to the i.MX50. If using eMMC 4.4 NAND, this pin can be connected to a GPIO. For non 4.4 eMMC applications, leave floating.
POP_LPDDR2_1.8V	A20, B19, B20, M5, N5	This is the 1.8V supply for the PoP LPDDR2. These pins do not connect to the i.MX50.
POP_LPDDR2_ZQ0	AA24	This is the PoP LPDDR2 ZQ0 pin. This pin does not connect to the i.MX50. This should be connected on the PCB to a 240 Ω 1% resistor to ground
POP_LPDDR2_ZQ1	AA23	This is the PoP LPDDR2 ZQ1 pin. This pin does not connect to the i.MX50. If used, this should be connected on the PCB to a 240 Ω 1% resistor to ground
POP_NAND_VCC	D19, D20	This is the 3.3V I/O and memory supply for the PoP eMMC NAND. Note that because the eMMC memory and I/O domains are shorted together, it is not possible to support 1.8 V I/O for the PoP eMMC NAND.
USB_VDDA25	AC9, AD9	Note that on the PoPBGA package, USB_OTG_VDDA25 and USB_H1_VDDA25 are shorted together.
USB_VDDA33	AC11, AD11	Note that on the PoPBGA package, USB_OTG_VDDA33 and USB_H1_VDDA33 are shorted together.
VCC	H14, H15, H16, H17, J17, K14, K15, K17, L15	—
VDD_DCDCI	Y6	—
VDD_DCDCO	Y5	—
VDD1P2	AD6	—
VDD1P8	AD7	—

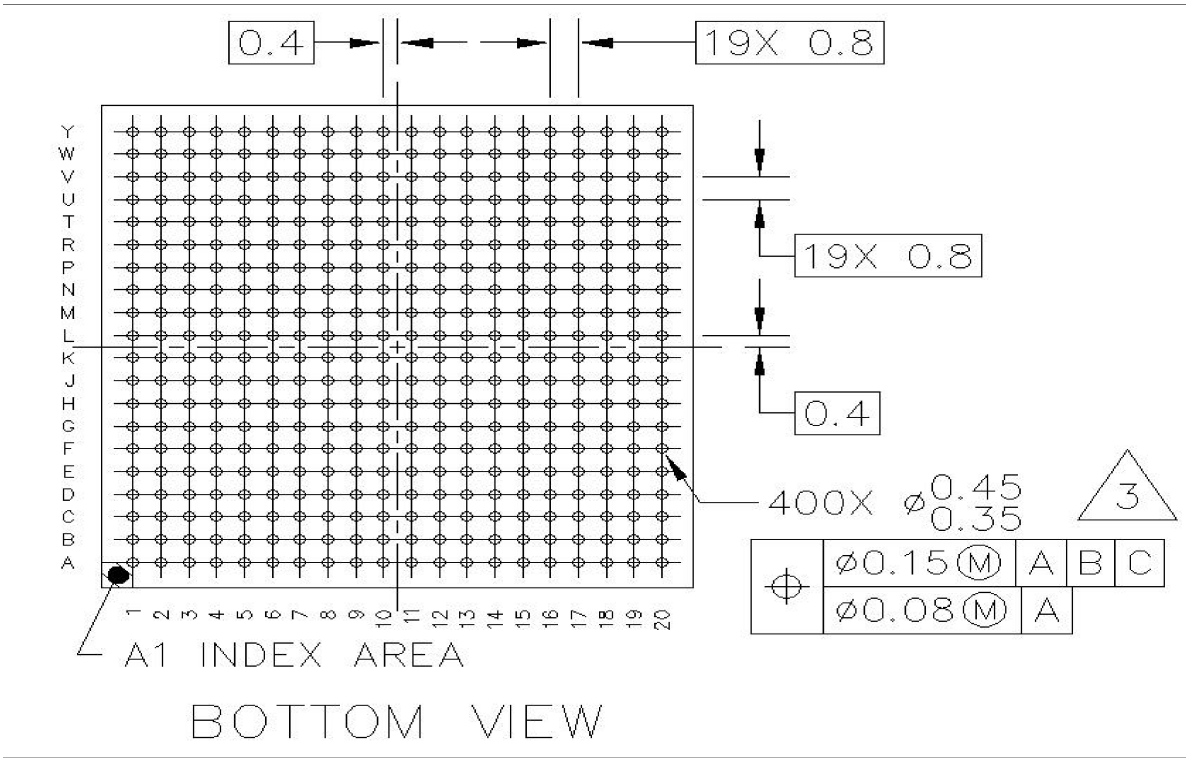

Figure 66. 400 MAPBGA 17x17 mm Package Bottom View

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
UART2_RTS	L2	C2		NVCC_UART	HVIO	ALT1	IN	Keeper
UART2_RXD	L1	C1	L2	NVCC_UART	HVIO	ALT1	IN	Keeper
UART2_TXD	K1	B1	L1	NVCC_UART	HVIO	ALT1	IN	Keeper
UART3_RXD	L4	E4	K3	NVCC_UART	HVIO	ALT1	IN	Keeper
UART3_TXD	K4	D4	J2	NVCC_UART	HVIO	ALT1	IN	Keeper
UART4_RXD	L5	D5	J3	NVCC_UART	HVIO	ALT1	IN	Keeper
UART4_TXD	K5	D6	H2	NVCC_UART	HVIO	ALT1	IN	Keeper
USB_H1_DN	AC10	AC10	W10	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	—	—
USB_H1_DP	AD10	AD10	Y10	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	—	—
USB_H1_GPANAIO	Y11	AA17	U10	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG25	—	—	—
USB_H1_RREFEXT	AA10	AA10	U9	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG25	—	—	—
USB_H1_VBUS	Y10	AA16	V9	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	—	—
USB_OTG_DN	AC8	AC8	W8	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG50	—	—	—
USB_OTG_DP	AD8	AD8	Y8	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG50	—	—	—
USB_OTG_GPANAIO	Y7	AA14	V7	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	—	—
USB_OTG_ID	Y8	AA12	Y7	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	—	—
USB_OTG_RREFEXT	AA8	AA8	W7	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	—	—
USB_OTG_VBUS	Y9	AA13	V8	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG50	—	—	—
VREF	M23	M23	K17	VDDO25	ANALOG	—	—	—
WDOG	G5	D9	F4	NVCC_MISC	HVIO	ALT1	IN	—
XTAL	AD5	AD5	Y6	VDD2P5	ANALOG	—	—	—

6 Revision History

Table 86 provides a revision history for this data sheet.

Table 86. i.MX50 Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 7	10/2013	• Added new part number information for parts with 1 GHz core frequencies: — MCIMX508CVK1B — MCIMX508CVM1B — MCIMX507CVM1B — MCIMX507CVK1B Updated sections: — Section 1, “Introduction” — Table 1, “Ordering Information” — Table 11, “i.MX50 Operating Ranges” — Table 15, “Maximum Supply Current Consumption—ARM CLK = 1 GHz” (added)
Rev. 6	07/2013	• In Table 11, “i.MX50 Operating Ranges,” added VCC Stop mode ranges.
Rev. 5	05/2013	• In Table 11, “i.MX50 Operating Ranges,” changed VCC peripheral supply (LPM) minimum voltage from 0.9 V to 1 V, and changed nominal voltage from 0.95 V to 1.05 V.
Rev. 4	01/2013	• In Table 1, "Ordering Information," on page 7, added new part number information for MCIMX507CVK8B. • In Figure 27, "DTACK Read Access," on page 67, updated timing of EIM_DTACK.
Rev. 3	10/2012	• In Table 11, "i.MX50 Operating Ranges," on page 24: —Changed DDR clock rate for reduced performance mode (RPM) of VCC from 100 MHz to 133 MHz —Changed DDR clock rate for high performance mode (HPM) of VCC from 200 MHz to 266 MHz
Rev. 2	05/2012	• In Table 1, "Ordering Information," on page 7, added the following new part numbers: MCIMX508CZK8B, MCIMX503CVK8B, MCIMX503EVM8B, MCIMX502CVK8B, and MCIMX502EVM8B. • In Table 1, "Ordering Information," on page 7, added a new column, $T_{junction}$. • In Table 3, "Package Feature Comparison," on page 9, added a new row for 416 PoPBGA package. • Updated Figure 1, "i.MX50 System Block Diagram," on page 10 by removing “LDOx3” and “DC-DC 1.2V.” • In Table 5, "Special Signal Considerations," on page 17, updated details for the following signals: DRAM_OPEN/DRAM_OPENFB and DRAM_SDODT0/DRAM_SDODT1 • In Table 5, "Special Signal Considerations," on page 17, added new rows for the following signals: POP_EMMC_RST, POP_LPDDR2_ZQ0/ZQ1, POP_LPDDR2_1.8V, and POP_NAND_VCC. • Added Section 4.1.2.1, “13 x 13 mm MAPBGA Package Thermal Resistance Data.” • Added Section 4.1.2.2, “13 x 13 mm PoPBGA Package Thermal Resistance Data.” • Added Section 4.1.2.3, “17 x 17 mm MAPBGA Package Thermal Resistance Data.” • In Table 11, "i.MX50 Operating Ranges," on page 24, added footnotes for USB_OTG_VDDA25 and USB_OTG_VDDA33. • In Table 78, "VBUS Comparators Thresholds," on page 101, changed VBUS input max current to 350 µA. • Added Section 5.2, “13 x 13 mm, 0.5 mm Pitch, 416 Pin PoPBGA Package Information.” • In Table 85, "Alphabetical List of Signal Assignments," on page 124: —Added a new column “416 PoPBGA Ball Number” —Changed “USB_H1_VDDA” to “USB_H1_VDDA25, USB_H1_VDDA33” —Changed “USB_OTG_VDDA” to “USB_OTG_VDDA25, USB_OTG_VDDA33” • Replace mDDR with LPDDR1 throughout the document.

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