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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Boot Security, Cryptography, Secure JTAG
Package / Case	416-LFBGA
Supplier Device Package	416-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx507cvk8br2

- Pixel Processing Pipeline (ePXP)

  The ePXP is a high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma mapping, and rotation. The ePXP is enhanced with features specifically for grayscale applications working in conjunction with the electrophoretic display controller to form a full grayscale display solution. In addition, the ePXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated LCD controller (eLCDIF).
- Graphics acceleration

  The i.MX50 provides a 2D graphics accelerator with performance up to 200 Mpix/s.

1.1.5 Multilevel Memory System

The multilevel memory system of the i.MX50 is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The i.MX50 supports many types of external memory devices, including DDR2, LPDDR2, LPDDR1, NOR Flash, PSRAM, Cellular RAM, NAND Flash (MLC and SLC) and OneNAND™, and managed NAND including eMMC up to rev. 4.4.

1.1.6 Smart Speed™ Technology

The i.MX50 device has power management throughout the SOC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart Speed technology enables the designer to deliver a feature-rich product that requires levels of power that are far less than industry expectations.

1.1.7 Interface Flexibility

The i.MX50 supports connection to a variety of interfaces, including an LCD controller for displays, two high-speed USB on-the-go-capable PHYs, multiple expansion card ports (high-speed MMC/SDIO host and others), 10/100 Ethernet controller, and a variety of other popular interfaces (for example, UART, I^2C, and I^2S serial audio).

1.1.8 Advanced Security

The i.MX50 delivers hardware-enabled security features, such as High-Assurance Boot 4 (HAB4) for signed/authenticated firmware images, basic DRM support with random private keys and AES encryption/decryption, and storage and programmability of on-chip fuses.

1.2 Features

The i.MX50 applications processor is based on the ARM Cortex-A8 platform and has the following features:

- MMU, L1 instruction cache, and L1 data cache
- Unified L2 cache
- 800 MHz or 1 GHz target frequency of the core (including NEON, VFPv3, and L1 cache)

- USB:
  - One High Speed (HS) USB 2.0 OTG-capable port with integrated HS USB PHY
  - One High Speed (HS) USB 2.0 host port with integrated HS USB PHY
- Miscellaneous interfaces:
  - One-wire (OWIRE) port
  - Two I2S/SSI/AC97 ports, supporting up to 1.4 Mbps each connected to the Audio Multiplexer (AUDMUX) providing four external ports
  - Five UART RS232 ports, up to 4.0 Mbps each
  - Two eCSPI (Enhanced CSPI) ports, up to 66 Mbps each plus CSPI port, up to 16.6 Mbps
  - Three I^2C ports, supporting 400 kbps
  - Fast Ethernet controller IEEE 802.3, 10/100 Mbps
  - Key pad port (KPP)
  - Two pulse width modulators (PWM)
  - GPIO with interrupt capabilities
  - Secure JTAG controller (SJC)

The system supports efficient and smart power control and clocking:

- Supporting DVFS techniques for low power modes, including auto slow architecture
- Power gating-SRPG (state retention power gating) for ARM core and NEON
- Support for various levels of system power modes
- Flexible clock gating control scheme
- On-chip temperature monitor
- On-chip 32 kHz and 24 MHz oscillators
- A total of four PLLs with the fourth PLL providing up to eight independently controllable outputs, improving the ease of clocking control, especially for display and connectivity modules

Security functions are enabled and accelerated by the following hardware:

- Secure JTAG controller (SJC)—Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features
- Secure real-time clock (SRTC)—Tamper resistant RTC with dedicated power domain and mechanism to detect voltage and clock glitches
- Advanced high assurance boot (A-HAB)—HAB with the next embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization

2 Architectural Overview

The following sections provide an architectural overview of the i.MX50 processor system.

2.1 Block Diagram

Figure 1 shows the functional modules in the i.MX50 processor system.

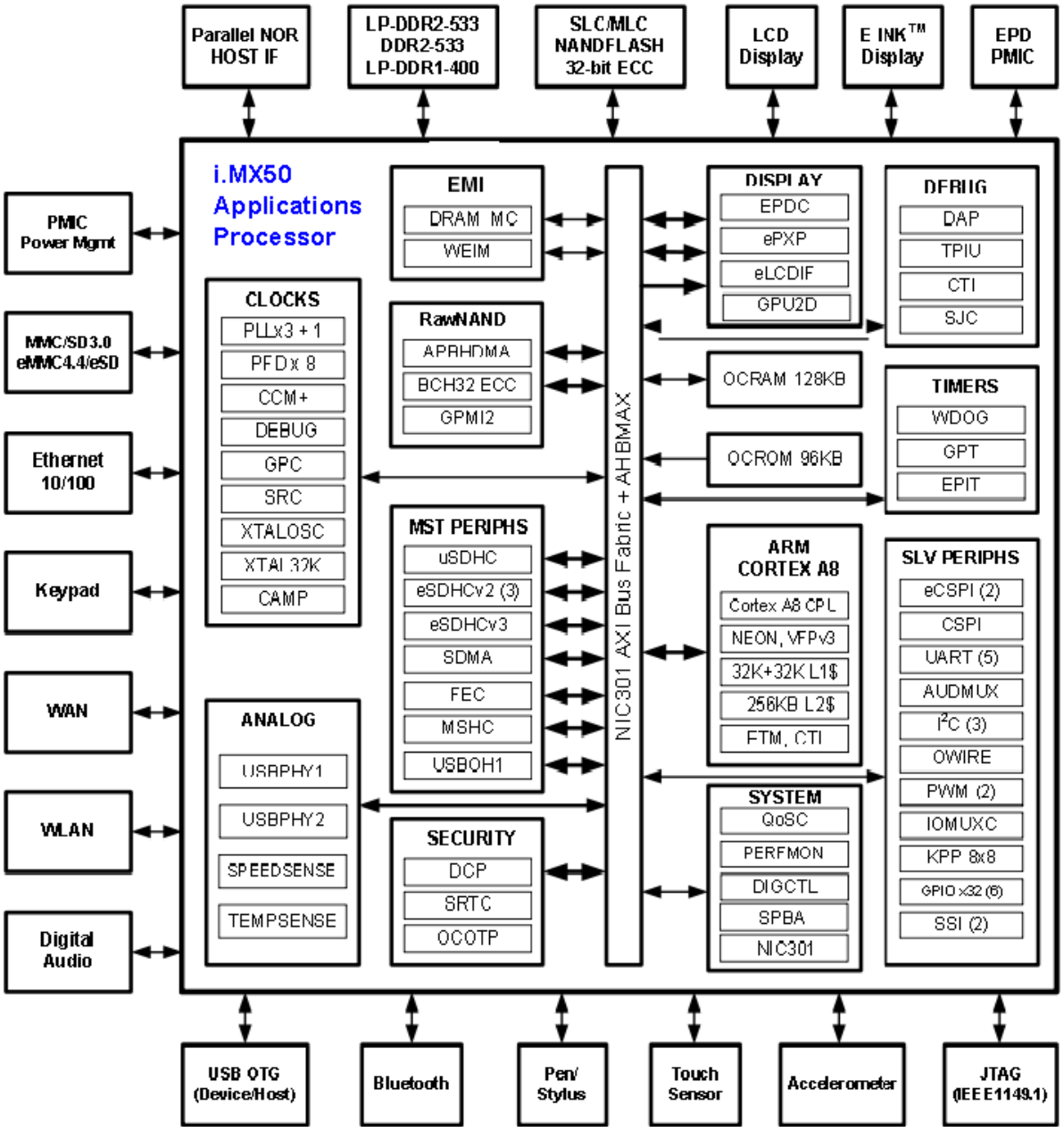

Figure 1. i.MX50 System Block Diagram

Table 4. i.MX50 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
eSDHCv3-3 (eMMC 4.4)	Ultra-High-Speed Multi-Media Card/ Secure Digital card host controller, ver. 3	Master Connectivity Peripherals	Ultra High-Speed eSDHC, enhanced to support eMMC 4.4 standard specification, for 832 Mbps. IP is backward compatible to eSDHCv2 IP. See complete features listing in eSDHCv2 entry below. Port 3 is specifically enhanced to support eMMC 4.4 specification, for double data rate (832 Mbps, 8-bit port).
eSDHCv2-1 eSDHCv2-2 eSDHCv2-4	Enhanced Multi-Media Card/ Secure Digital Host Controller, ver. 2		In Enhanced Multi-Media Card/Secure Digital Host Controller the Ports 1, 2, and 4 are compatible with the *MMC System Specification* version 4.3, full support The generic features of the eSDHCv2 module, when serving as SD/MMC host, include the following: • Can be configured either as SD/MMC controller • Supports eSD and eMMC standard, for SD/MMC embedded type cards • Conforms to *SD Host Controller Standard Specification* version 2.0, full support • Compatible with the SD Memory Card Specification version 1.1 • Compatible with the SDIO Card Specification version 1.2 • Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC and MMC RS cards • Configurable to work in one of the following modes: —SD/SDIO 1-bit, 4-bit —MMC 1-bit, 4-bit, 8-bit • Full/High speed mode • Host clock frequency variable between 32 kHz to 52 MHz • Up to 200 Mbps data transfer for SD/SDIO cards using four parallel data lines • Up to 416 Mbps data transfer for MMC cards using eight parallel data lines
FEC	Fast Ethernet Controller	Master Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support both 10 Mbps and 100 Mbps Ethernet/IEEE Std 802.3™ networks. An external transceiver interface and transceiver function are required to complete the interface to the media.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6	General Purpose I/O Modules	Slave Connectivity Peripherals	These modules are used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit *free-running* or *set* and *forget* mode timer with a programmable prescaler and compare and capture register. A timer counter value can be captured using an external event, and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.

Table 5. Special Signal Considerations (continued)

Signal Name	Remarks
DRAM_OPEN, DRAM_OPENFB (for 416 MAPBGA and 400 MAPBGA)	These pins are the echo gating output and feedback pins used by the DRAM PHY to bound a window around the DQS transition. For an application using a single DRAM device, these pins should be routed so that the trace length (DRAM_OPEN + DRAM_OPENFB) = trace length (DRAM_SDCLK0 + DRAM_SDQS0). For an application using two DRAM devices, they should be routed so that the trace length (DRAM_OPEN + DRAM_OPENFB) = trace length (AVG(DRAM_SDCLK0+DRAM_SDCLK1) + AVG (DRAM_SDQS0_to_Device0 + DRAM_SDQS0_to_Device1)). This connection is required for LPDDR1, LPDDR2, and DDR2. For the i.MX50 PoP package, these signals are connected on the substrate.
DRAM_SDODT0 (for 416 MAPBGA and 400 MAPBGA), DRAM_SDODT1 (for 416 MAPBGA only)	These pins are the On-die termination outputs from the i.MX50. For DDR2, these pins should be connected to the DDR2 DRAM ODT pins. For LPDDR1 and LPDDR2, these pins should be left floating. Note that both SDODT pins are removed on the 416 PoPBGA package, and only SDODT0 exists on the 400 MAPBGA package.
DRAM_CALIBRATION	This pin is the ZQ calibration used to calibrate DRAM Ron and ODT. For LPDDR2, this pin should be connected to ground through a 240 Ω 1% resistor. For DDR2 and LPDDR1, this pin should be connected to ground through a 300 Ω 1% resistor.
JTAG_MOD	This input has an internal 100K pull-up, by default. Note that JTAG_MOD is referenced as SJC_MOD in the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM) - both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. If JTAG port is not needed, the internal pull-up can be disabled in order to reduce supply current to the pin.
JTAG_TCK	This input has an internal 100K pull-down. This pin is in the NVCC_JTAG domain.
JTAG_TDI	This input has an internal 47K pull-up to NVCC_JTAG. This pin is in the NVCC_JTAG domain.
JTAG_TDO	This is a 3-state output with an internal gate keeper enable to prevent a floating condition. An external pull-up or pull-down resistor on JTAG_TDO is detrimental and should be avoided. This pin is in the NVCC_JTAG domain.
JTAG_TMS	This input has an internal 47K pull-up to NVCC_JTAG. This pin is in the NVCC_JTAG domain.
JTAG_TRSTB	This input has an internal 47K pull-up to NVCC_JTAG. This pin is in the NVCC_JTAG domain.
NC	These signals are No Connect (NC) and should be floated by the user.
LOW_BATT_GPIO	If the LOW_BATT_GPIO (UART4_TXD) is asserted at power up, the i.MX50 will boot up at a lower ARM clock frequency to reduce system power. The actual ARM clock frequency used when LOW_BATT_GPIO is asserted is determined by the BT_LPB_FREQ[1:0] pins (220 MHz to 55.3 MHz). The polarity of the LOW_BATT_GPIO is active high by default, but may be set to active low by setting the LOW_BATT_GPIO_LEVEL OTP bit. See the “System Boot” chapter of the Reference Manual for more details. Note that this is not a dedicated pin: LOW_BATT_GPIO appears on the UART4_TXD pin.
PMIC_STBY_REQ	This output may be driven high when the i.MX50 enters the STOP mode to notify the PMIC to enter its low power standby state. This output is in the NVCC_SRTC domain.
PMIC_ON_REQ	This output from the i.MX50 can instruct the PMIC to turn on when the i.MX50 only has NVCC_SRTC power. This may be useful for an alarm application, as it allows the i.MX50 to turn off all blocks except for the RTC and then power on again at a specified time. This output is in the NVCC_SRTC domain.

4.1 Chip-Level Conditions

This section provides the chip-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX50 Chip-Level Conditions

For these characteristics, see	Topic appears ...
Absolute Maximum Ratings	on page 21
13 x 13 mm MAPBGA Package Thermal Resistance Data	on page 22
13 x 13 mm PoPBGA Package Thermal Resistance Data	on page 23
17 x 17 mm MAPBGA Package Thermal Resistance Data	on page 23
Operating Ranges	on page 24
Operating Frequencies	on page 26
Supply Current	on page 26

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 7 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Table 11 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 7. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Peripheral core supply voltage	VCC	–0.3	1.5	V
ARM core supply voltage	VDDGP	–0.3	1.35	V
Bandgap and 480 MHz PLL supply	VDD3P0	–0.5	3.6	V
PLL digital supplies	VDD1P2	–0.3	1.35	V
PLL analog supplies	VDD1P8	–0.3	2.25	V
Efuse, 24 MHz oscillator, 32 kHz oscillator mux supply	VDD2P5	–0.5	2.85	V
Memory array supply	VDDA/VDDAL1	–0.5	1.35	V
Supply voltage (HVIO)	Supplies denoted as I/O supply	–0.5	3.6	V
Supply voltage (GPIO, LVIO)	Supplies denoted as I/O supply	–0.5	3.3	V
Input/output voltage range	V_{in}/V_{out}	–0.5	OVDD + 0.3[1]	V
USB VBUS DC Transient (t<30ms, duty cycle < 0.05%)	VBUS	 — —	 6.00 7.00	V

4.2.1 Power-Up Sequence

Figure 2 shows the power-up sequence.

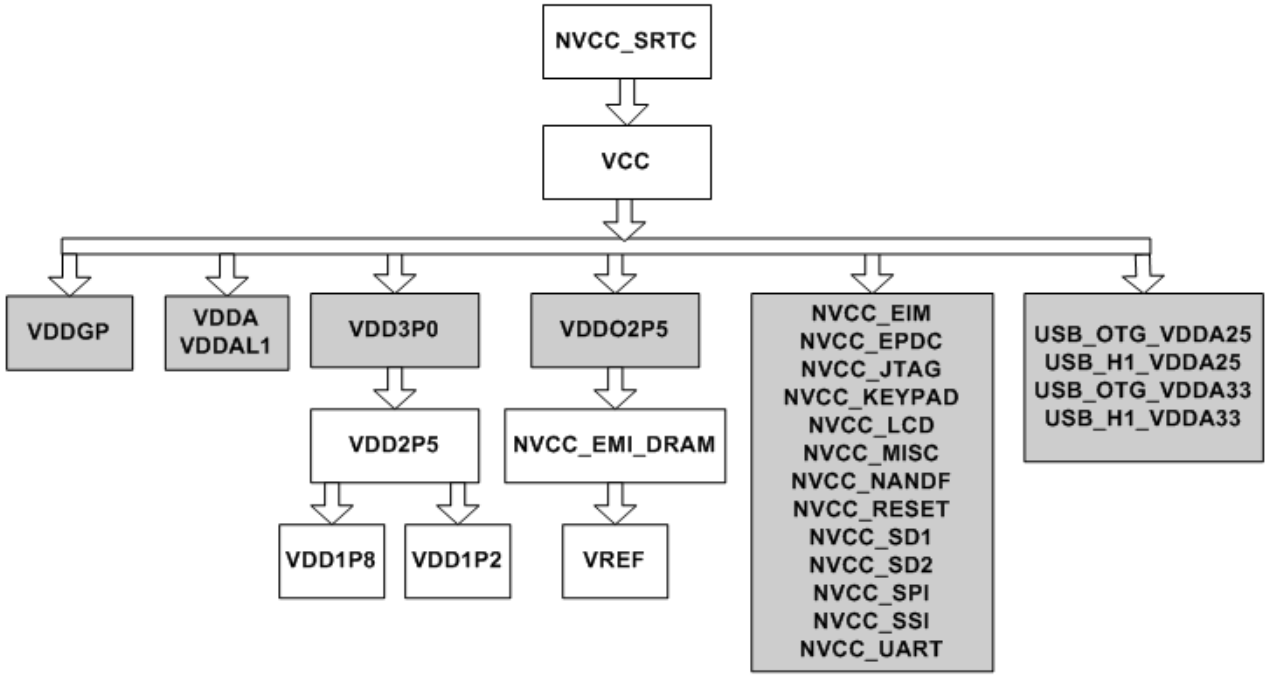

Figure 2. Power-Up Sequence

NOTE

1) The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail is at its working voltage.

2) No power-up sequence dependencies exist between the supplies shown shaded in gray.

4.2.2 Power-Down Sequence

The power-down sequence is recommended to be the opposite of the power-up sequence. In other words, the same power supply constraints exist while powering off as while powering on.

4.2.3 Resume Sequence

When the i.MX50 is resuming from STOP mode, there are some special sequencing considerations. The resume timing is determined by the following internal counters:

1. STBY_COUNT. This register is in the CCM block and may be set to a maximum of 16 x 32 kHz cycles, or 500 µsec.

2. OSCNT. This register is in the CCM block and may be set to a maximum of 256 x 32 kHz cycles, or 8 msec. This counter is intended to give the 24MHz clock time to start up and stabilize.

If the PMIC_RDY input is used and BYPASS_PMIC_VFUNCTIONAL_READY = 0, the i.MX50 will wait for STBY_COUNT cycles after PMIC_STBY_REQ negation before checking PMIC_RDY status. Once the STBY_COUNT has expired AND the PMIC_RDY signal has been asserted, the OSCNT counter begins and the 24MHz oscillator is powered up. After OSCNT expires the processor will enter RUN mode.

If the PMIC_RDY input is not used, the processor will attempt to start the 24 MHz oscillator after STBY_COUNT expires. So at a minimum, all the supplies necessary to start up the 24 MHz oscillator need to be powered before STBY_COUNT expires: NVCC_SRTC,VDD1P2, VDD1P8, VDD2P5, VDD3P0. After STBY_COUNT expires, the OSCNT counter begins and the 24 MHz oscillator is powered up. After OSCNT expires the processor will enter RUN mode, so all other supplies need to be at the appropriate operating levels before OSCNT expires.

4.3 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O and High-Speed General Purpose I/O (GPIO)
- Double Data Rate 2 (DDR2)
- Low Power Double Data Rate 2 (LPDDR2)
- Low Power Double Data Rate 1(LPDDR1)
- Low Voltage I/O (LVIO)
- High Voltage I/O (HVIO)
- Secure Digital Host Controllers (eSDHCv2 and eSDHCv3)
- USB-OTG and USB Host ports

NOTE

The term **OVDD** in this section refers to the associated supply rail of an input or output.

4.3.1 GPIO I/O DC Parameters

The parameters in Table 18 are guaranteed per the operating ranges in Table 11, unless otherwise noted.

Table 18. GPIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	MIN	Typ	MAX	Units
High-level output voltage	Voh	Ioh=-1mA Ioh=spec'ed Drive	OVDD-0.15 0.8*OVDD	—	—	V
Low-level output voltage	Vol	Iol=1mA Iol=specified Drive	—	—	0.15 0.2*OVDD	V

Table 23. HVIO DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	MIN	TYP	MAX	Units
Pull-up resistor (22 KΩ PU)	Rpu	Vi=OVDD/2	22	29	71	KΩ
Pull-up resistor (47 KΩ PU)	Rpu	Vi=OVDD/2	43	59	148	KΩ
Pull-up resistor (100 KΩ PU)	Rpu	Vi=OVDD/2	46	62	156	KΩ
Pull-down resistor (100 KΩ PD)	Rpd	Vi=OVDD/2	53	77	256	KΩ
Input current (no pull-up/down)	IIN	VI = 0 VI=OVDD	—	2.8	470 50	nA
Input current (22 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	153 0.05	μA
Input current (47 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	77 0.05	μA
Input current (100 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	73 0.05	μA
Input current (100 KΩ PD)	IIN	VI = 0 VI=OVDD	—	—	0.47 63	μA
High-level output current, high voltage mode	Ioh_hv	Vol=0.8*OVDD Low Drive Medium Drive High Drive	 -5.1 -10.2 -15.3	—	—	 mA
External pull-up / pull-down resistor required to overdrive internal keeper	Rext	—	—	—	2.5	KΩ

[1] To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s. VIL and VIH do not apply when hysteresis is enabled.

[2] Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.4 Output Buffer Impedance Characteristics

This section defines the I/O impedance parameters of the i.MX50 processor.

4.5 I/O AC Parameters

The load circuit and output transition time waveforms are shown in Figure 4 and Figure 5. The AC electrical characteristics for slow and fast I/O are presented in the Table 27 and Table 28, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bit in the IOMUX control registers.

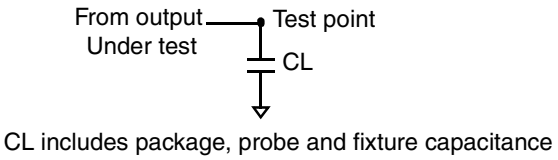

Figure 4. Load Circuit for Output

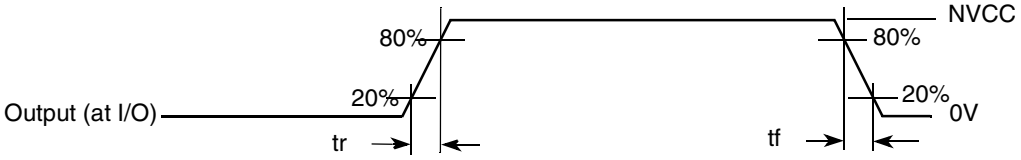

Figure 5. Output Transition Time Waveform

4.5.1 GPIO I/O Slow AC Parameters

Table 27 shows the AC parameters for GPIO slow I/O.

Table 27. GPIO I/O Slow AC Parameters

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF			1.91/1.52 3.07/2.65	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF			2.22/1.81 3.81/3.42	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF			2.88/2.42 5.43/5.02	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF			4.94/4.50 10.55/9.70	ns
Output Pad Slew Rate (Max Drive)[1]	tps	15 pF 35 pF	0.5/0.65 0.32/0.37			V/ns
Output Pad Slew Rate (High Drive)	tps	15 pF 35 pF	0.43/0.54 0.26/0.41			V/ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0.34/0.41 0.18/0.2			V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0.20/0.22 0.09/0.1			V/ns
Output Pad di/dt (Max Drive)	tdit				30	mA/ns

4.5.4 LVIO I/O Fast AC Parameters

Table 30 shows the AC parameters for LVIO fast I/O.

Table 30. LVIO I/O Fast AC Parameters

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF			1.44/1.27 2.78/2.56	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF			1.80/1.61 3.59/3.34	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF			2.55/2.28 5.32/5.01	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF			4.74/4.59 10.59/10.21	ns
Output Pad Slew Rate (Max Drive)[1]	tps	15 pF 35 pF	0.69/0.78 0.36/0.39			V/ns
Output Pad Slew Rate (High Drive)	tps	15 pF 35 pF	0.55/0.61 0.28/0.30			V/ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0.39/0.44 0.19/0.20			V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0.21/0.22 0.09/0.10			V/ns
Output pad di/dt (Max drive)	tdit	—	—	—	70	mA/ns
Output pad di/dt (High drive)	tdit	—	—	—	54	mA/ns
Output pad di/dt (Medium drive)	tdit	—	—	—	35	mA/ns
Output pad di/dt (Low drive)	tdit	—	—	—	18	mA/ns
Input transition times[2]	trm	—	—	—	25	ns

1 tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

2 Hysteresis mode is recommended for inputs with transition time greater than 25 ns.

4.5.5 HVIO I/O Low Voltage (1.8 V) AC Parameters

Table 27 shows the AC parameters for HVIO I/O Low Voltage (1.8 V).

Table 31. HVIO I/O Low Voltage (1.8 V) AC Parameters

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF			1.82/1.97 3.39/3.57	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF			2.48/2.62 4.95/5.14	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF			4.57/4.77 9.60/9.91	ns

4.8.1 DRAM Command & Address Output Timing—DDR2 and LPDDR1

The following diagrams and tables specify the timings related to the address and command pins, which interfaces DDR2 and LPDDR1 memory devices.

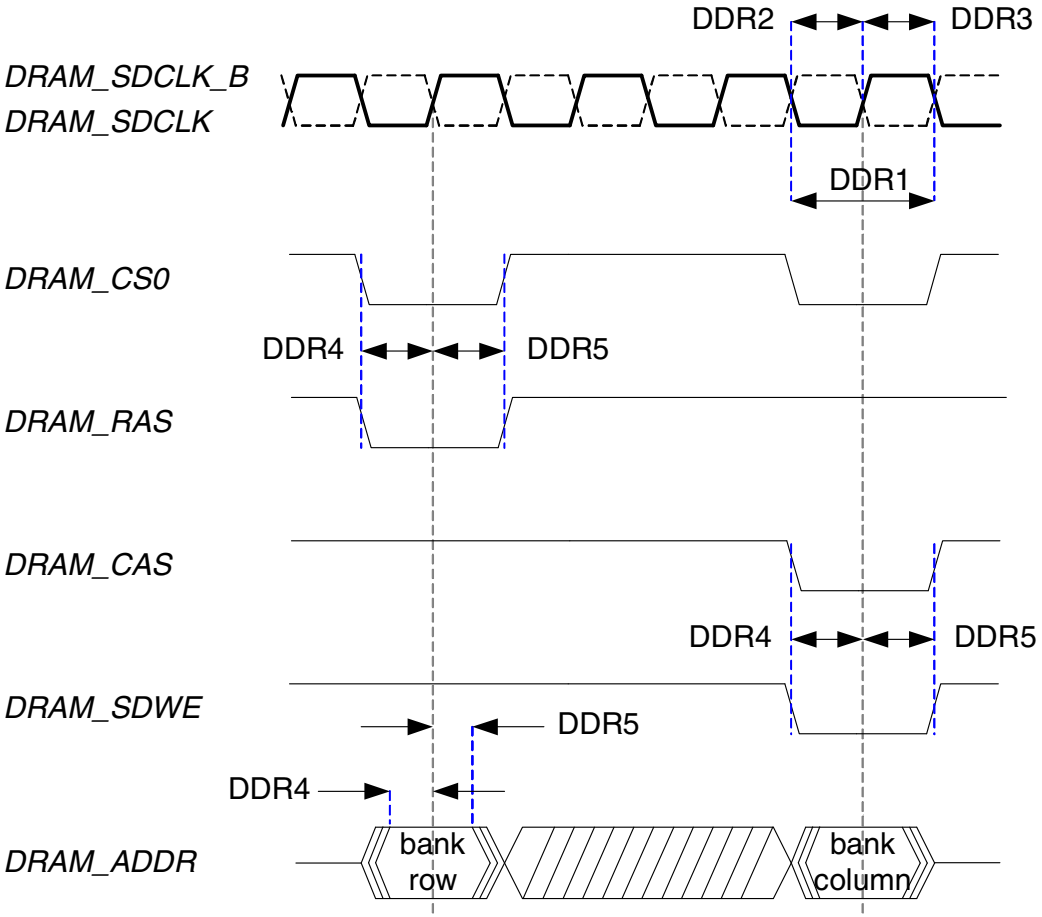

Figure 28. DRAM Command/Address Output Timing—DDR2 and LPDDR1

Table 45. EMI Command/Address AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR1	CK cycle time	tCK	3.75	—	ns
DDR2	CK high level width	tCH	0.48 tCK	0.52 tCK	ns
DDR3	CK low level width	tCL	0.48 tCK	0.52 tCK	ns
DDR4	Address and control output setup time	tIS	0.5 tCK - 0.3	—	ns
DDR5	Address and control output hold time	tIH	0.5 tCK - 0.3	—	ns

Table 47. DDR Output AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR16 CK >= 200 MHz	DQ & DQM output hold time relative to DQS	tDH	0.5 tCK - 1.3	—	ns
DDR15 CK < 200 MHz	DQ & DQM output setup time relative to DQS	tDS	1	—	ns
DDR16 CK < 200 MHz	DQ & DQM output hold time relative to DQS	tDH	1	—	ns

NOTE

The DDR15,16 could be adjusted by the parameter “DLL_WR_DELAY”;

The ideal case is that SDQS is center aligned to the DRAM_D data valid window;

For this table, HW_DRAM_PHY15[14:8] (DLL_WR_DELAY) = 0x10;

4.8.4 DRAM Data Input Timing

DRAM Data input timing is defined for all DDR types: DDR2, LPDDR1, and LPDDR2.

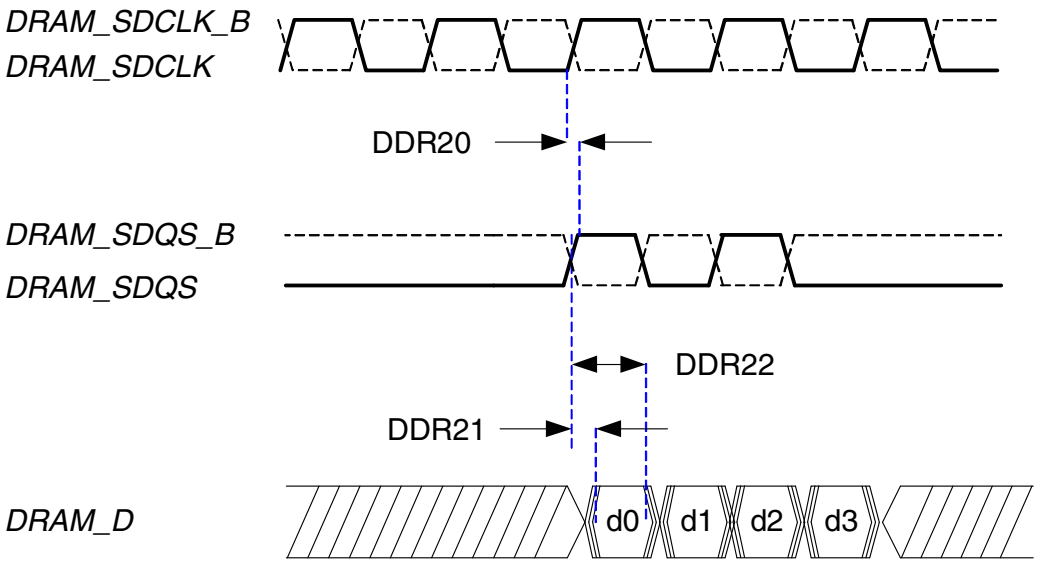

Figure 31. DRAM Data Input Timing

Table 48. DDR2 Input AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR20	Positive DQS latching edge to associated CK edge	tDQSCK	-0.5 tCK	—	ns

Table 59. I²C Module Timing Parameters (continued)

ID	Parameter	Standard Mode Supply Voltage = 1.65 V–1.95 V, 2.7 V–3.3 V		Fast Mode Supply Voltage = 2.7 V–3.3 V		Unit
		Min	Max	Min	Max	
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal.

3 A Fast-mode I²C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2CLK line is released.

4 C_b = total capacitance of one bus line in pF.

4.9.6 One-Wire (OWIRE) Timing Parameters

Figure 42 depicts the RPP timing, and Table 60 lists the RPP timing parameters.

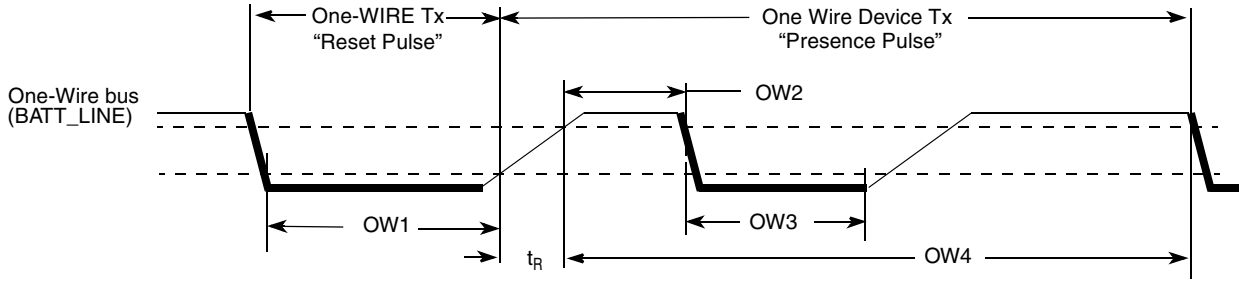

Figure 42. Reset and Presence Pulses (RPP) Timing Diagram

Table 60. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min	Typ	Max	Unit
OW1	Reset Time Low	t_{RSTL}	480	511	—[1]	µs
OW2	Presence Detect High	t_{PDH}	15	—	60	µs
OW3	Presence Detect Low	t_{PDL}	60	—	240	µs
OW4	Reset Time High (includes recovery time)	t_{RSTH}	480	512	—	µs

[1] In order not to mask signaling by other devices on the 1-Wire bus, $t_{RSTL} + t_R$ should always be less than 960 µs.

Figure 43 depicts Write 0 Sequence timing, and Table 61 lists the timing parameters.

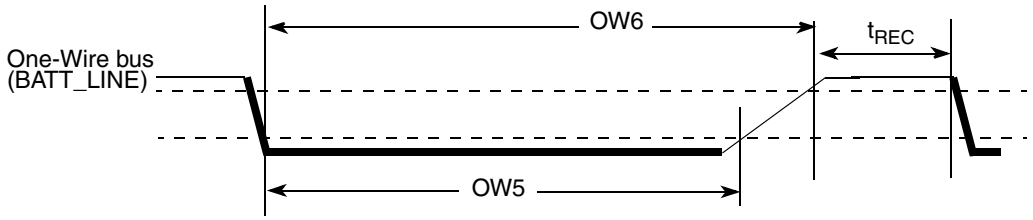

Figure 43. Write 0 Sequence Timing Diagram

Table 61. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Unit
OW5	Write 0 Low Time	t_{LOW0}	60	100	120	µs
OW6	Transmission Time Slot	t_{SLOT}	OW5	117	120	µs
—	Recovery time	t_{REC}	1	—	—	µs

Figure 44 depicts Write 1 Sequence timing, Figure 45 depicts the Read Sequence timing, and Table 62 lists the timing parameters.

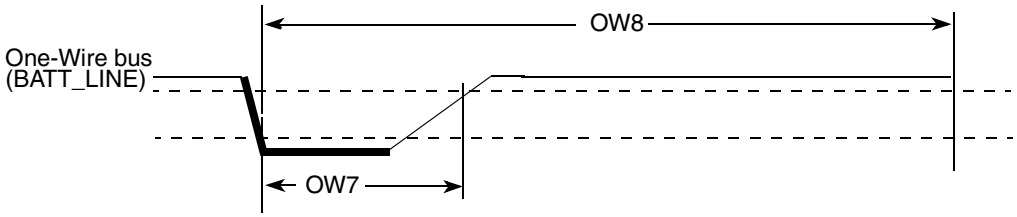

Figure 44. Write 1 Sequence Timing Diagram

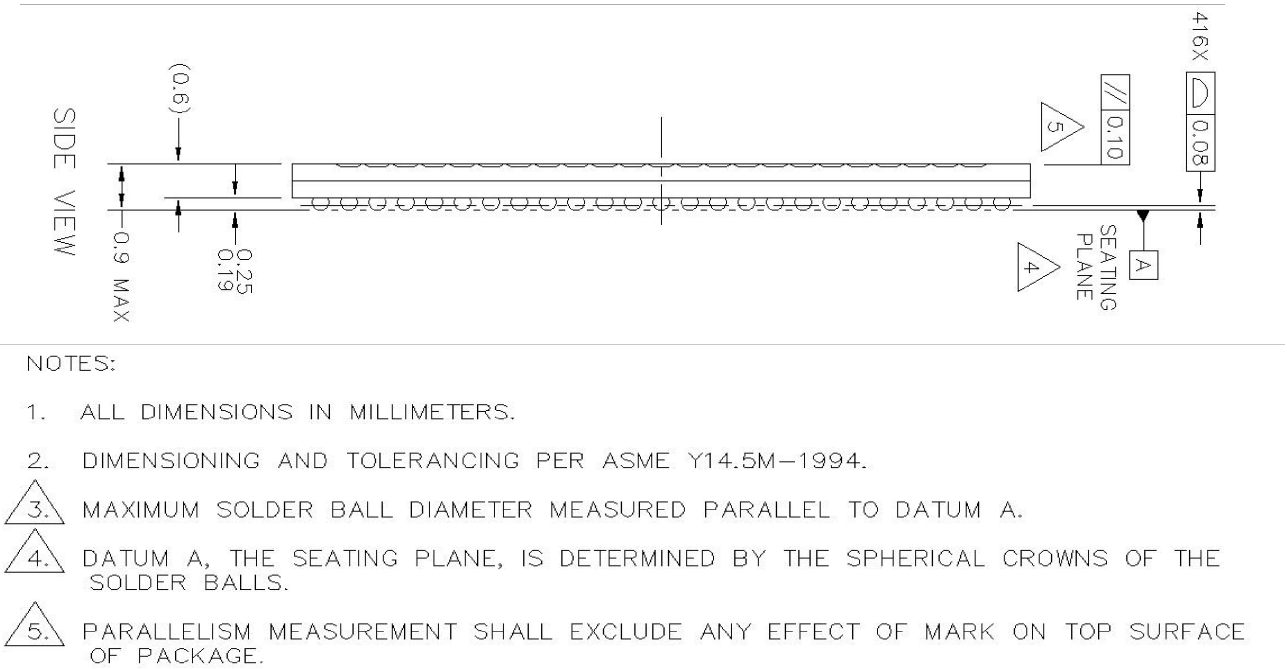

Figure 63. 416 PoPBGA 13 x 13 Package Side View

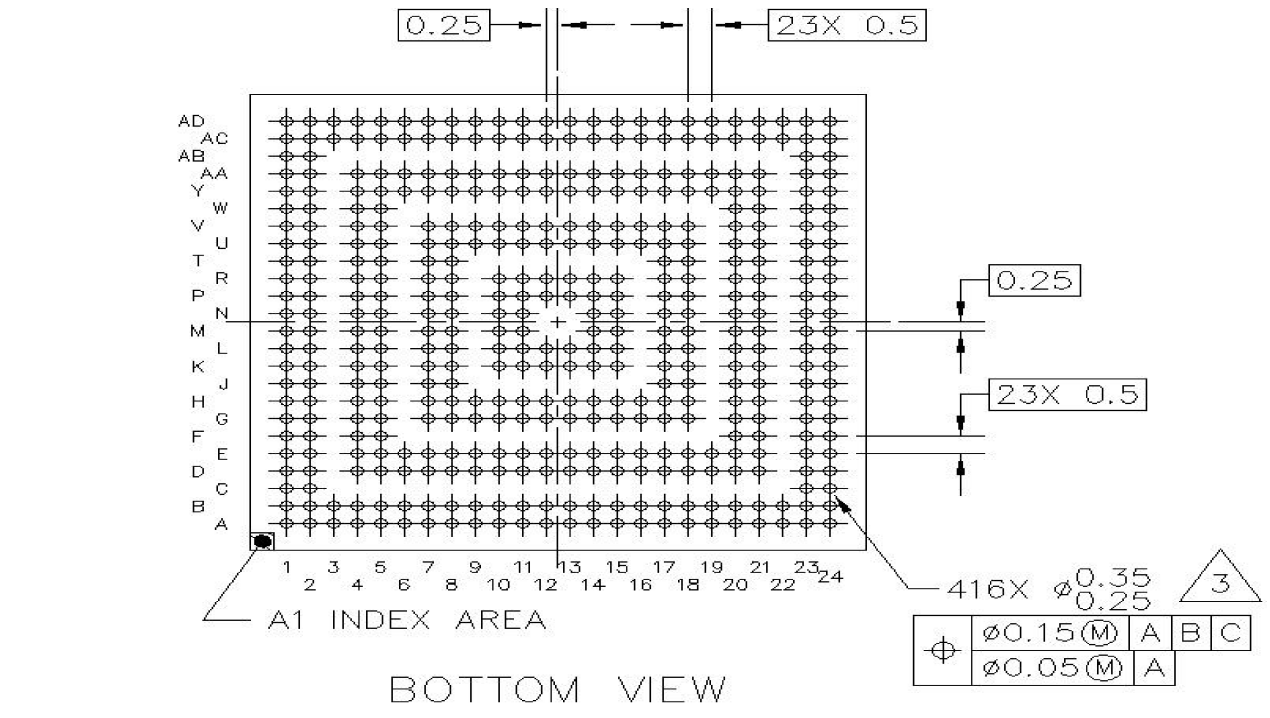

Figure 64. 416 PoPBGA 13 x 13 mm Package Bottom View

The following notes apply to Figure , Figure 63, and Figure 64:

- Unless otherwise specified dimensions are in millimeters.

Table 81. 416 PoPBGA 13 x 13 mm Ball Map (continued)

AA	NVCC_SRTC	VSS	NC	JTAG_TDI	JTAG_TRSTB	CKIH	GND_KEL	USB_OTG_RREFEXT	VSS	USB_H1_RREFEXT	VSS	USB_OTG_ID	USB_OTG_VBUS	USB_OTG_GPANAIO	CHGR_DET_B	USB_H1_VBUS	USB_H1_GPANAIO	VSS	DISP_RESET	DISP_RD	DISP_BUSY	NC	POP_LPDDR2_ZQ1	POP_LPDDR2_ZQ0
AB	BOOT_MODE0	BOOT_MODE1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	DISP_D14	DISP_D5
AC	RESET_IN_B	TEST_MODE	VSS	VSS	EXTAL	VSS	VSS	USB_OTG_DN	USB_VDDA25	USB_H1_DN	USB_VDDA33	SSI_TXFS	SSI_TXC	SSI_RXD	DISP_D3	DISP_D1	DISP_D0	VSS	DISP_D7	DISP_D9	DISP_CS	DISP_D12	DISP_D13	DISP_D4
AD	VSS	POR_B	VDD3P0	VDD2P5	XTAL	VDD1P2	VDD1P8	USB_OTG_DP	USB_VDDA25	USB_H1_DP	USB_VDDA33	SSI_RXC	SSI_RXFS	SSI_TXD	DISP_D2	DISP_D6	DISP_	VSS	DISP_D11	DISP_WR	DISP_D15	DISP_D10	DISP_RS	VSS

5.2.3 416 PoPBGA 13 x 13 mm Power Rails

Table 82 shows the device connection list for ground, power, sense, and reference contact signals. Table 85 displays an alpha-sorted list of the signal assignments including power rails and associated power supplies.

Table 82. 416 PoPBGA 13 x 13 mm Ground, Power, Sense, and Reference Contact Signals

Pin Name	Ball Number	Comments
GND_DCDC	W5	—
NVCC_EIM	N7 M7 M8	—
NVCC_EMI_DRAM	A21, B21, D21, D23, D24, E5, E6, E7, F5, G5, G7, K20, L20, M20, N20, P20, R20, V18, V20, W20, Y18, Y19, Y20	These are the 1.2V supply to both the i.MX50 DRAM controller as well as the PoP LPDDR2.
NVCC_EPDC	M10, N10, P10, R10, U10	—
NVCC_JTAG	U9	—
NVCC_KEYPAD	N8	—
NVCC_LCD	U11	—
NVCC_MISC	P8	—
NVCC_NANDF	V9, V10	—

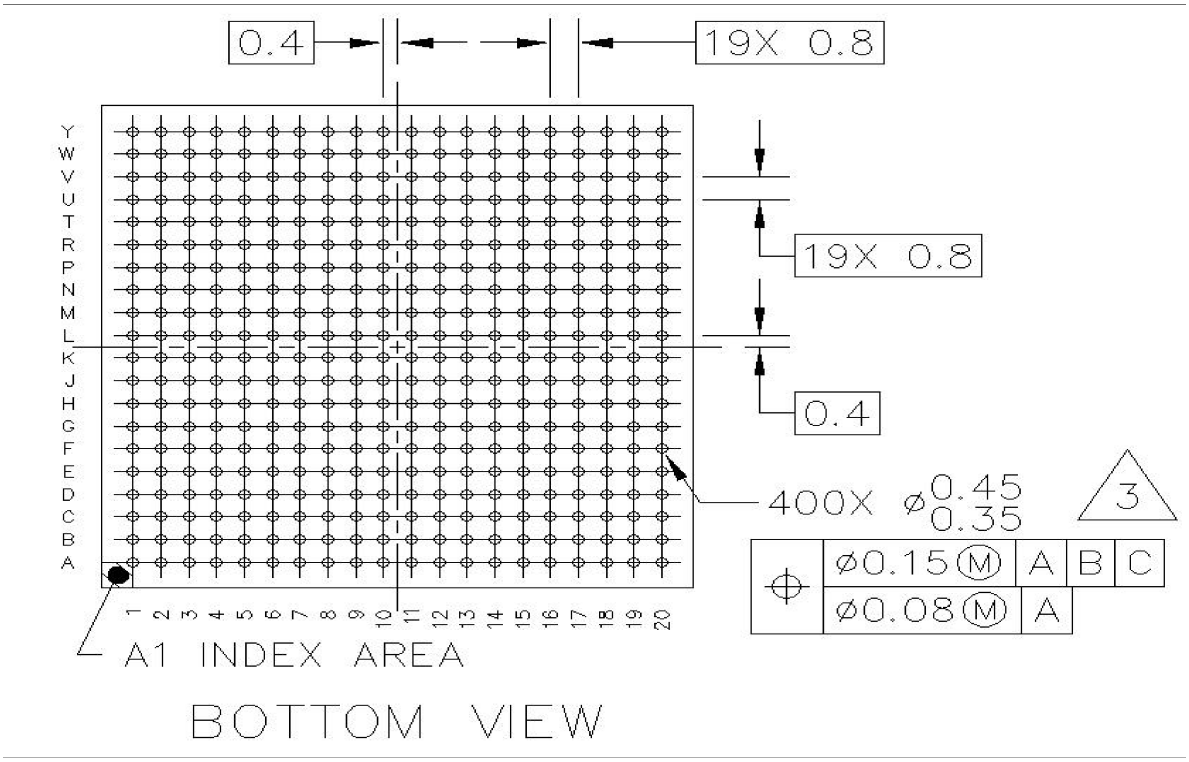

Figure 66. 400 MAPBGA 17x17 mm Package Bottom View

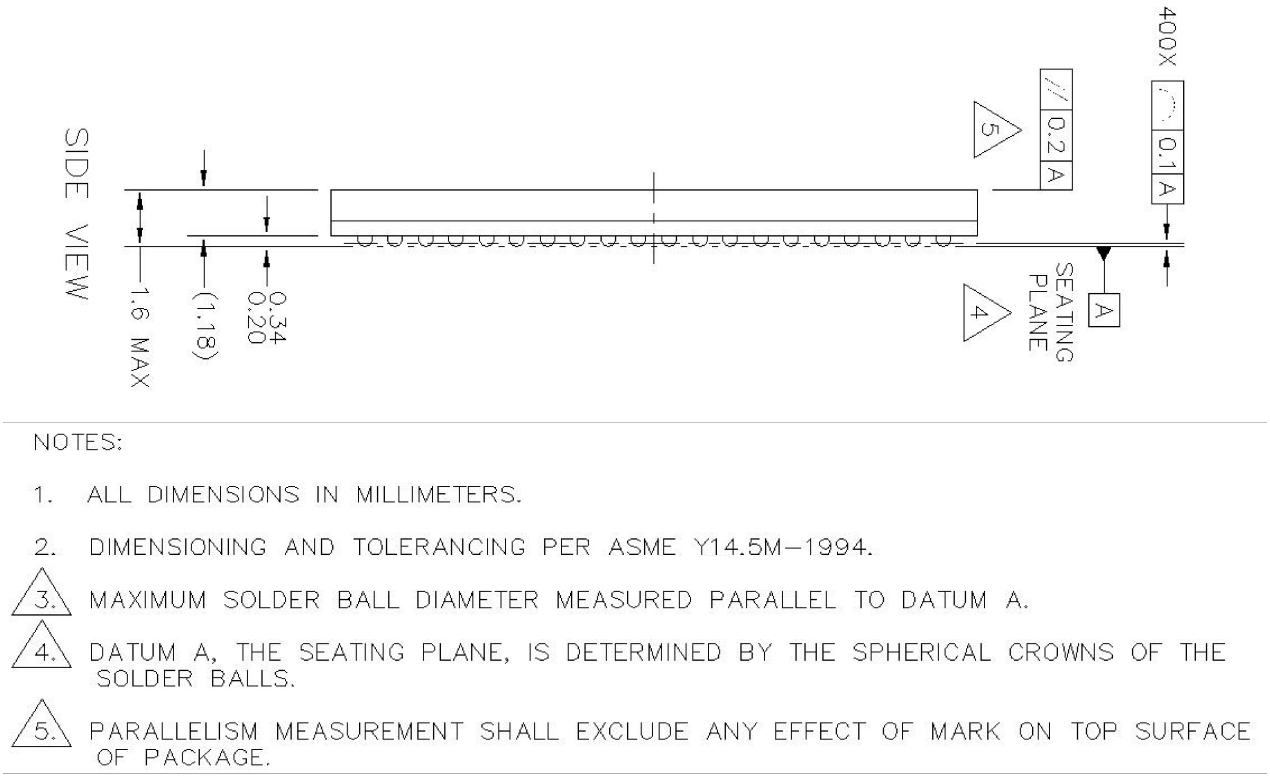

Figure 67. 400 MAPBGA 17x17 mm Package Side View

The following notes apply to Figure 65, Figure 66, and Figure 67:

- Unless otherwise specified dimensions are in millimeters.
- All dimensions and tolerances conform to ASME Y14.5M-1994.
- Parallelism measurement shall exclude any effect of mark on top surface of package.

5.3.2 400 MAPBGA 17 x 17 mm Ball Map

Table 83 shows the 400 MAPBGA 17 x 17 mm ball map.

Table 83. 400 MAPBGA 17 x 17 mm Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	NC	EIM_RDY	EIM_CRE	EIM_EB0	EIM_BCLK	EIM_DA12	EIM_DA8	EPDC_SDSHR	EIM_DA4	EPDC_GDRL	EPDC_GDCLK	EPDC_SDCE1	EPDC_D5	EPDC_D1	EPDC_BDR0	DRAM_D26	DRAM_D28	DRAM_D29	DRAM_D30	NC
B	KEY_COL0	KEY_COL1	EIM_OE	EIM_EB1	EIM_RW	EIM_DA13	EIM_DA9	EIM_DA5	EIM_DA1	EIM_DA0	EIM_CS0	EPDC_SDCE0	EPDC_SDCLK	EPDC_VCOM0	EPDC_D0	EPDC_D2	DRAM_D27	DRAM_D25	DRAM_D24	DRAM_D31

Table 84. 400 MAPBGA 17x17 Ground, Power, Sense, and Reference Contact Signals (continued)

VDD_DCDCI	R7
VDD_DCDCO	T6
GND_DCDC	R6

5.4 Signal Assignments

Table 85. Alphabetical List of Signal Assignments

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
BOOT_MODE0	AB1	AB1	V3	NVCC_RESET	LVIO	ALT0	IN	100K PU
BOOT_MODE1	AB2	AB2	U3	NVCC_RESET	LVIO	ALT0	IN	100K PU
CHGR_DET_B	V11	AA15	T10	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG25	—	OUT-OD	—
CKIH	AA6	AA6	V4	NVCC_JTAG	ANALOG	—	—	—
CKIL	Y1	Y1	Y4	NVCC_SRTC	ANALOG	—	—	—
CSPI_MISO	M5	H2	K4	NVCC_SPI	HVIO	ALT1	IN	Keeper
CSPI_MOSI	M2	J1	L3	NVCC_SPI	HVIO	ALT1	IN	Keeper
CSPI_SCLK	M1	H1	M1	NVCC_SPI	HVIO	ALT1	IN	Keeper
CSPI_SS0	M4	J2	J4	NVCC_SPI	HVIO	ALT1	IN	Keeper
DISP_BUSY	AC12	AA21	U11	NVCC_LCD	HVIO	ALT1	IN	Keeper
DISP_CS	AD14	AC21	T12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D0	AA12	AC17	V11	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D1	Y12	AC16	T11	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D10	Y17	AD22	Y16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D11	V12	AD19	W14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D12	V13	AC22	V14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D13	V14	AC23	T13	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D14	V15	AB23	U14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D15	V16	AD21	Y15	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D2	AA13	AD15	W12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D3	Y13	AC15	W13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D4	AA14	AC24	Y13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D5	Y14	AB24	U13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU