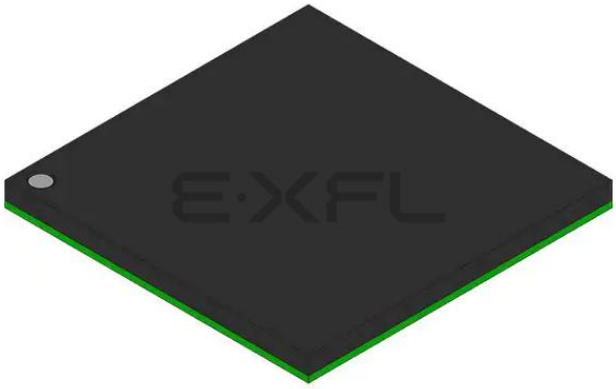

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Boot Security, Cryptography, Secure JTAG
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx507cvm1br2

application chipset, the i.MX50 provides a rich set of interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, and displays.

1.1 Product Overview

The i.MX50 is designed to enable high-tier portable applications by satisfying the performance requirements of advanced operating systems and applications.

1.1.1 Dynamic Performance Scaling

Freescale's dynamic voltage and frequency scaling (DVFS) allows the device to run at much lower voltage and frequency with ample processing capacity for tasks, such as audio decode, resulting in significant power reduction.

1.1.2 Multimedia Processing Powerhouse

The multimedia performance of the i.MX50 processor ARM Cortex-A8 core is boosted by a multi-level cache system, a NEON™ coprocessor with SIMD media processing architecture and 32-bit single-precision floating point support, and two vector floating point coprocessors. The system is further enhanced by a programmable smart DMA (SDMA) controller.

1.1.3 Powerful Display System

The i.MX50 includes support for both standard LCD displays as well as electrophoretic displays (e-paper). The display subsystem consists of the following modules:

- Electrophoretic Display Controller (EPDC) (i.MX508 only)

  The EPDC is a feature-rich, low power, and high-performance direct-drive active matrix EPD controller. It is specifically designed to drive E-INK^{TM} EPD panels, supporting a wide variety of TFT architectures. The goal of the EPDC is to provide an efficient SoC integration of this functionality for e-paper applications, allowing a significant bill of materials cost savings over an external solution while reaching much higher levels of performance and lower power. The EPDC module is defined in the context of an optimized hardware/software partitioning and works in conjunction with the ePXP (see Section 1.1.4, "Graphics Accelerators").
- Enhanced LCD Controller Interface (eLCDIF)

  The eLCDIF is a high-performance LCD controller interface that supports a rich set of modes and allows interoperability with a wide variety of LCD panels, including DOTCK/RGB and smart panels. The module also supports synchronous operation with the ePXP to allow the processed frames to be passed from the ePXP to the eLCDIF through an on-chip SRAM buffer. The eLCDIF can support up to 32-bit interfaces.

1.1.4 Graphics Accelerators

Integrated graphics accelerators offload processing from the ARM processor, enabling high performance graphic applications at minimum power.

- NEON coprocessor (SIMD Media Processing Architecture) and Vector Floating Point (VFP-Lite) coprocessor supporting VFPv3

The memory system consists of the following components:

- Level 1 cache:
  - Instruction (32 Kbyte)
  - Data (32 Kbyte)
- Level 2 cache:
  - Unified instruction and data (256 Kbyte)
- Level 2 (internal) memory:
  - Boot ROM, including HAB (96 Kbyte)
  - Internal multimedia/shared, fast access RAM (128 Kbyte)
- External memory interfaces:
  - 16/32-bit DDR2-533, LPDDR2-533, or LPDDR1-400 up to a total of 2 GByte
  - 8-bit NAND SLC/MLC Flash with up to 100 MHz synchronous clock rate and up to 32-bit hardware ECC for 1 Kbyte block size
  - 16/32-bit NOR Flash with a dedicated 16-bit muxed-mode interface. I/O muxing logic selects EIMv2 port as primary muxing at system boot.
  - 16-bit PSRAM, Cellular RAM
  - Managed NAND, including eMMC up to rev 4.4

The i.MX50 introduces a next generation system bus fabric architecture that aggregates various sub-system buses and masters for access to system peripherals and memories. The various bus-systems and components are as follows:

- 64-bit AXI Fabric (266 MHz)—This bus-fabric is the SoC's central bus aggregation point.
  - Provides access to all slave targets in the SoC:
    - ROM (ROMCP)
    - On-chip RAM (OCRAM)
    - External DRAM (DRAM MC)
    - External static RAM (EIM)
    - Interrupt controller (TZIC)
    - Decode into the AHB MAX crossbar second level AHB fabric.
  - Provides arbitration to the following masters in the system:
    - ARM CPU complex
    - Pixel processing pipeline (ePXP)
    - Electrophoretic display controller (EPDC)
    - eLCDIF LCD display controller
    - DCP Crypto engine
    - BCH ECC engine
    - MAX AHB crossbar

1.4 Part Number Feature Comparison

Table 2 provides an overview of the feature differences between the i.MX50 part numbers.

Table 2. Part Number Feature Comparison

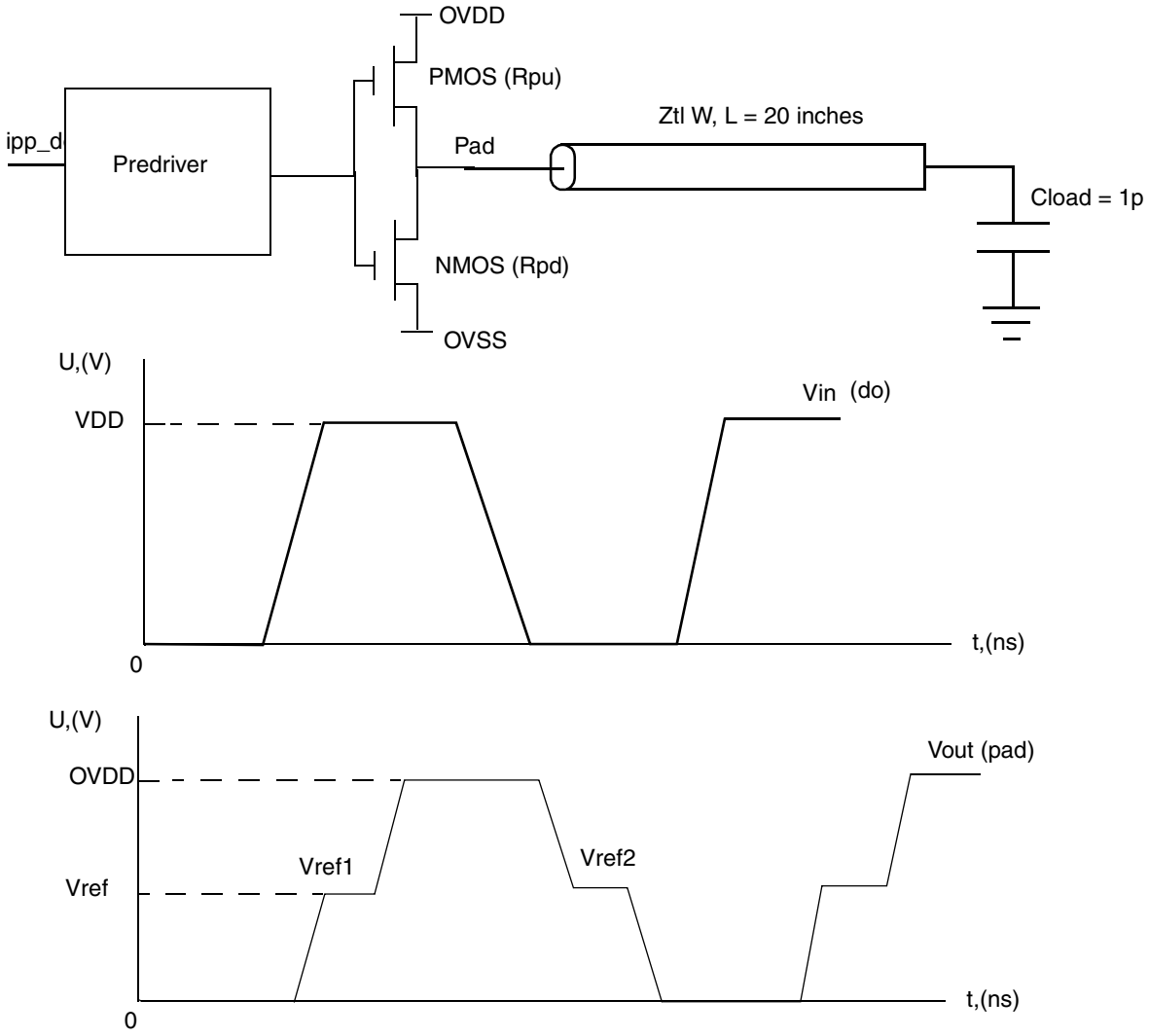
Part Number	Disabled Features	Comments
MCIMX508	None	
MCIMX507	GPU	
MCIMX503	EPDC	The i.MX503 has the same ball map and IOMUX as the i.MX508. The EPDC pins still exist on the i.MX503, but because the EPDC block is disabled, those pins cannot be used for EPDC functionality (ALT0) and must be configured in the IOMUX with another ALT-mode setting.
MCIMX502	GPU, EPDC	The i.MX502 has the same ball map and IOMUX as the i.MX508. The EPDC pins still exist on the i.MX502, but because the EPDC block is disabled, those pins cannot be used for EPDC functionality (ALT0) and must be configured in the IOMUX with another ALT-mode setting.

3.1 Special Signal Considerations

Table 5 lists special signal considerations for the i.MX50. The signal names are listed in alphabetical order. The package contact assignments are found in Section 5, "Package Information and Contact Assignments." The signal descriptions are defined in the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM).

Table 5. Special Signal Considerations

Signal Name	Remarks
BOOT_MODE0, BOOT_MODE1	These two input pins are sampled out of reset and set the boot mode. For Internal boot, they should be set to 00. For Internal Fuse Only boot, they should be set to 10. For USB downloader, they should be set to 11. The BOOTMODE pins are in the NVCC_RESET domain and include an internal 100K pull-up resistor at start-up.
BOOT_CONFIG1[7:0], BOOT_CONFIG2[7:0], BOOT_CONFIG3[7:0]	These 24 pins are the GPIO boot override pins and may be driven at power up to select the boot mode. They are sampled 4 x CKIL clock cycles after POR is de-asserted. Consult the "System Boot" chapter of the Reference Manual for more details. Note that these are not dedicated pins: the BOOT_CONFIG pins appear over 24 pins of the EIM interface.
BT_LPB_FREQ[1:0]	If the LOW_BATT_GPIO (UART4_TXD) is asserted at power up, the BT_LPB_FREQ[1:0] pins will be sampled to determine the ARM core frequency. Consult the "System Boot" chapter of the Reference Manual for more details. Note that these are not dedicated pins: BT_LPB_FREQ0 appears on SSI_TXFS and BT_LPB_FREQ1 appears on SSI_TXC.
CHGR_DET_B	This is the USB Charger Detect pin. It is an open drain output pin that expects a 100 K pull-up. This pin is asserted low when a USB charger is detected on the OTG PHY DP and DM. This detection occurs with the application of VBUS. This pin is a raw sensor output and care must be taken to follow the system timings outlined in the USB charger specification Rev 1.1. The maximum current leakage at this pin is 8.5 μA. This pin can be controlled by software control as well. If not used, this pin should be tied to ground or left floating.
CKIH	This is an input to the CAMPs (Clock Amplifiers), which include on-chip AC-coupling precluding the need for external coupling capacitors. The CAMPs are enabled by default, but the main clocks feeding the on-chip clock tree are sourced from XTAL/EXTAL by default. Optionally, the use of a low jitter external oscillators to feed CKIH (while not required) can be an advantage if low jitter or special frequency clock sources are required by modules sourced by CKIH. See CCM chapter in the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM) for details on the respective clock trees. After initialization, the CAMPs may be disabled if not used by programming the CCR CAMPx_EN field. If disabled, the on-chip CAMP output is low and the input is irrelevant. CKIH is on the NVCC_JTAG power domain, so the input clock amplitude should not exceed NVCC_JTAG. If unused, the user should tie CKIH to GND for best practice.
CKIL/ECKIL	The user must tie a fundamental mode 32.768 K crystal across ECKIL and CKIL. The target ESR should be 50 K or less. The bias resistor for the amplifier is integrated and approximately 14 MΩ. The target load capacitance for the crystal is approximately 10 pF. The load capacitors on the board should be slightly less than double this value after taking parasitics into account. While driving in an external 32 KHz signal into ECKIL, CKIL should be left floating so that it biases. A differential amplifier senses these two pins to propagate the clock inside the i.MX508. Care must be taken to minimize external leakages on ECKIL and CKIL. If they are significant to the 14 MΩ feedback or 1 μA, then loss of oscillation margin or cessation of oscillation may result.



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 3. Impedance Matching Load for Measurement

Table 40. Asynchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T[2] = GPMI Clock Cycle[3]		Example Timing for GPMI Clock ≈ 100MHz T = 10ns		Unit
			Min.	Max.	Min.	Max.	
NF5	$\overline{WE}$ pulse width	tWP	DS*T		10		ns
NF6	ALE setup time	tALS	(AS+1)*T	—	10	—	ns
NF7	ALE hold time	tALH	(DH+1)*T	—	20	—	ns
NF8	Data setup time	tDS	DS*T	—	10	—	ns
NF9	Data hold time	tDH	DH*T	—	10	—	ns
NF10	Write cycle time	tWC	(DS+DH)*T		20		ns
NF11	$\overline{WE}$ hold time	tWH	DH*T		10		ns
NF12	Ready to $\overline{RE}$ low	tRR	(AS+1)*T	—	10	—	ns
NF13	$\overline{RE}$ pulse width	tRP	DS*T	—	10	—	ns
NF14	READ cycle time	tRC	(DS+DH)*T	—	20	—	ns
NF15	$\overline{RE}$ high hold time	tREH	DH*T		10	—	ns
NF16	Data setup on read	tDSR	N/A		10	—	ns
NF17	Data hold on read	tDHR	N/A		10	—	ns

1 GPMI's Async Mode output timing could be controlled by module's internal register, say HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers' setting. In the above table, we use AS/DS/DH representing these settings each.

2 T represents for the GPMI clock period.

3 AS minimum value could be 0, while DS/DH minimum value is 1.

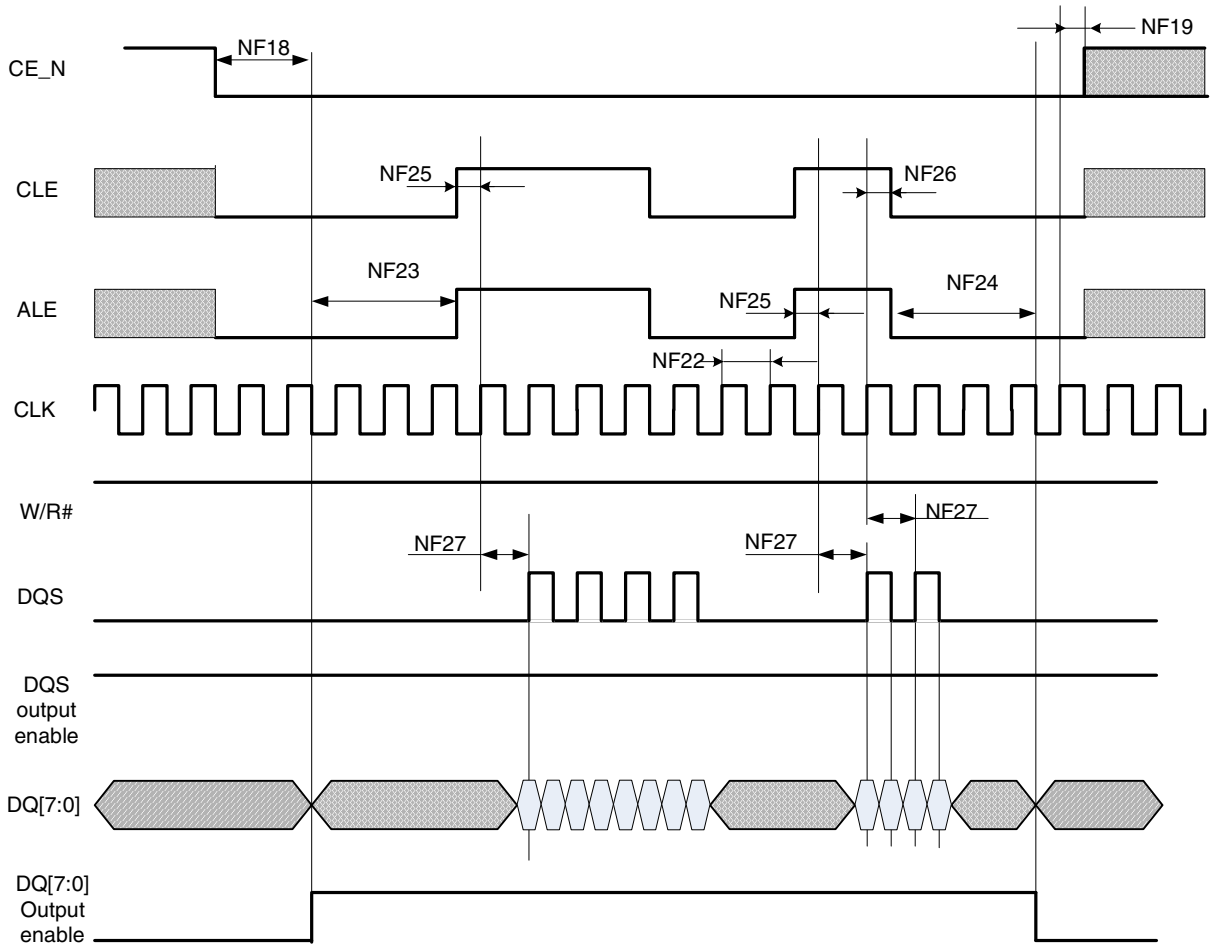


Figure 13. Source Synchronous Mode Data Write Timing Diagram

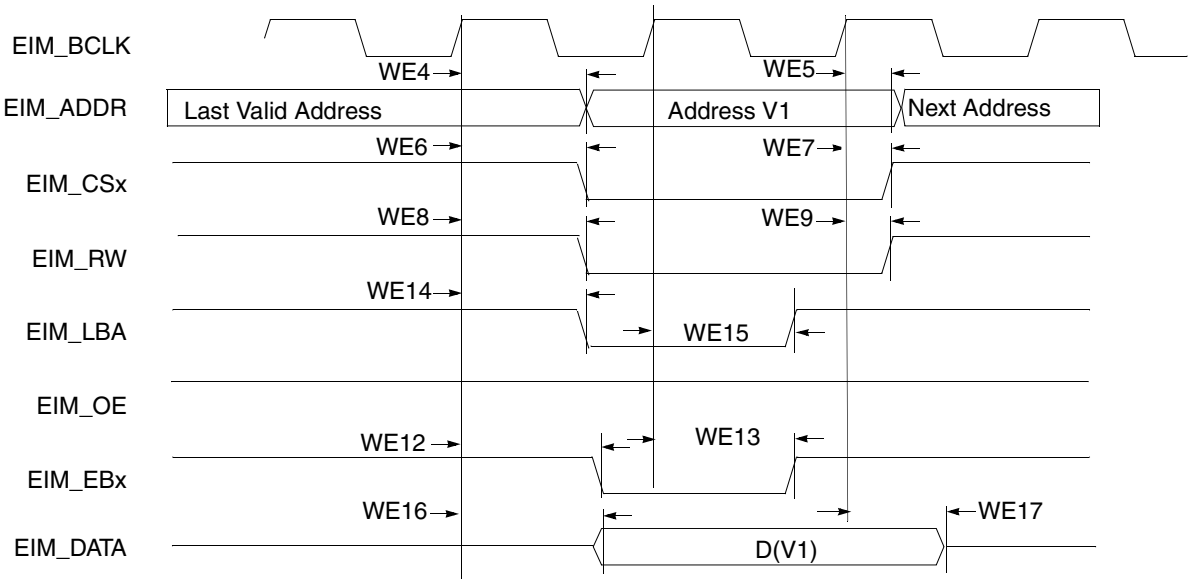


Figure 20. Synchronous Memory, Write Access, WSC=1, WBEA=1, WBEN=1, and WADVN=0

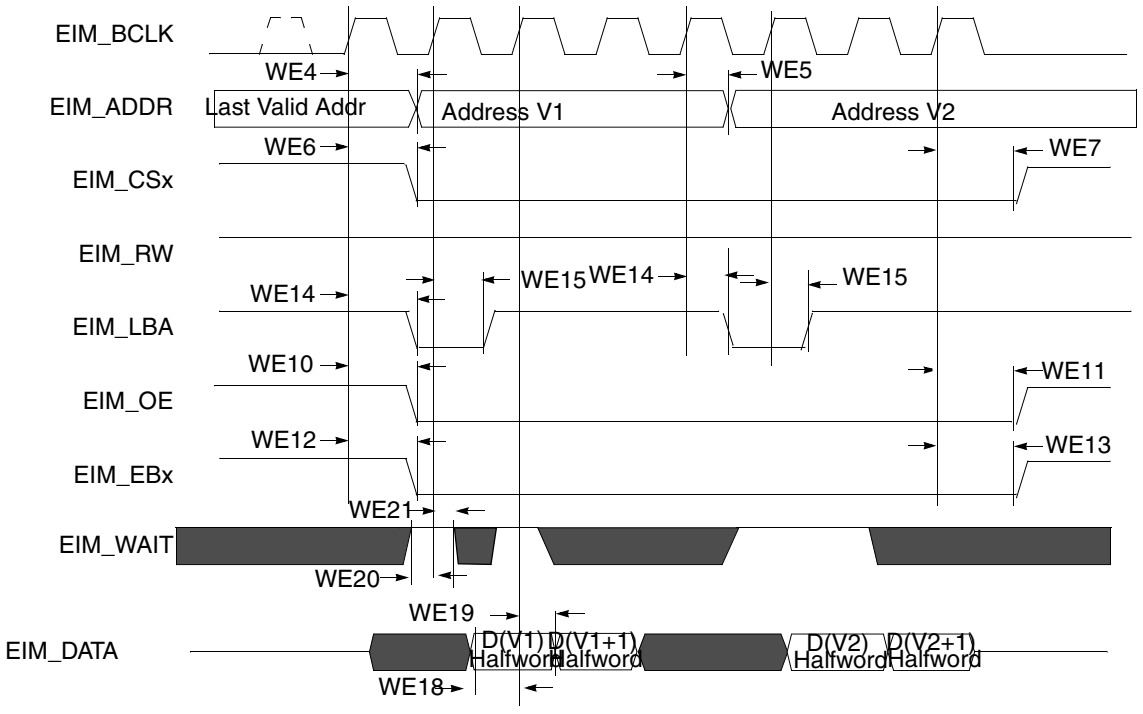


Figure 21. Synchronous 16-Bit Memory, Two Non-Sequential 32-Bit Read Accesses, WSC=2, SRD=1, BCD=0

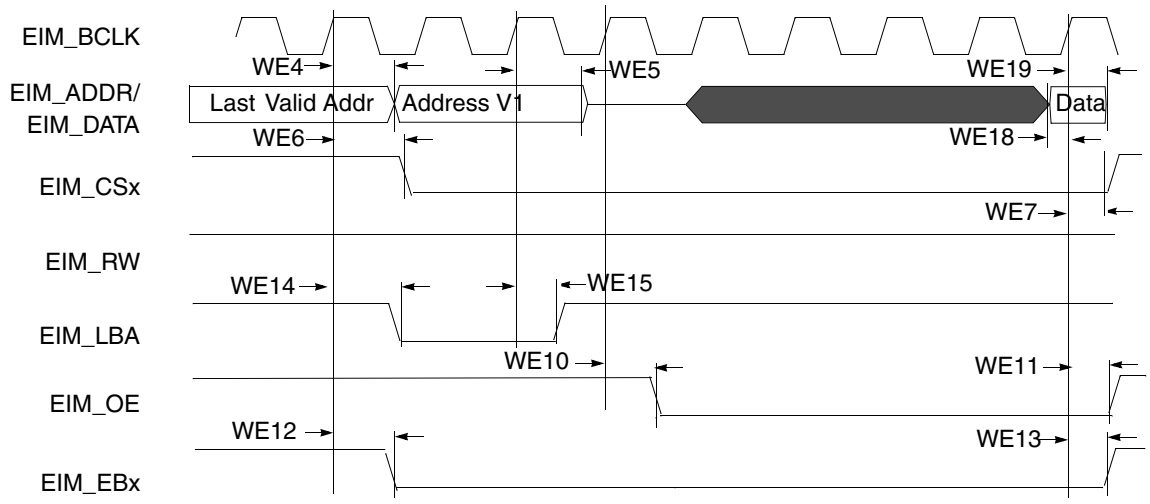


Figure 24. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=2

Figure 25, Figure 26, Figure 27, and Table 44 help to determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

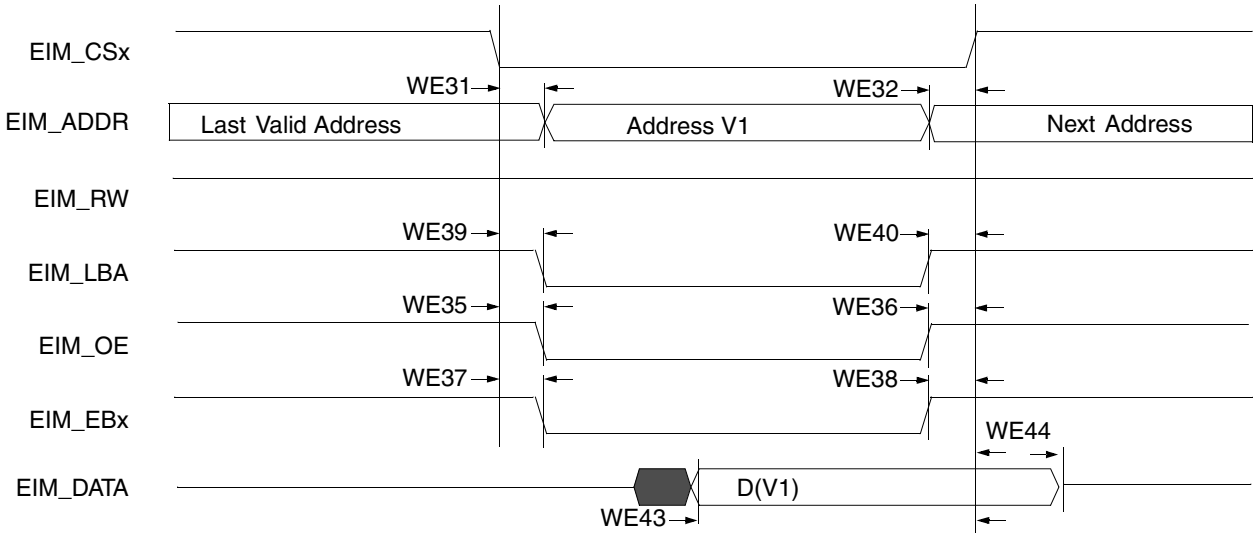


Figure 25. Asynchronous Memory Read Access

4.9.2.1 CSPI Master Mode Timing

Figure 32 depicts the timing of CSPI in master mode and Table 50 lists the CSPI master mode timing characteristics.

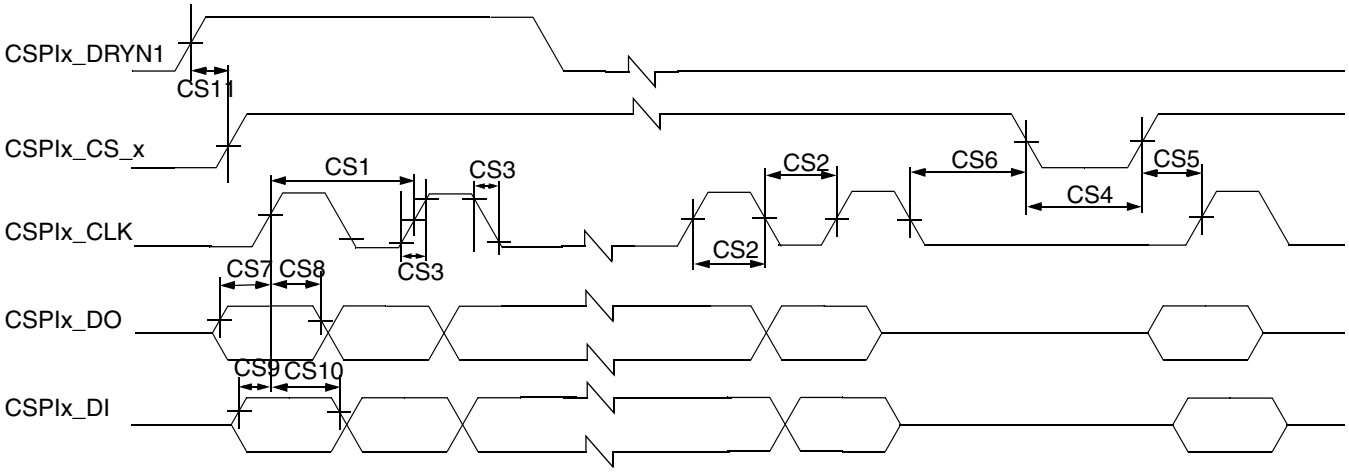


Figure 32. CSPI Master Mode Timing Diagram

Table 50. CSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	CSPIx_CLK Cycle Time	t_{clk}	60	—	ns
CS2	CSPIx_CLK High or Low Time	t_{SW}	6	—	ns
CS3	CSPIx_CLK Rise or Fall	$t_{RISE/FALL}$	—	—	ns
CS4	CSPIx_CS_x pulse width	t_{CSLH}	15	—	ns
CS5	CSPIx_CS_x Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	CSPIx_CS_x Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	CSPIx_DO Setup Time	t_{Smosi}	5	—	ns
CS8	CSPIx_DO Hold Time	t_{Hmosi}	5	—	ns
CS9	CSPIx_DI Setup Time	t_{Smiso}	5	—	ns
CS10	CSPIx_DI Hold Time	t_{Hmiso}	5	—	ns
CS11	CSPIx_DRYN Setup Time	t_{SDRY}	5	—	ns

Table 59. I²C Module Timing Parameters (continued)

ID	Parameter	Standard Mode Supply Voltage = 1.65 V–1.95 V, 2.7 V–3.3 V		Fast Mode Supply Voltage = 2.7 V–3.3 V		Unit
		Min	Max	Min	Max	
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal.

3 A Fast-mode I²C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2CLK line is released.

4 C_b = total capacitance of one bus line in pF.

4.9.6 One-Wire (OWIRE) Timing Parameters

Figure 42 depicts the RPP timing, and Table 60 lists the RPP timing parameters.

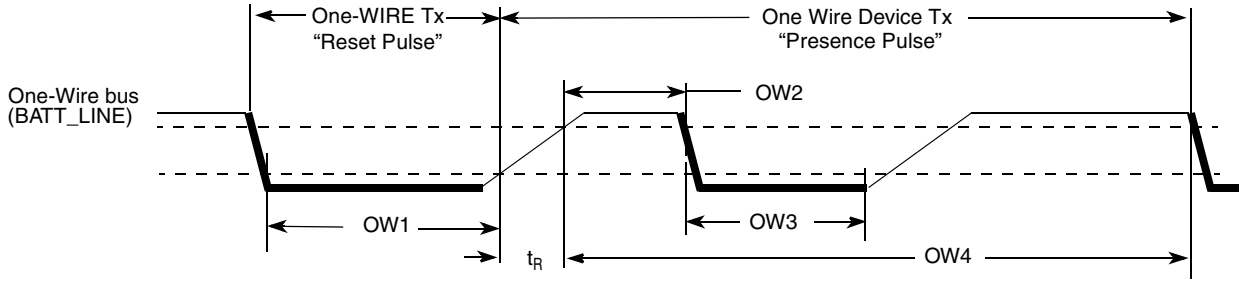


Figure 42. Reset and Presence Pulses (RPP) Timing Diagram

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in both the tables and figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- Tx and Rx refer to the transmit and receive sections of the SSI.
- The terms WL and BL refer to word length (WL) and bit length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.9.10 UART I/O Configuration and Timing Parameters

The following sections describe the UART I/O configuration and timing parameters.

4.9.10.1 UART RS-232 I/O Configuration in Different Modes

Table 70 shows the UART I/O configuration based on which mode is enabled.

Table 70. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
RTS	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
CTS	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
TXD_MUX	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
RXD_MUX	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.9.10.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.9.11 USB PHY Parameters

This section describes the USB OTG PHY and the USB host port PHY parameters.

4.9.11.1 USB PHY AC Parameters

Table 75 lists the AC timing parameters for USB PHY.

Table 75. USB PHY AC Timing Parameters

Parameter	Conditions	Min	Typ	Max	Unit
trise	1.5Mbps 12Mbps 480Mbps	75 4 0.5	—	300 20	ns
tfall	1.5Mbps 12Mbps 480Mbps	75 4 0.5	—	300 20	ns
Jitter	1.5Mbps 12Mbps 480Mbps	—	—	10 1 0.2	ns

4.9.11.2 USB PHY Additional Electrical Parameters

Table 76 lists the parameters for additional electrical characteristics for USB PHY.

Table 76. Additional Electrical Characteristics for USB PHY

Parameter	Conditions	Min	Typ	Max	Unit
Vcm DC (dc level measured at receiver connector)	HS Mode LS/FS Mode	–0.05 0.8	—	0.5 2.5	V
Crossover Voltage	LS Mode FS Mode	1.3 1.3	—	2 2	V
Power supply ripple noise (analog 3.3 V)	< 160 MHz	–50	0	50	mV
Power supply ripple noise (analog 2.5 V)	< 1.2 MHz > 1.2 MHz	–10 –50	0 0	10 50	mV
Power supply ripple noise (Digital 1.2 V)	All conditions	–50	0	50	mV

4.9.11.3 USB PHY System Clocking (SYSCLK)

Table 77 lists the USB PHY system clocking parameters

Table 77. USB PHY System Clocking Parameters

Parameter	Conditions	Min	Typ	Max	Unit
Clock deviation	Reference Clock frequency 24 MHz	–150	—	150	ppm
Rise/fall time	—	—	—	200	ps

5.1.2 416 MAPBGA 13 x 13 mm, 0.5 mm Pitch Ball Map

Table 79 shows the 416 MAPBGA 13 x 13 mm, 0.5 mm pitch ball map.

Table 79. 416 MAPBGA 13x13 mm, 0.5 mm Pitch Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
A	VSS	EIM_RDY	EIM_CRE	EIM_EB0	EIM_BCLK	EIM_DA12	EIM_DA8	EIM_DA4	EIM_DA0	EPDC_SDSHR	EPDC_GDCLK	EPDC_GDRL	EPDC_SDCLK	EPDC_D12	EPDC_D8	EPDC_D4	EPDC_D0	VSS	DRAM_D30	DRAM_D29	NVCC_EMI_DRAM	DRAM_D26	DRAM_D25	VSS	A
B	KEY_COL0	KEY_COL1	EIM_OE	EIM_EB1	EIM_RW	EIM_DA13	EIM_DA9	EIM_DA5	EIM_DA1	EIM_CS0	EPDC_GDOE	EPDC_GDSP	EPDC_SDCLKN	EPDC_D13	EPDC_D9	EPDC_D5	EPDC_D1	VSS	DRAM_D31	DRAM_D28	NVCC_EMI_DRAM	DRAM_D27	DRAM_D24	DRAM_DQM3	B
C	KEY_COL2	KEY_COL3	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	DRAM_SDQS3	DRAM_SDQS3_B	C
D	KEY_ROW0	KEY_ROW1	NC	KEY_ROW2	EIM_WAIT	EIM_DA14	EIM_DA10	EIM_DA6	EIM_DA2	EIM_CS1	EPDC_SDCE4	EPDC_SDCE2	EPDC_SDCE0	EPDC_D14	EPDC_D10	EPDC_D6	EPDC_D2	EPDC_SDLE	EPDC_SDOED	EPDC_VCOM1	NVCC_EMI_DRAM	NC	NVCC_EMI_DRAM	NVCC_EMI_DRAM	D
E	I2C1_SCL	I2C1_SDA	NC	KEY_ROW3	EIM_LBA	EIM_DA15	EIM_DA11	EIM_DA7	EIM_DA3	EIM_CS2	EPDC_SDCE5	EPDC_SDCE3	EPDC_SDCE1	EPDC_D15	EPDC_D11	EPDC_D7	EPDC_D3	EPDC_SDOE	EPDC_SDOEZ	EPDC_BDR0	EPDC_BDR1	NC	DRAM_D15	DRAM_D14	E
F	I2C2_SCL	I2C2_SDA	NC	PWM2	PWM1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	DRAM_A14	DRAM_A13	NC	DRAM_D12	DRAM_D13	F
G	I2C3_SCL	I2C3_SDA	NC	EPITO	WDOG	NC	OWIRE	VDDGP	VDDGP	VDDGP	EPDC_PWRCOM	EPDC_PWRCTRL0	EPDC_PWRCTRL1	EPDC_PWRCTRL2	EPDC_PWRCTRL3	EPDC_PWRSTAT	EPDC_VCOM0	DRAM_SDODT0	NC	VSS	VSS	NC	VSS	DRAM_D10	G

Table 79. 416 MAPBGA 13x13 mm, 0.5 mm Pitch Ball Map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
AB	BOOT_MODE0	BOOT_MODE1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	DRAM_SDQS2	DRAM_SDQS2_B	AB
AC	RESET_IN_B	TEST_MODE	GND3P0	GND2P5	EXTAL	GND1P2	GND1P8	USB_OTG_DN	USB_OTG_VDDA25_1	USB_H1_DN	USB_H1_VDDA33	DISP_BUSY	DISP_RS	DISP_RESET	SD3_D0	SD3_D1	SD3_D2	VSS	DRAM_D16	DRAM_D18	NVCC_EMI_DRAM	DRAM_D20	DRAM_D22	DRAM_DQM2	AC
AD	VSS	POR_B	VDD3P0	VDD2P5	XTAL	VDD1P2	VDD1P8	USB_OTG_DP	USB_H1_VDDA25_1	USB_H1_DP	USB_OTG_VDDA33	DISP_WR	DISP_RD	DISP_CS	SD3_WP	SD3_CLK	SD3_CMD	VSS	DRAM_D17	DRAM_D19	NVCC_EMI_DRAM	DRAM_D21	DRAM_D23	VSS	AD

5.1.3 416 MAPBGA 13 x 13 Power Rails

Table 80. 416 MAPBGA 13x13 Ground, Power, Sense, and Reference Contact Signals

Pin Name	Ball Number	Comments
GND_DCDC	W5	—
NVCC_EIM	L7, M7, M8	—
NVCC_EMI_DRAM	A21, AA21, AA23, AA24, AC21, AD21, B21, D21, D23, D24, K21, K23, K24, R21, R23, R24	—
NVCC_EPDC	M10, N10, P10, R10, U10	—
NVCC_JTAG	U9	—
NVCC_KEYPAD	N8	—
NVCC_LCD	U11	—
NVCC_MISC	P8	—
NVCC_NANDF	V9, V10	—
NVCC_RESET	V8	—
NVCC_SD1	T7	—
NVCC_SD2	U8	—
NVCC_SPI	R7	—

Table 82. 416 PoPBGA 13 x 13 mm Ground, Power, Sense, and Reference Contact Signals (continued)

VDD2P5	AD4	—
VDD3P0	AD3	—
VDDA	P17, R17	—
VDDAL1	P15, R15	—
VDDGP	G10, G8, G9, H10, H7, H8, H9, J7, J8, K10, K7, K8, L10, L7, L8	—
VDDO25	N23	—
VSS	A1, A24, AA11, AA18, AA2, AA9, AC18, AC3, AC4, AC6, AC7, AD1, AD18, AD24, E17, E18, E21, E8, E9, F21, G11, G12, G13, G21, G23, H11, H12, H13, K11, K12, K13, L11, L12, L13, L14, L17, M11, M14, M15, M17, N11, N14, N15, N17, P11, P12, P13, P14, R11, R12, R13, R14, T17, U12, U13, U14, U15, U16, U17	—

5.3 17 x 17 mm, 0.8 mm Pitch, 400 Pin MAPBGA Package Information

This section contains the outline drawing, signal assignment map, ground, power, reference ID (by ball grid location) for the 17 x 17 mm, 0.8 mm pitch, 400 pin MAPBGA package.

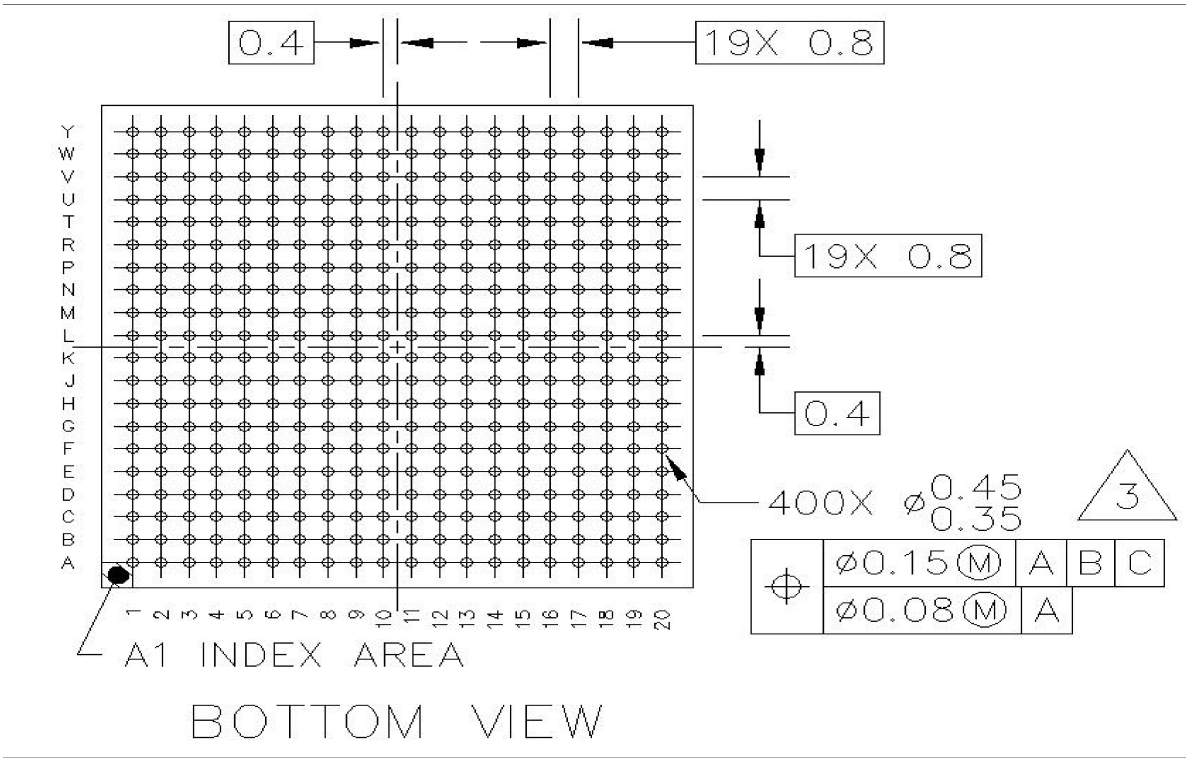


Figure 66. 400 MAPBGA 17x17 mm Package Bottom View

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
DRAM_DQM0	T24	M18	N17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_DQM1	J24	L18	F17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_DQM2	AC24	Y16	U20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_DQM3	B24	G17	D20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_OPEN	J18	—	H18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_OPENFB	H18	—	H17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_RAS	H21	—	E20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	Keeper
DRAM_SDBA0	K18	—	J20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDBA1	L18	—	H20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDBA2	N18	—	M19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDCKE	U20	T5	R18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDCLK_0	N24	R5	J17	NVCC_EMI_DRAM	DRAMCLK	ALT0	OUT-LO	Keeper
DRAM_SDCLK_0_B	M24	P5	J18	NVCC_EMI_DRAM	DRAMCLK	ALT0	OUT-HI	—
DRAM_SDCLK_1	T20	—	—	NVCC_EMI_DRAM	DRAMCLK	ALT0	OUT-LO	Keeper
DRAM_SDCLK_1_B	R20	—	—	NVCC_EMI_DRAM	DRAMCLK	ALT0	OUT-HI	—
DRAM_SDODT0	G18	—	K18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDODT1	R18	—	—	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDQS0	P23	N18	M17	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS0_B	P24	P18	M18	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS1	L23	J20	G17	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS1_B	L24	K18	G18	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS2	AB23	Y15	T19	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS2_B	AB24	V15	T20	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS3	C23	E16	C19	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS3_B	C24	G16	C20	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDWE	P18	—	L18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	Keeper
ECKIL	Y2	Y2	W4	NVCC_SRTC	ANALOG	—	—	—
ECSPI1_MISO	N7	K4	M3	NVCC_SPI	HVIO	ALT1	IN	Keeper
ECSPI1_MOSI	N2	N4	M4	NVCC_SPI	HVIO	ALT1	IN	Keeper

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
EPDC_PWRCTRL2	G14	F23	E12	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_PWRCTRL3	G15	L21	F15	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_PWRSTAT	G16	F24	C12	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE0	D13	N24	B12	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE1	E13	P24	A12	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE2	D12	H21	C11	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE3	E12	J21	E8	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE4	D11	K21	D10	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE5	E11	D18	E6	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCLK	A13	K24	B13	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCLKN	B13	L24	D12	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDLE	D18	M24	C15	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDOE	E18	V21	C13	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDOED	D19	R23	G16	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDOEZ	E19	U21	F16	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDSHR	A10	H23	A8	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_VCOM0	G17	H24	B14	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_VCOM1	D20	W21	G15	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPITO	G4	D8	F5	NVCC_MISC	HVIO	ALT1	IN	Keeper
EXTAL	AC5	AC5	W6	VDD2P5	ANALOG	—	—	—
GND_KEL	AA7	AA7	T7	VDD2P5	ANALOG	—	—	—
I2C1_SCL	E1	A6	E1	NVCC_MISC	HVIO	ALT1	IN	Keeper
I2C1_SDA	E2	B7	E2	NVCC_MISC	HVIO	ALT1	IN	Keeper
I2C2_SCL	F1	A5	F1	NVCC_MISC	HVIO	ALT1	IN	Keeper
I2C2_SDA	F2	B6	F2	NVCC_MISC	HVIO	ALT1	IN	Keeper
I2C3_SCL	G1	A4	G1	NVCC_MISC	HVIO	ALT1	IN	Keeper
I2C3_SDA	G2	B5	G2	NVCC_MISC	HVIO	ALT1	IN	Keeper
JTAG_MOD	V7	V5	T8	NVCC_JTAG	GPIO	ALT0	IN	100K PU
JTAG_TCK	W4	W4	R8	NVCC_JTAG	GPIO	ALT0	IN	100K PD

Table 86. i.MX50 Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 1	10/2011	• Table 5, "Special Signal Considerations," on page 17 changed CHRG_DET_B to CHGR_DET_B. • Table 5, "Special Signal Considerations," on page 17 in the CHGR_DET_B signal remarks, added “The maximum current leakage at this pin is 8.5 μA.” • Table 5, "Special Signal Considerations," on page 17 in the JTAG_MOD remarks, changed “pull-down” to “pull-up, by default” and added “If JTAG port is not needed, the internal pull-up can be disabled in order to reduce supply current to the pin.” • Table 14, "Maximum Supply Current Consumption—ARM CLK = 800 MHz," on page 27 in the 11th row under the Supply column, changed VDDO2P5 to VDDO25. • Table 78, "VBUS Comparators Thresholds," on page 101 changed CHRG_DET_B to CHGR_DET_B. • Table 5, "Special Signal Considerations," on page 17 for 416 MAPBGA, DRAM_SDCLK_0 pin number was changed to N24 and DRAM_SDCLK_0_B pin number was changed to M24. • Table 5, "Special Signal Considerations," on page 17 for 416 MAPBGA, DRAM_SDCLK_1 pin number was changed to T20 and DRAM_SDCLK_1_B pin number was changed to R20. • Table 5, "Special Signal Considerations," on page 17 for 416 MAPBGA, DRAM_SDQS0 pin number was changed to P23 and DRAM_SDQS0_B pin number was changed to P24. • Table 5, "Special Signal Considerations," on page 17 changed pad type of pin DRAM_CALIBRATION to DRAMCALIB. • Table 5, "Special Signal Considerations," on page 17 changed pad type of pins DRAM_SDCLK_0, DRAM_SDCLK_0_B, DRAM_SDCLK_1, DRAM_SDCLK_1_B, DRAM_SDQS0, DRAM_SDQS0_B, DRAM_SDQS1, DRAM_SDQS1_B, DRAM_SDQS2, DRAM_SDQS2_B, DRAM_SDQS3, and DRAM_SDQS3_B to DRAMCLK.
Rev. 0	07/2011	Initial release.