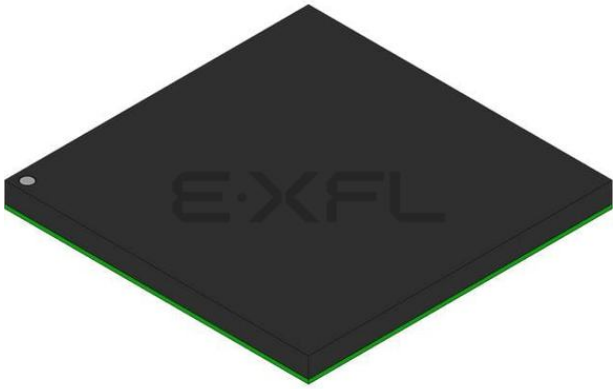

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	EPDC, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Boot Security, Cryptography, Secure JTAG
Package / Case	416-LFBGA
Supplier Device Package	416-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx508cvk8b

- Pixel Processing Pipeline (ePXP)

  The ePXP is a high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma mapping, and rotation. The ePXP is enhanced with features specifically for grayscale applications working in conjunction with the electrophoretic display controller to form a full grayscale display solution. In addition, the ePXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated LCD controller (eLCDIF).
- Graphics acceleration

  The i.MX50 provides a 2D graphics accelerator with performance up to 200 Mpix/s.

1.1.5 Multilevel Memory System

The multilevel memory system of the i.MX50 is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The i.MX50 supports many types of external memory devices, including DDR2, LPDDR2, LPDDR1, NOR Flash, PSRAM, Cellular RAM, NAND Flash (MLC and SLC) and OneNAND™, and managed NAND including eMMC up to rev. 4.4.

1.1.6 Smart Speed™ Technology

The i.MX50 device has power management throughout the SOC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart Speed technology enables the designer to deliver a feature-rich product that requires levels of power that are far less than industry expectations.

1.1.7 Interface Flexibility

The i.MX50 supports connection to a variety of interfaces, including an LCD controller for displays, two high-speed USB on-the-go-capable PHYs, multiple expansion card ports (high-speed MMC/SDIO host and others), 10/100 Ethernet controller, and a variety of other popular interfaces (for example, UART, I^2C, and I^2S serial audio).

1.1.8 Advanced Security

The i.MX50 delivers hardware-enabled security features, such as High-Assurance Boot 4 (HAB4) for signed/authenticated firmware images, basic DRM support with random private keys and AES encryption/decryption, and storage and programmability of on-chip fuses.

1.2 Features

The i.MX50 applications processor is based on the ARM Cortex-A8 platform and has the following features:

- MMU, L1 instruction cache, and L1 data cache
- Unified L2 cache
- 800 MHz or 1 GHz target frequency of the core (including NEON, VFPv3, and L1 cache)

  - GPU 2D
  - SDMA
  - USBOH1 (USB OTG and host controller complex)
  - FEC Ethernet controller
- MAX AHB crossbar (133 MHz)—This connects the various AHB bus sub-segments in the system and provides decode into the following slaves:
  - IP-Bus 1 (66 MHz)—This bus segment contains peripherals accessible by the ARM core and without DMA capability
  - IP-Bus 2 (66 MHz)—This bus segment contains peripherals accessible by the ARM core and without DMA capability
  - APBH DMA bridge (133 MHz)—The APBH DMA bridge is a master to the MAX for its memory-side DMA operations. The APBH bus is an AMBA APB slave bus providing peripheral access to many of the high-speed IP blocks on the i.MX50.
- IP-Bus 3 (66 MHz)—This third peripheral bus segment contains peripherals accessible by the ARM core and SDMA and as such houses peripherals with DMA capability. The IP-Bus 3 can be accessed by the ARM CPU through IP-Bus 1 and SPBA.
- Quality of service controller (QoSC)—This provides both soft and dynamic arbitration/priority control. The QoSC works in conjunction with the critical display modules such as the eLCDIF and EPDC to provide dynamic priority control, based on real-time metrics.

The i.MX50 makes use of dedicated hardware accelerators to achieve state-of-the-art multimedia performance. The use of hardware accelerators provides both high performance and low power consumption, while freeing up the CPU core for other tasks.

The i.MX50 incorporates the following hardware accelerators:

- GPU2Dv1—2D Graphics accelerator, OpenVG 1.1, 200 Mpix/s performance
- ePXP—enhanced PiXel Processing Pipeline off loading key pixel processing operations required to support both LCD and EPD display applications

The i.MX50 includes the following interfaces to external devices:

NOTE

Not all the interfaces are available simultaneously depending on I/O multiplexer configuration.

- Displays:
  - EPDC (i.MX508 Only)—Supporting direct-driver TFT backplanes beyond 2048 × 1536 at 106 Hz refresh (or 4096 × 4096 at 20 Hz)
  - eLCDIF—Supporting beyond SXGA + (1400 × 1050) at 60 Hz resolutions with up to a 32-bit display interface
  - On the i.MX508, both displays can be active simultaneously. If both displays are active, the eLCDIF only provides a 16-bit interface due to pin muxing.
- Expansion cards:
  - Four SD/MMC card

Table 4. i.MX50 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SDMA	Smart Direct Memory Access	Master Connectivity Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by offloading various cores in dynamic data routing. The SDMA features list is as follows: • Powered by a 16-bit instruction-set micro-RISC engine • Multi-channel DMA supports up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM Cortex-A8 and SDMA • Very fast context-switching with two-level priority-based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle uni-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers for EMI • Support of byte-swapping and CRC calculations • A library of scripts and API is available
SJC	Secure JTAG Controller	System Control Peripherals	The Secure JTAG Controller provides a mechanism for regulating JTAG access, preventing unauthorized JTAG usage while allowing JTAG access for manufacturing tests and software debugging. The i.MX50 JTAG port provides debug access to several hardware blocks including the ARM processor and the system bus, therefore, it must be accessible for initial laboratory bring-up, manufacturing tests and troubleshooting, and for software debugging by authorized entities. However, if the JTAG port is left unsecured it provides a method for executing unauthorized program code, getting control over secure applications, and running code in privileged modes. The Secure JTAG controller provides three different security modes that can be selected through an e-fuse configuration to prevent unauthorized JTAG access.
SPBA	Shared Peripheral Bus Arbiter	System Control Peripherals	SPBA (Shared Peripheral Bus Arbiter) is a two-to-one IP bus interface (IP bus) arbiter.
SRTC	Secure Real Time Clock	Security Peripherals	The SRTC incorporates a special System State Retention Register (SSRR) that stores system parameters during system shutdown modes. This register and all SRTC counters are powered by dedicated supply rail NVCC_SRTC. The NVCC_SRTC can be energized separately even if all other supply rails are shut down. This register is helpful for storing warm boot parameters. The SSRR also stores the system security state. In case of a security violation, the SSRR marks the event (security violation indication).

Table 5. Special Signal Considerations (continued)

Signal Name	Remarks
USB_H1_VBUS, USB_OTG_VBUS	These inputs are used by the i.MX50 to detect the presence and level of USB 5 V. If either VBUS input pin is connected to an external USB connector, there is a possibility that a fast 5 V edge rate during a cable attach could trigger the VBUS input ESD protection, which could result in damage to the i.MX50 silicon. To prevent this, the system should use some circuitry to prevent the 5 V edge rate from exceeding 5.25 V / 1 μs. Freescale recommends the use of a low pass filter consisting of 100 Ω resistor in series and a 1 μF capacitor close to the i.MX50 pin. In the case when the USB interface is connected on an on-board USB device (for example, 3G modem), the corresponding USB_VBUS pin may be left floating.
VREF	This pin is the DRAM MC reference voltage input. For LPDDR2 and DDR2, this pin should be connected to ½ of NVCC_EMI_DRAM. For LPDDR1, this pin should be left floating. The user may generate VREF using a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_EMI_DRAM. Shunt each resistor with a closely-mounted 0.1 μF capacitor.
WDOG_B	This output can be used to reset the system PMIC when the i.MX50 processor is locked up. This output is in the NVCC_MISC domain.
WDOG_RST_B_DEB	This output may be used to drive out the internal system reset signal to the system reset controller. This is only intended for debug purposes.
XTAL/EXTAL	These pins are the 24 MHz crystal driver as well as the external 24 MHz clock input. If using these pins to directly drive a 24 MHz crystal: • The user should tie a 24 MHz fundamental-mode crystal across XTAL and EXTAL. • The crystal must be rated for a maximum drive level of 100 μW or higher. • The recommended crystal ESR (equivalent series resistance) is 80 Ω or less. If using these pins as a clock input from an external 24 MHz oscillator: • The crystal may be eliminated and EXTAL driven directly driven by the external oscillator. The clock signal level on EXTAL must swing from NVCC_SRTC to GND. • In this configuration, the XTAL pin must be floated and the COSC_EN bit (bit 12 in the CCR register in the Clock Control Module) must be cleared to put the on-chip oscillator circuit in bypass mode which allows EXTAL to be externally driven. • Note there are strict jitter requirements if using an external oscillator in a USB application: < 50 ps peak-to-peak below 1.2 MHz and < 100 ps peak-to-peak above 1.2 MHz for the USB PHY.

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics of the i.MX50 processor.

NOTE

These electrical specifications are preliminary. These specifications are not fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications are published after thorough characterization and device qualifications have been completed.

Table 15. Maximum Supply Current Consumption—ARM CLK = 1 GHz

Condition	Supply	Voltage (V)	Current (mA)	Power (mW)
• T_a = 70°C • ARM core in Run mode • ARM CLK = 1GHz • SYS CLK = 266 MHz • AHB CLK = 133 MHz • DDR CLK = 266 MHz • All voltages operating at maximum levels • External (MHz) crystal and on-chip oscillator enabled • All modules enabled	VDDGP	1.35	1000	1350
	VCC	1.275	220	280.5
	VDDA/VDDAL1	1.35	40	54
	VDD1P2	1.3	15	19.5
	VDD1P8	1.95	3	5.9
	VDD2P5[1]	2.75	2	5.5
	VDD3P0	3.3	2	6.6
	NVCC_EMI_DRAM	1.95	8.3	16.17
	VDD_DCDCi	1.95	0.021	0.041
	USB_OTG_VDDA33 + USB_H1_VDDA33	3.6	10.8	38.8
	VDDO25 + USB_OTG_VDDA25 + USB_H1_VDDA25	2.75	12.45	34.239
	NVCC_RESET	3.1	0.226	0.701
	NVCC_SRTC	1.3	0.0035	0.0045
	Total	—	—	1812

1 During eFuse programming, the maximum current on VDD2P5 will exceed these values. See Table 13 on page 26 for the maximum VDD2P5 current during eFuse programming.

Table 16. Stop Mode Current and Power Consumption [1]

Supply	Voltage (V)	Current (mA)	
		Typical, T_a = 25°C	Max, T_a = 25°C
VDDGP	0.85	0.057	0.198
VCC	0.95	0.544	1.890
VDDA/VDDAL1	0.95	0.071	0.247

1 The typical power, at Ta = 25°C, will be < 1 mW, including all supplies. Total max power, at Ta=25°C, will not exceed 2.5 mW, including all supplies.

4.1.5.1 Conditions for Stop Mode Current and Power Consumption

- ARM core in STOP mode and power gated
- VDDGP, VCC, and VDDA/VDDAL1 voltages at suspend levels
- VDD3P0, VDD2P5, VDD1P8, and VDD1P2 powered off
- USB_VDDA25 and USB_VDDA33 powered off

Table 23. HVIO DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	MIN	TYP	MAX	Units
Pull-up resistor (22 KΩ PU)	Rpu	Vi=OVDD/2	22	29	71	KΩ
Pull-up resistor (47 KΩ PU)	Rpu	Vi=OVDD/2	43	59	148	KΩ
Pull-up resistor (100 KΩ PU)	Rpu	Vi=OVDD/2	46	62	156	KΩ
Pull-down resistor (100 KΩ PD)	Rpd	Vi=OVDD/2	53	77	256	KΩ
Input current (no pull-up/down)	IIN	VI = 0 VI=OVDD	—	2.8	470 50	nA
Input current (22 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	153 0.05	μA
Input current (47 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	77 0.05	μA
Input current (100 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	73 0.05	μA
Input current (100 KΩ PD)	IIN	VI = 0 VI=OVDD	—	—	0.47 63	μA
High-level output current, high voltage mode	Ioh_hv	Vol=0.8*OVDD Low Drive Medium Drive High Drive	 -5.1 -10.2 -15.3	—	—	 mA
External pull-up / pull-down resistor required to overdrive internal keeper	Rext	—	—	—	2.5	KΩ

[1] To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s. VIL and VIH do not apply when hysteresis is enabled.

[2] Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.4 Output Buffer Impedance Characteristics

This section defines the I/O impedance parameters of the i.MX50 processor.

4.5 I/O AC Parameters

The load circuit and output transition time waveforms are shown in Figure 4 and Figure 5. The AC electrical characteristics for slow and fast I/O are presented in the Table 27 and Table 28, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bit in the IOMUX control registers.

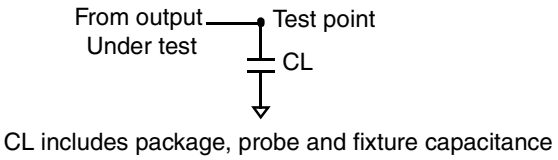

Figure 4. Load Circuit for Output

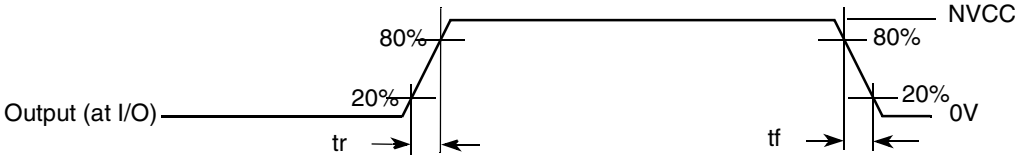

Figure 5. Output Transition Time Waveform

4.5.1 GPIO I/O Slow AC Parameters

Table 27 shows the AC parameters for GPIO slow I/O.

Table 27. GPIO I/O Slow AC Parameters

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF			1.91/1.52 3.07/2.65	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF			2.22/1.81 3.81/3.42	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF			2.88/2.42 5.43/5.02	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF			4.94/4.50 10.55/9.70	ns
Output Pad Slew Rate (Max Drive)[1]	tps	15 pF 35 pF	0.5/0.65 0.32/0.37			V/ns
Output Pad Slew Rate (High Drive)	tps	15 pF 35 pF	0.43/0.54 0.26/0.41			V/ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0.34/0.41 0.18/0.2			V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0.20/0.22 0.09/0.1			V/ns
Output Pad di/dt (Max Drive)	tdit				30	mA/ns

4.5.4 LVIO I/O Fast AC Parameters

Table 30 shows the AC parameters for LVIO fast I/O.

Table 30. LVIO I/O Fast AC Parameters

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF			1.44/1.27 2.78/2.56	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF			1.80/1.61 3.59/3.34	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF			2.55/2.28 5.32/5.01	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF			4.74/4.59 10.59/10.21	ns
Output Pad Slew Rate (Max Drive)[1]	tps	15 pF 35 pF	0.69/0.78 0.36/0.39			V/ns
Output Pad Slew Rate (High Drive)	tps	15 pF 35 pF	0.55/0.61 0.28/0.30			V/ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0.39/0.44 0.19/0.20			V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0.21/0.22 0.09/0.10			V/ns
Output pad di/dt (Max drive)	tdit	—	—	—	70	mA/ns
Output pad di/dt (High drive)	tdit	—	—	—	54	mA/ns
Output pad di/dt (Medium drive)	tdit	—	—	—	35	mA/ns
Output pad di/dt (Low drive)	tdit	—	—	—	18	mA/ns
Input transition times[2]	trm	—	—	—	25	ns

1 tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

2 Hysteresis mode is recommended for inputs with transition time greater than 25 ns.

4.5.5 HVIO I/O Low Voltage (1.8 V) AC Parameters

Table 27 shows the AC parameters for HVIO I/O Low Voltage (1.8 V).

Table 31. HVIO I/O Low Voltage (1.8 V) AC Parameters

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF			1.82/1.97 3.39/3.57	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF			2.48/2.62 4.95/5.14	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF			4.57/4.77 9.60/9.91	ns

Table 40. Asynchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T[2] = GPMI Clock Cycle[3]		Example Timing for GPMI Clock ≈ 100MHz T = 10ns		Unit
			Min.	Max.	Min.	Max.	
NF5	$\overline{WE}$ pulse width	tWP	DS*T		10		ns
NF6	ALE setup time	tALS	(AS+1)*T	—	10	—	ns
NF7	ALE hold time	tALH	(DH+1)*T	—	20	—	ns
NF8	Data setup time	tDS	DS*T	—	10	—	ns
NF9	Data hold time	tDH	DH*T	—	10	—	ns
NF10	Write cycle time	tWC	(DS+DH)*T		20		ns
NF11	$\overline{WE}$ hold time	tWH	DH*T		10		ns
NF12	Ready to $\overline{RE}$ low	tRR	(AS+1)*T	—	10	—	ns
NF13	$\overline{RE}$ pulse width	tRP	DS*T	—	10	—	ns
NF14	READ cycle time	tRC	(DS+DH)*T	—	20	—	ns
NF15	$\overline{RE}$ high hold time	tREH	DH*T		10	—	ns
NF16	Data setup on read	tDSR	N/A		10	—	ns
NF17	Data hold on read	tDHR	N/A		10	—	ns

1 GPMI's Async Mode output timing could be controlled by module's internal register, say HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers' setting. In the above table, we use AS/DS/DH representing these settings each.

2 T represents for the GPMI clock period.

3 AS minimum value could be 0, while DS/DH minimum value is 1.

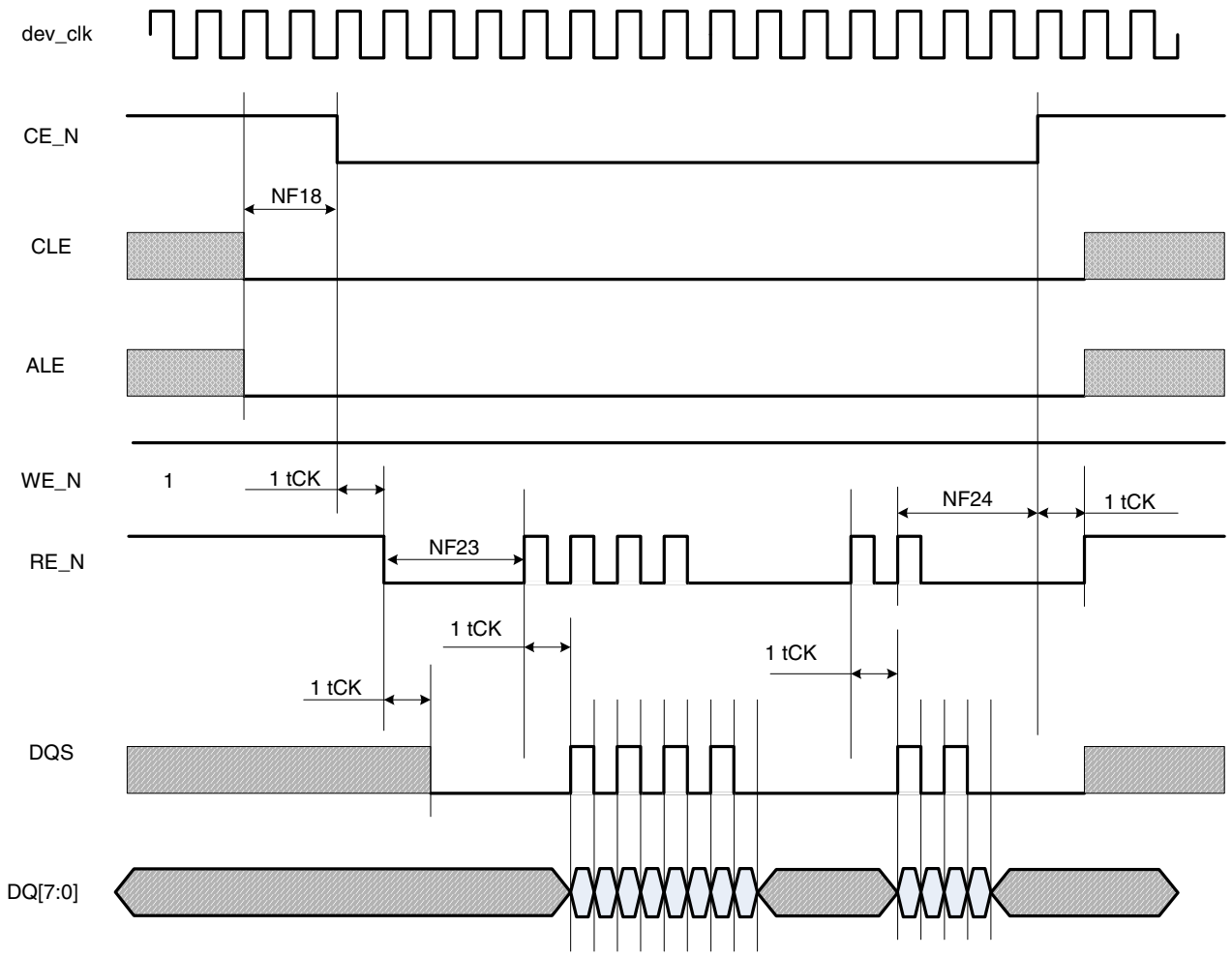

Figure 16. Samsung Toggle Mode Data Read Timing

Table 42. Samsung Toggle Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	CE# access time	t_{CE}	CE_DELAY*t_{CK}	—	ns
NF19	CE# hold time	t_{CH}	0.5 *t_{CK}	—	ns
NF20	Command/address DQ setup time	t_{CAS}	0.5*t_{CK}	—	ns
NF21	Command/address DQ hold time	t_{CAH}	0.5*t_{CK}	—	ns
NF22	clock period	t_{CK}	7.5	—	ns

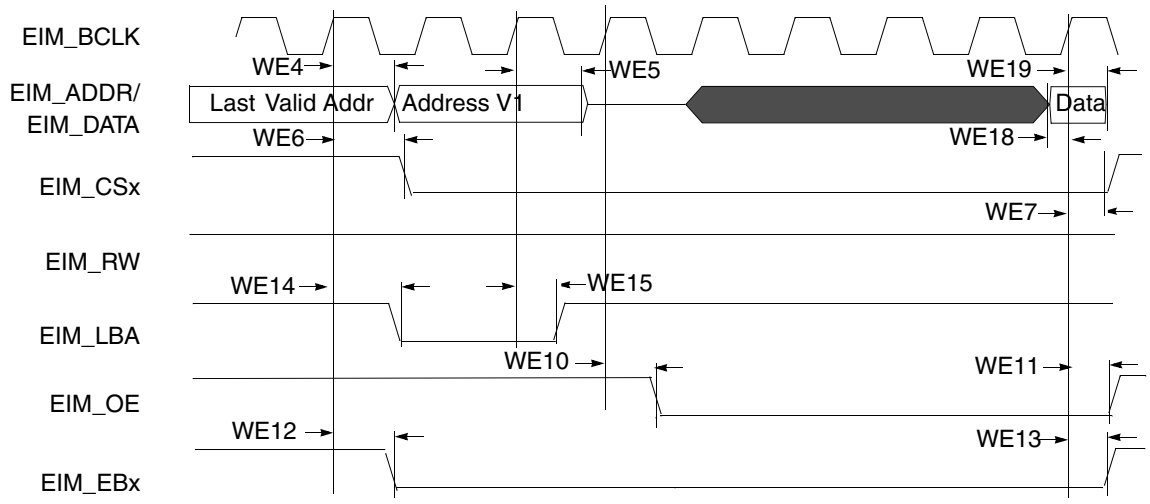

Figure 24. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=2

Figure 25, Figure 26, Figure 27, and Table 44 help to determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

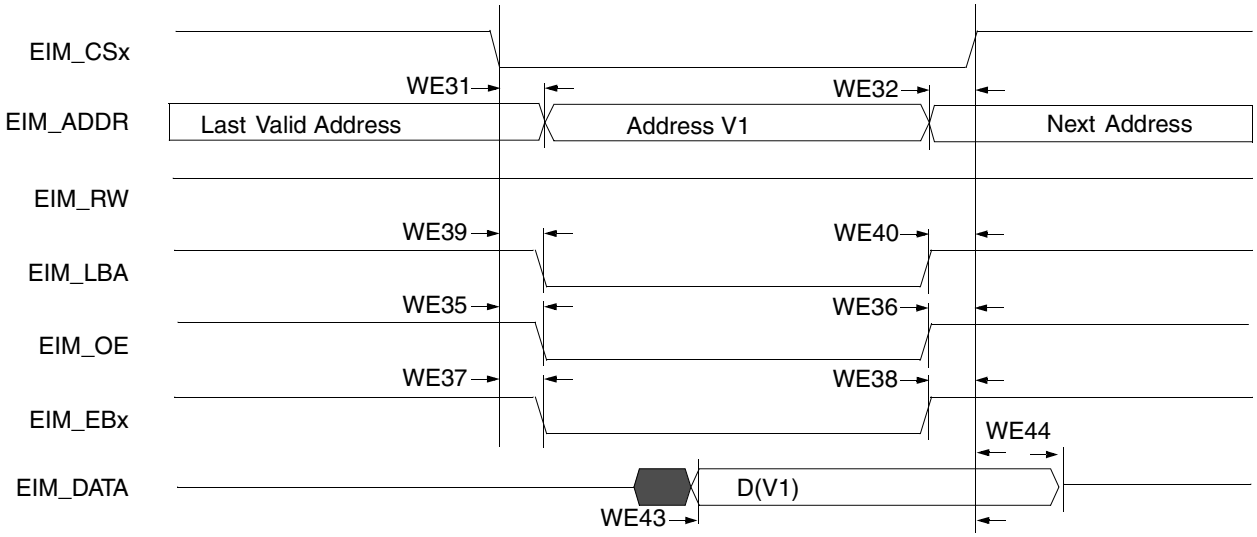

Figure 25. Asynchronous Memory Read Access

4.8.1 DRAM Command & Address Output Timing—DDR2 and LPDDR1

The following diagrams and tables specify the timings related to the address and command pins, which interfaces DDR2 and LPDDR1 memory devices.

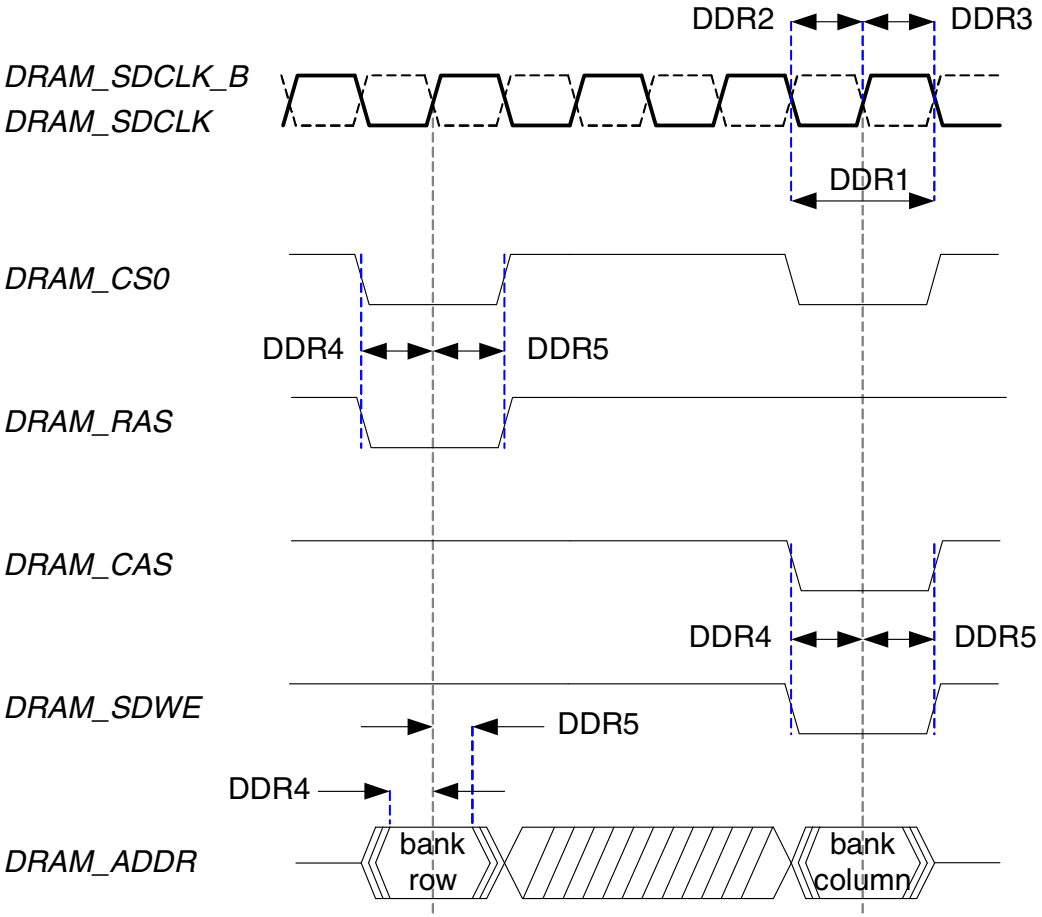

Figure 28. DRAM Command/Address Output Timing—DDR2 and LPDDR1

Table 45. EMI Command/Address AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR1	CK cycle time	tCK	3.75	—	ns
DDR2	CK high level width	tCH	0.48 tCK	0.52 tCK	ns
DDR3	CK low level width	tCL	0.48 tCK	0.52 tCK	ns
DDR4	Address and control output setup time	tIS	0.5 tCK - 0.3	—	ns
DDR5	Address and control output hold time	tIH	0.5 tCK - 0.3	—	ns

Table 60. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min	Typ	Max	Unit
OW1	Reset Time Low	t_{RSTL}	480	511	—[1]	µs
OW2	Presence Detect High	t_{PDH}	15	—	60	µs
OW3	Presence Detect Low	t_{PDL}	60	—	240	µs
OW4	Reset Time High (includes recovery time)	t_{RSTH}	480	512	—	µs

[1] In order not to mask signaling by other devices on the 1-Wire bus, $t_{RSTL} + t_R$ should always be less than 960 µs.

Figure 43 depicts Write 0 Sequence timing, and Table 61 lists the timing parameters.

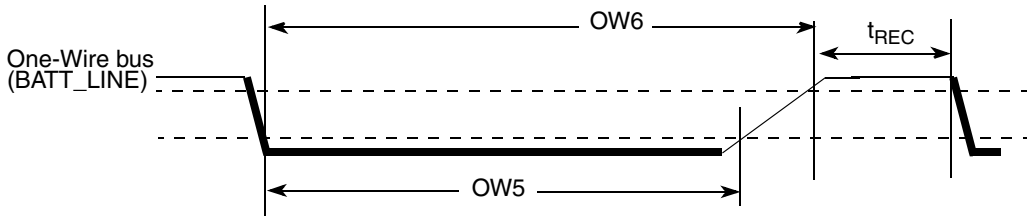

Figure 43. Write 0 Sequence Timing Diagram

Table 61. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Unit
OW5	Write 0 Low Time	t_{LOW0}	60	100	120	µs
OW6	Transmission Time Slot	t_{SLOT}	OW5	117	120	µs
—	Recovery time	t_{REC}	1	—	—	µs

Figure 44 depicts Write 1 Sequence timing, Figure 45 depicts the Read Sequence timing, and Table 62 lists the timing parameters.

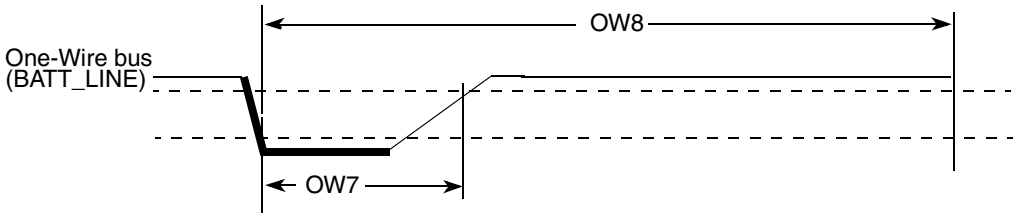

Figure 44. Write 1 Sequence Timing Diagram

4.9.10.3.1 UART IrDA Mode Transmitter

Figure 57 depicts the UART IrDA mode transmit timing with 8 data bit/1 stop bit format. Table 73 lists the transmit timing characteristics.

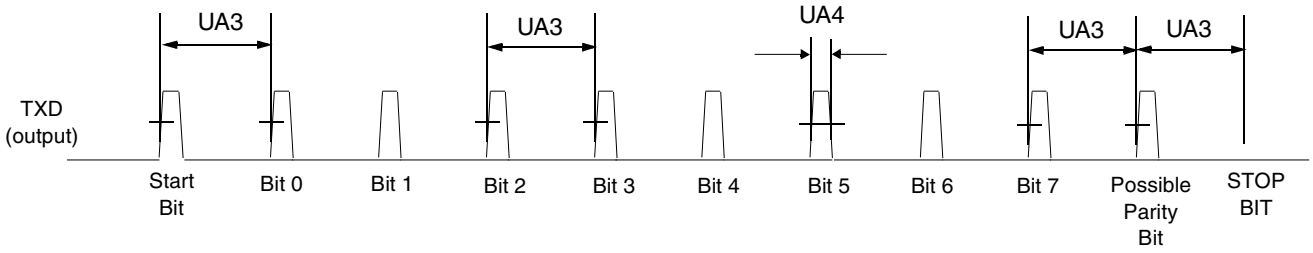

Figure 57. UART IrDA Mode Transmit Timing Diagram

Table 73. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16)*(1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16)*(1/F_{baud\_rate}) + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.9.10.3.2 UART IrDA Mode Receiver

Figure 58 depicts the UART IrDA mode receive timing with 8 data bit/1 stop bit format. Table 74 lists the receive timing characteristics.

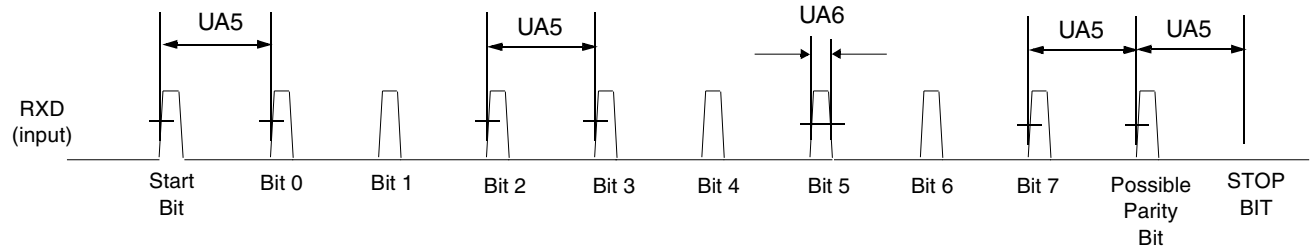

Figure 58. UART IrDA Mode Receive Timing Diagram

Table 74. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$ [2] – $1/(16*F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16*F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16)*(1/F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16*F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16*F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

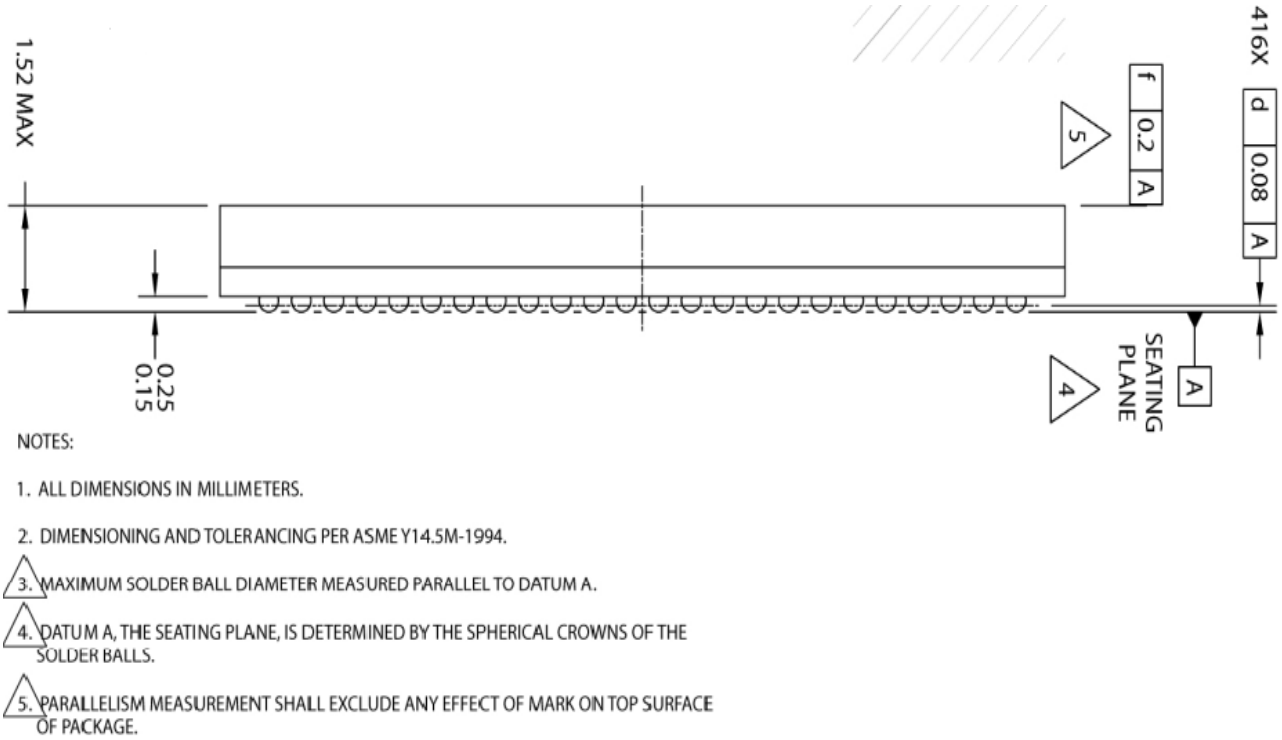

Figure 61. 416 MAPBGA 13x13 mm Package Side View

The following notes apply to Figure 59, Figure 60, and Figure 61:

- Unless otherwise specified dimensions are in millimeters.
- All dimensions and tolerances conform to ASME Y14.5M-1994.
- Parallelism measurement shall exclude any effect of mark on top surface of package.

Table 79. 416 MAPBGA 13x13 mm, 0.5 mm Pitch Ball Map (continued)

AA	Y	W	V	U	T	R
NVCC_SRTC	CKIL	PMIC_ON_REQ	SD2_D2	SD2_CLK	SD2_D0	SD1_CMD
NGND_SRTC	ECKIL	PMIC_STBY_REQ	SD2_D3	SD2_D5	SD2_D1	SD1_D0
NC	NC	NC	NC	NC	NC	NC
JTAG_TDI	JTAG_TMS	JTAG_TCK	SD2_D4	SD2_D6	SD2_CD	SD1_D2
JTAG_TRSTB	VDD_DCDCO	GND_DCDC	SD2_CMD	SD2_D7	SD2_WP	SD1_D3
CKIH	VDD_DCDCI	NC	NC	NC	NC	NC
GND_KEL	USB_OTG_GPANAIO	NC	JTAG_MOD	JTAG_TDO	NVCC_SD1	NVCC_SPI
USB_OTG_RREFEXT	USB_OTG_ID	NC	NVCC_RESET	NVCC_SD2	NVCC_UART	NVCC_SSI
VSS	USB_OTG_VBUS	NC	NVCC_NANDF	NVCC_JTAG	NC	NC
USB_H1_RREFEXT	USB_H1_VBUS	NC	NVCC_NANDF	NVCC_EPDC	NC	NVCC_EPDC
VSS	USB_H1_GPANAIO	NC	CHGR_DET_B	NVCC_LCD	NC	VSS
DISP_D0	DISP_D1	NC	DISP_D11	VSS	NC	VSS
DISP_D2	DISP_D3	NC	DISP_D12	VSS	NC	VSS
DISP_D4	DISP_D5	NC	DISP_D13	VSS	NC	VSS
DISP_D6	DISP_D7	NC	DISP_D14	VSS	NC	VDDAL1
DISP_D8	DISP_D9	NC	DISP_D15	VSS	NC	NC
SD3_D3	DISP_D10	NC	VSS	VSS	VSS	VDDA
SD3_D4	SD3_D5	NC	VSS	VSS	VSS	DRAM_SDODT1
SD3_D6	SD3_D7	NC	NC	NC	NC	NC
DRAM_A4	DRAM_A2	DRAM_A0	VSS	DRAM_SDCKE	DRAM_SDCLK_1	DRAM_SDCLK_1_B
NVCC_EMI_DRAM	DRAM_A3	DRAM_A1	VSS	DRAM_CS1	DRAM_CS0	NVCC_EMI_DRAM
NC	NC	NC	NC	NC	NC	NC
NVCC_EMI_DRAM	DRAM_D1	DRAM_D2	VSS	DRAM_D5	DRAM_D6	NVCC_EMI_DRAM
NVCC_EMI_DRAM	DRAM_D0	DRAM_D3	DRAM_D4	DRAM_D7	DRAM_DQM0	NVCC_EMI_DRAM
AA	Y	W	V	U	T	R

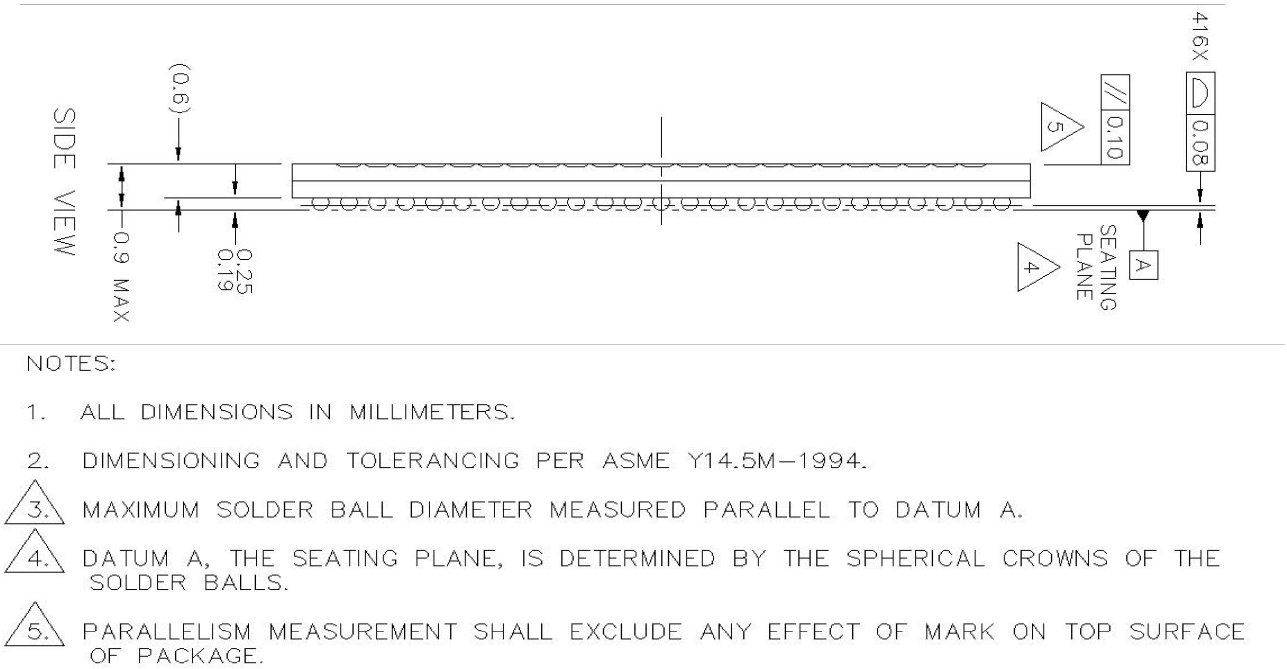

Figure 63. 416 PoPBGA 13 x 13 Package Side View

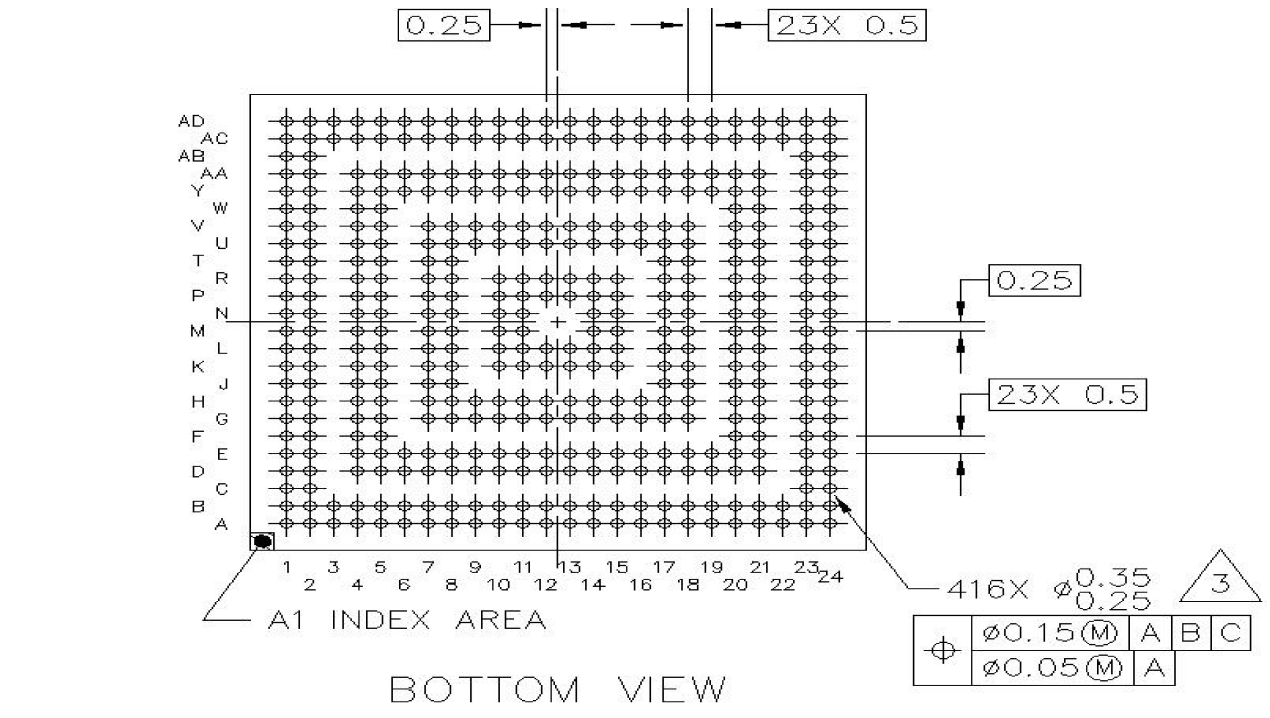

Figure 64. 416 PoPBGA 13 x 13 mm Package Bottom View

The following notes apply to Figure , Figure 63, and Figure 64:

- Unless otherwise specified dimensions are in millimeters.

Table 83. 400 MAPBGA 17 x 17 mm Ball Map (continued)

T	R	P	N	M	L	K
SD2_CD	SD1_CLK	SD1_D1	ECSPI2_MOSI	CSPI_SCLK	UART2_TXD	UART1_RXD
SD2_WP	SD1_D0	SD1_D3	ECSPI1_SCLK	ECSPI2_SS0	UART2_RXD	UART1_RTS
SD2_CLK	SD2_D0	SD1_D2	ECSPI1_SS0	ECSPI1_MISO	CSPI_MOSI	UART3_RXD
SD2_D3	SD2_D6	SD1_CMD	ECSPI2_SCLK	ECSPI1_MOSI	ECSPI2_MISO	CSPI_MISO
VSS	NVCC_SRTC	NVCC_SD2	NVCC_SD1	NVCC_SPI	NVCC_UART	NVCC_SSI
VDD_DCDCO	GND_DCDC	NVCC_RESET	VSS	VSS	VDDGP	VDDGP
GND_KEL	VDD_DCDCI	VSS	VSS	VSS	VSS	VDDGP
JTAG_MOD	JTAG_TCK	VSS	VSS	VSS	VSS	VSS
JTAG_TDO	JTAG_TMS	NVCC_JTAG	VSS	VSS	VSS	VDDA
CHGR_DET_B	VSS	NVCC_LCD	VSS	VCC	VCC	VCC
DISP_D1	VSS	NVCC_NANDF	VSS	VCC	VCC	VCC
DISP_CS	VSS	NVCC_NANDF	VSS	VSS	VCC	VCC
DISP_D13	VSS	VSS	VSS	VSS	VSS	VSS
DISP_RESET	VSS	VSS	NVCC_EMI_DRAM	VSS	VSS	NVCC_EMI_DRAM
SD3_D7	VSS	NVCC_EMI_DRAM	NVCC_EMI_DRAM	VSS	NVCC_EMI_DRAM	NVCC_EMI_DRAM
SD3_D2	NVCC_EMI_DRAM	NVCC_EMI_DRAM	NVCC_EMI_DRAM	NVCC_EMI_DRAM	NVCC_EMI_DRAM	NVCC_EMI_DRAM
DRAM_A0	DRAM_A4	DRAM_CS0	DRAM_DQM0	DRAM_SDQS0	VDDO25	VREF
DRAM_A1	DRAM_SDCKE	DRAM_CS1	DRAM_D5	DRAM_SDQS0_B	DRAM_SDWE	DRAM_SDODT0
DRAM_SDQS2	DRAM_D1	DRAM_D3	DRAM_D7	DRAM_SDBA2	DRAM_A6	DRAM_A5
DRAM_SDQS2_B	DRAM_D0	DRAM_D2	DRAM_D4	DRAM_D6	DRAM_A8	DRAM_A7

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
JTAG_TDI	AA4	AA4	U8	NVCC_JTAG	GPIO	ALT0	IN	47K PU
JTAG_TDO	U7	V4	T9	NVCC_JTAG	GPIO	ALT0	OUT-LO	Keeper
JTAG_TMS	Y4	Y4	R9	NVCC_JTAG	GPIO	ALT0	IN	47K PU
JTAG_TRSTB	AA5	AA5	U7	NVCC_JTAG	GPIO	ALT0	IN	47K PU
KEY_COL0	B1	A9	B1	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_COL1	B2	A10	B2	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_COL2	C1	B9	C1	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_COL3	C2	B10	C2	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW0	D1	A8	D1	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW1	D2	B8	D2	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW2	D4	D7	C3	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW3	E4	A7	D3	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
OWIRE	G7	D12	E5	NVCC_MISC	HVIO	ALT1	IN	Keeper
PMIC_ON_REQ	W1	W1	Y3	NVCC_SRTC	GPIO	ALT0	OUT-LO	—
PMIC_STBY_REQ	W2	W2	Y2	NVCC_SRTC	GPIO	ALT0	OUT-LO	—
POR_B	AD2	AD2	Y5	NVCC_RESET	LVIO	ALT0	IN	100K PU
PWM1	F5	D11	E4	NVCC_MISC	HVIO	ALT1	IN	Keeper
PWM2	F4	D10	E3	NVCC_MISC	HVIO	ALT1	IN	Keeper
RESET_IN_B	AC1	AC1	W3	NVCC_RESET	LVIO	ALT0	IN	100K PU
SD1_CLK	P1	M1	R1	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_CMD	R1	N1	P4	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D0	R2	P2	R2	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D1	P2	N2	P1	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D2	R4	M2	P3	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D3	R5	R4	P2	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD2_CD	T4	J4	T1	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_CLK	U1	E1	T3	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_CMD	V5	G1	V1	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D0	T1	D1	R3	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D1	T2	D2	U1	NVCC_SD2	HVIO	ALT1	IN	Keeper

Table 86. i.MX50 Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 1	10/2011	• Table 5, "Special Signal Considerations," on page 17 changed CHRG_DET_B to CHGR_DET_B. • Table 5, "Special Signal Considerations," on page 17 in the CHGR_DET_B signal remarks, added “The maximum current leakage at this pin is 8.5 μA.” • Table 5, "Special Signal Considerations," on page 17 in the JTAG_MOD remarks, changed “pull-down” to “pull-up, by default” and added “If JTAG port is not needed, the internal pull-up can be disabled in order to reduce supply current to the pin.” • Table 14, "Maximum Supply Current Consumption—ARM CLK = 800 MHz," on page 27 in the 11th row under the Supply column, changed VDDO2P5 to VDDO25. • Table 78, "VBUS Comparators Thresholds," on page 101 changed CHRG_DET_B to CHGR_DET_B. • Table 5, "Special Signal Considerations," on page 17 for 416 MAPBGA, DRAM_SDCLK_0 pin number was changed to N24 and DRAM_SDCLK_0_B pin number was changed to M24. • Table 5, "Special Signal Considerations," on page 17 for 416 MAPBGA, DRAM_SDCLK_1 pin number was changed to T20 and DRAM_SDCLK_1_B pin number was changed to R20. • Table 5, "Special Signal Considerations," on page 17 for 416 MAPBGA, DRAM_SDQS0 pin number was changed to P23 and DRAM_SDQS0_B pin number was changed to P24. • Table 5, "Special Signal Considerations," on page 17 changed pad type of pin DRAM_CALIBRATION to DRAMCALIB. • Table 5, "Special Signal Considerations," on page 17 changed pad type of pins DRAM_SDCLK_0, DRAM_SDCLK_0_B, DRAM_SDCLK_1, DRAM_SDCLK_1_B, DRAM_SDQS0, DRAM_SDQS0_B, DRAM_SDQS1, DRAM_SDQS1_B, DRAM_SDQS2, DRAM_SDQS2_B, DRAM_SDQS3, and DRAM_SDQS3_B to DRAMCLK.
Rev. 0	07/2011	Initial release.