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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	EPDC, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Boot Security, Cryptography, Secure JTAG
Package / Case	416-LFBGA
Supplier Device Package	416-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx508cvk8br2

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by using the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1.3 Operating Ranges

Table 11 provides the operating ranges of the i.MX50 processor.

Table 11. i.MX50 Operating Ranges

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
VDDGP	ARM core supply voltage f_{ARM} = 1 GHz	1.20	1.275	1.35	V
	ARM core supply voltage 400 < f_{ARM} ≤ 800 MHz	0.95	1.05	1.15	V
	ARM core supply voltage 167 < f_{ARM} ≤ 400 MHz	0.85	0.95	1.15	V
	ARM core supply voltage 24 ≤ f_{ARM} ≤ 167 MHz	0.8	0.9	1.15	V
	ARM core supply voltage Stop mode	0.75	0.85	1.15	V
VCC	Peripheral supply voltage Low Performance mode (LPM). The DDR clock rate is 24 MHz.	1[3]	1.05	1.275	V
	Peripheral supply voltage Reduced Performance mode (RPM). The DDR clock rate is 133 MHz.	1[3]	1.05	1.275	V
	Peripheral supply voltage High Performance mode (HPM). The clock frequencies are derived from AHB bus using 133 MHz and AXI bus using 266 MHz (as needed). The DDR clock rate is 266 MHz.	1.175	1.225	1.275	V
	Peripheral supply voltage Stop mode	0.9[3]	0.95	1.275	V
VDDA/VDDAL1	Memory arrays voltage—Run mode 24 ≤ f_{ARM} ≤ 800 MHz	1.15	1.20	1.275	V
	Memory arrays voltage—Run mode f_{ARM} = 1 GHz	1.25	1.30	1.35	V
	Memory arrays voltage—Stop mode	0.9	0.95	1.275	V
VDD3P0	Bandgap and 480 MHz PLL supply	2.7	3.0	3.3	V
VDD2P5	Efuse, 24 MHz oscillator, 32 kHz oscillator mux supply	2.375	2.5	2.625	V
VDD1P2	PLL digital supplies	1.15	1.2	1.32	V
VDD1P8	PLL analog supplies	1.75	1.8	1.95	V

Table 22. LVIO DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	MIN	Typ	MAX	Units
Input current (100 KΩ PD)	IIN	VI = 0 VI=OVDD	—	—	0.25 36	µA
External pull-up / pull-down resistor required to overdrive internal keeper	Rext	—	—	—	47	KΩ

1 To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s. VIL and VIH do not apply when hysteresis is enabled.

2 Hysteresis of 350 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.3.6 High Voltage I/O (HVIO) DC Parameters

Table 23 shows the HVIO DC electrical operating conditions. The parameters are guaranteed per the operating ranges in Table 11, unless otherwise noted.

Table 23. HVIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	MIN	TYP	MAX	Units
High-level output voltage	Voh	Ioh=-1mA Ioh=spec'ed Drive	OVDD-0.15 0.8*OVDD	—	—	V
Low-level output voltage	Vol	Iol=1mA Iol=specified Drive	—	—	0.15 0.2*OVDD	V
High-level output current, low voltage mode	Ioh_lv	Voh=0.8*OVDD Low Drive Medium Drive High Drive	 -2.2 -4.4 -6.6	—	—	 mA
High-level output current, high voltage mode	Ioh_hv	Vol=0.8*OVDD Low Drive Medium Drive High Drive	 -5.1 -10.2 -15.3	—	—	 mA
Low-level output current, low voltage mode	Iol_lv	Voh=0.2*OVDD Low Drive Medium Drive High Drive	 2.2 4.4 6.6	—	—	 mA
Low-level output current, high voltage mode	Iol_hv	Voh=0.2*OVDD Low Drive Medium Drive High Drive	5.1 10.2 15.3	—	—	 mA
High-Level DC input voltage[1]	VIH	—	0.7*OVDD	—	OVDD	V
Low-Level DC input voltage	VIL	—	0V	—	0.3*OVDD	V
Input Hysteresis	VHYS	OVDD=1.875 OVDD=3.0	0.25	0.36 0.80	—	V
Schmitt trigger VT+[2]	VT+	—	0.5*OVDD	—	—	V
Schmitt trigger VT-	VT-	—	—	—	0.5*OVDD	V

Table 23. HVIO DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	MIN	TYP	MAX	Units
Pull-up resistor (22 KΩ PU)	Rpu	Vi=OVDD/2	22	29	71	KΩ
Pull-up resistor (47 KΩ PU)	Rpu	Vi=OVDD/2	43	59	148	KΩ
Pull-up resistor (100 KΩ PU)	Rpu	Vi=OVDD/2	46	62	156	KΩ
Pull-down resistor (100 KΩ PD)	Rpd	Vi=OVDD/2	53	77	256	KΩ
Input current (no pull-up/down)	IIN	VI = 0 VI=OVDD	—	2.8	470 50	nA
Input current (22 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	153 0.05	μA
Input current (47 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	77 0.05	μA
Input current (100 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	73 0.05	μA
Input current (100 KΩ PD)	IIN	VI = 0 VI=OVDD	—	—	0.47 63	μA
High-level output current, high voltage mode	Ioh_hv	Vol=0.8*OVDD Low Drive Medium Drive High Drive	 -5.1 -10.2 -15.3	—	—	 mA
External pull-up / pull-down resistor required to overdrive internal keeper	Rext	—	—	—	2.5	KΩ

[1] To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s. VIL and VIH do not apply when hysteresis is enabled.

[2] Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.4 Output Buffer Impedance Characteristics

This section defines the I/O impedance parameters of the i.MX50 processor.

Table 37. WDOG_RST_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC5	Duration of WDOG_RST_B Assertion	1	—	T_{CKIL}

NOTE

CKIL is approximately 32 kHz. T_{CKIL} is one period or approximately 30 µs.

4.6.3 Clock Amplifier Parameters (CKIH)

The input to clock amplifier (CAMP) is internally ac-coupled allowing direct interface to a square wave or sinusoidal frequency source. No external series capacitors are required.

Table 38 shows the electrical parameters of CAMP.

Table 38. CAMP Electrical Parameters (CKIH)

Parameter	Min	Typ	Max	Unit
Input frequency	8.0	—	40.0	MHz
VIL (for square wave input)	0	—	0.3	V
VIH (for square wave input)	(VCC[1] – 0.25)	—	3	V
Sinusoidal input amplitude	0.4 [2]	—	VDD	Vp-p
Output duty cycle	45	50	55	%

1 VCC is the supply voltage of CAMP.

2 This value of the sinusoidal input is determined during characterization.

4.6.4 DPLL Electrical Parameters

Table 39 shows the electrical parameters of digital phase-locked loop (DPLL).

Table 39. DPLL Electrical Parameters

Parameter	Test Conditions/Remarks	Min	Typ	Max	Unit
Reference clock frequency range[1]	—	10	—	100	MHz
Reference clock frequency range after pre-divider	—	10	—	40	MHz
Output clock frequency range (dpdck_2)	—	300	—	1025	MHz
Pre-division factor[2]	—	1	—	16	—
Multiplication factor integer part	—	5	—	15	—
Multiplication factor numerator[3]	Should be less than denominator	–67108862	—	67108862	—
Multiplication factor denominator[2]	—	1	—	67108863	—
Output duty cycle	—	48.5	50	51.5	%

operations under Asynchronous mode. Table 40 describes the timing parameters (NF1–NF17) that are shown in the figures.

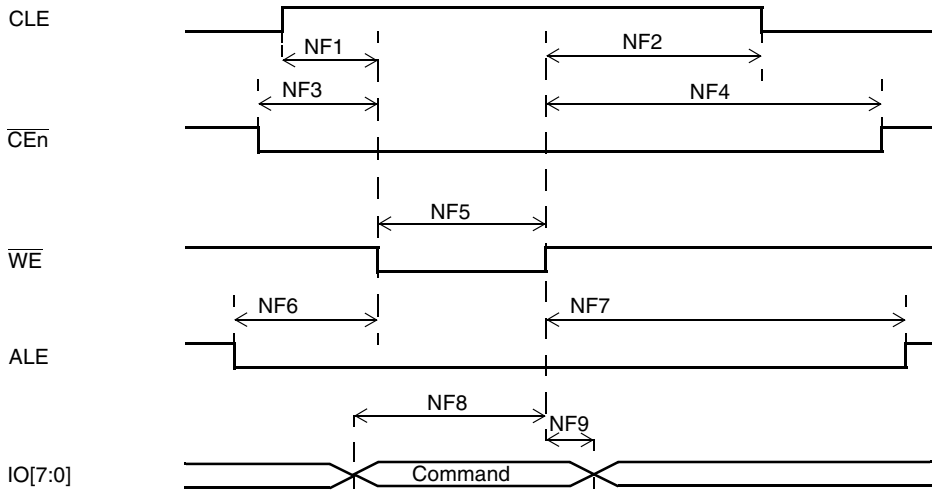

Figure 8. Command Latch Cycle Timing Diagram

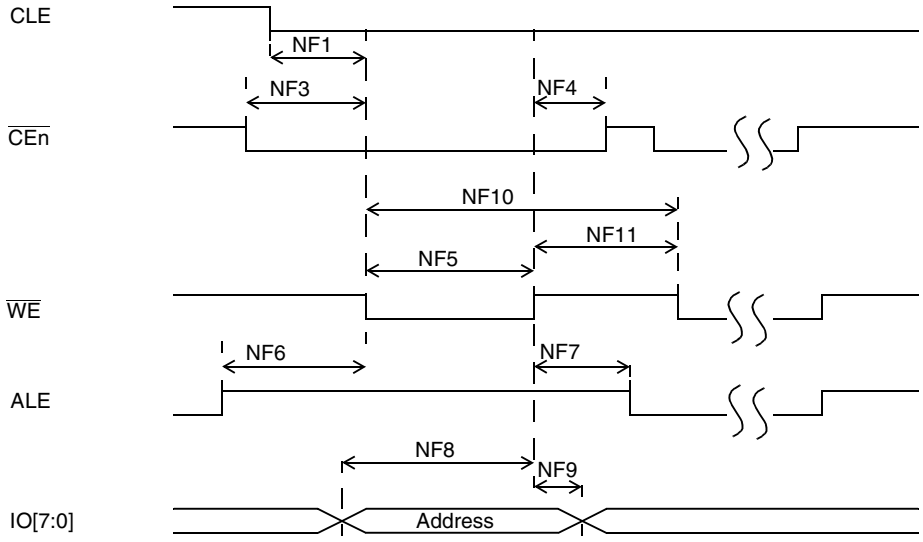

Figure 9. Address Latch Cycle Timing Diagram

4.6.5.2 Source Synchronous Mode AC Timing (ONFI 2.x Compatible)

The following diagrams show the write and read timing of Source Synchronous Mode.

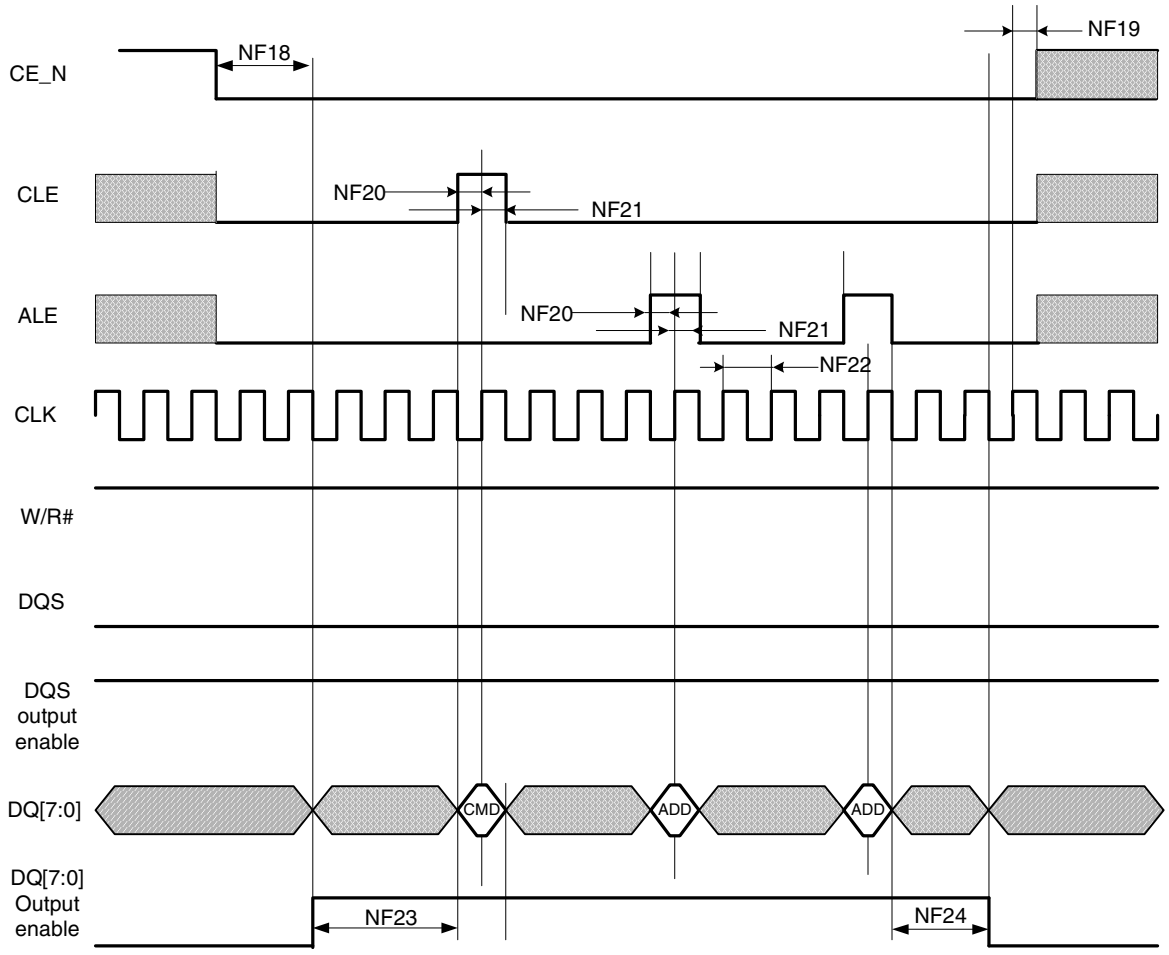

Figure 12. Source Synchronous Mode Command and Address Timing Diagram

Table 48. DDR2 Input AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR21	DQS to DQ input skew	tDQSQ	—	0.65	ns
DDR22	DQS to DQ input hold time	tQH	0.45 tCK -0.85	—	ns

NOTE

The timing parameter DDR20(tDQSCK) is not strictly required by this DRAM MC design.

4.9 External Peripheral Interfaces

The following sections provide information on external peripheral interfaces.

4.9.1 AUDMUX Timing Parameters

The AUDMUX provides programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is hence governed by the SSI module.

4.9.2 CSPI and eCSPI Timing Parameters

This section describes the timing parameters of the CSPI and eCSPI modules. The CSPI and eCSPI have separate timing parameters for master and slave modes. The nomenclature used with the CSPI/eCSPI modules and the respective routing of these signals is shown in Table 49.

Table 49. CSPI Nomenclature and Routing

Module	I/O Access
eCSPI1	GPIO, KPP, DISP0_DAT, CSI0_DAT, and EIM_D through IOMUX
eCSPI2	DISP0_DAT, CSI0_DAT, and EIM through IOMUX
CSPI	DISP0_DAT, EIM_A/D, SD1, and SD2 through IOMUX

Table 59. I²C Module Timing Parameters (continued)

ID	Parameter	Standard Mode Supply Voltage = 1.65 V–1.95 V, 2.7 V–3.3 V		Fast Mode Supply Voltage = 2.7 V–3.3 V		Unit
		Min	Max	Min	Max	
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal.

3 A Fast-mode I²C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2CLK line is released.

4 C_b = total capacitance of one bus line in pF.

4.9.6 One-Wire (OWIRE) Timing Parameters

Figure 42 depicts the RPP timing, and Table 60 lists the RPP timing parameters.

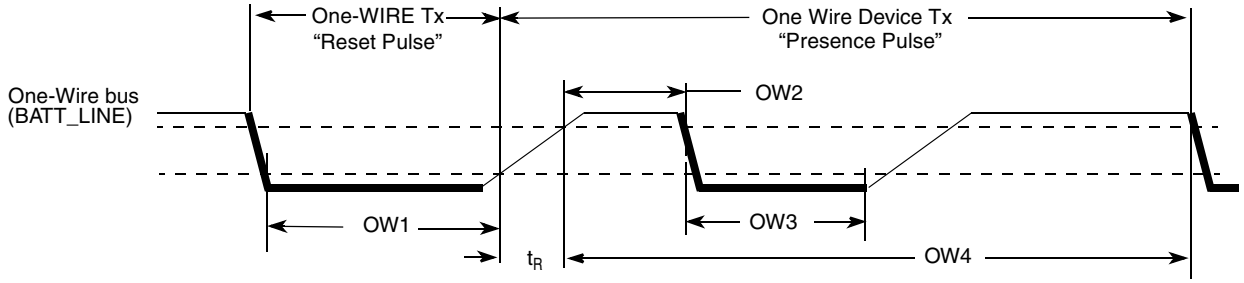

Figure 42. Reset and Presence Pulses (RPP) Timing Diagram

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in both the tables and figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- Tx and Rx refer to the transmit and receive sections of the SSI.
- The terms WL and BL refer to word length (WL) and bit length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.9.10 UART I/O Configuration and Timing Parameters

The following sections describe the UART I/O configuration and timing parameters.

4.9.10.1 UART RS-232 I/O Configuration in Different Modes

Table 70 shows the UART I/O configuration based on which mode is enabled.

Table 70. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
RTS	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
CTS	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
TXD_MUX	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
RXD_MUX	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.9.10.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

Table 79. 416 MAPBGA 13x13 mm, 0.5 mm Pitch Ball Map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
AB	BOOT_MODE0	BOOT_MODE1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	DRAM_SDQS2	DRAM_SDQS2_B	AB
AC	RESET_IN_B	TEST_MODE	GND3P0	GND2P5	EXTAL	GND1P2	GND1P8	USB_OTG_DN	USB_OTG_VDDA25_1	USB_H1_DN	USB_H1_VDDA33	DISP_BUSY	DISP_RS	DISP_RESET	SD3_D0	SD3_D1	SD3_D2	VSS	DRAM_D16	DRAM_D18	NVCC_EMI_DRAM	DRAM_D20	DRAM_D22	DRAM_DQM2	AC
AD	VSS	POR_B	VDD3P0	VDD2P5	XTAL	VDD1P2	VDD1P8	USB_OTG_DP	USB_H1_VDDA25_1	USB_H1_DP	USB_OTG_VDDA33	DISP_WR	DISP_RD	DISP_CS	SD3_WP	SD3_CLK	SD3_CMD	VSS	DRAM_D17	DRAM_D19	NVCC_EMI_DRAM	DRAM_D21	DRAM_D23	VSS	AD

5.1.3 416 MAPBGA 13 x 13 Power Rails

Table 80. 416 MAPBGA 13x13 Ground, Power, Sense, and Reference Contact Signals

Pin Name	Ball Number	Comments
GND_DCDC	W5	—
NVCC_EIM	L7, M7, M8	—
NVCC_EMI_DRAM	A21, AA21, AA23, AA24, AC21, AD21, B21, D21, D23, D24, K21, K23, K24, R21, R23, R24	—
NVCC_EPDC	M10, N10, P10, R10, U10	—
NVCC_JTAG	U9	—
NVCC_KEYPAD	N8	—
NVCC_LCD	U11	—
NVCC_MISC	P8	—
NVCC_NANDF	V9, V10	—
NVCC_RESET	V8	—
NVCC_SD1	T7	—
NVCC_SD2	U8	—
NVCC_SPI	R7	—

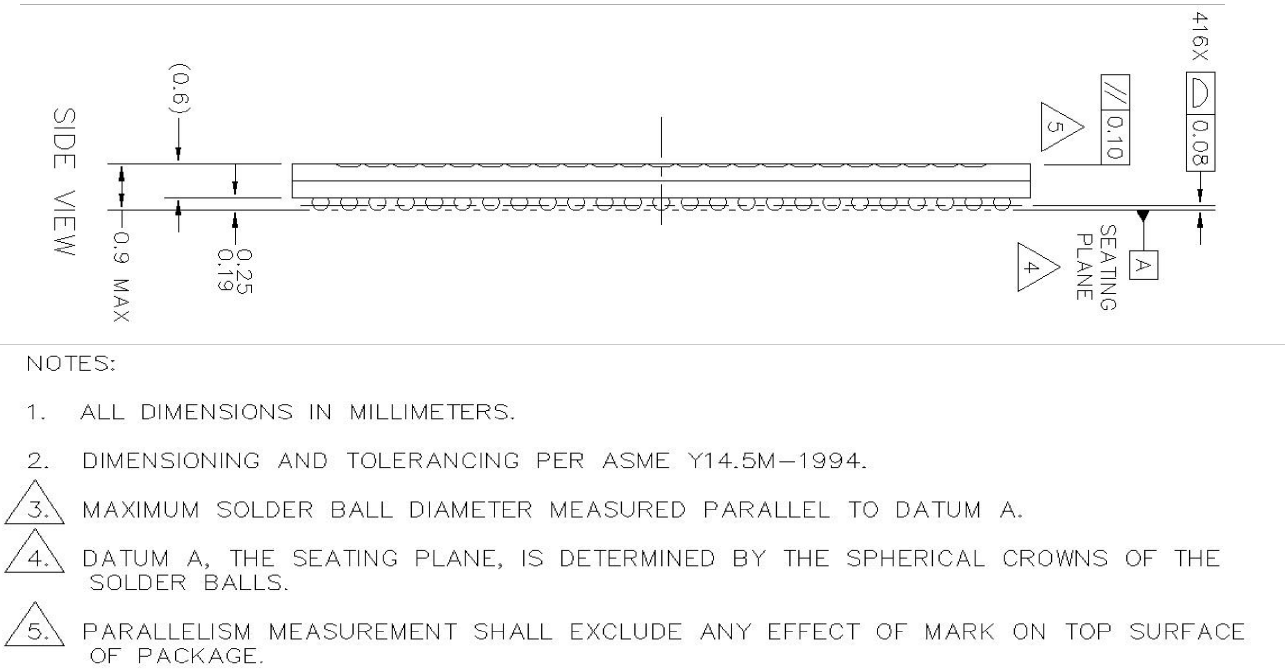

Figure 63. 416 PoPBGA 13 x 13 Package Side View

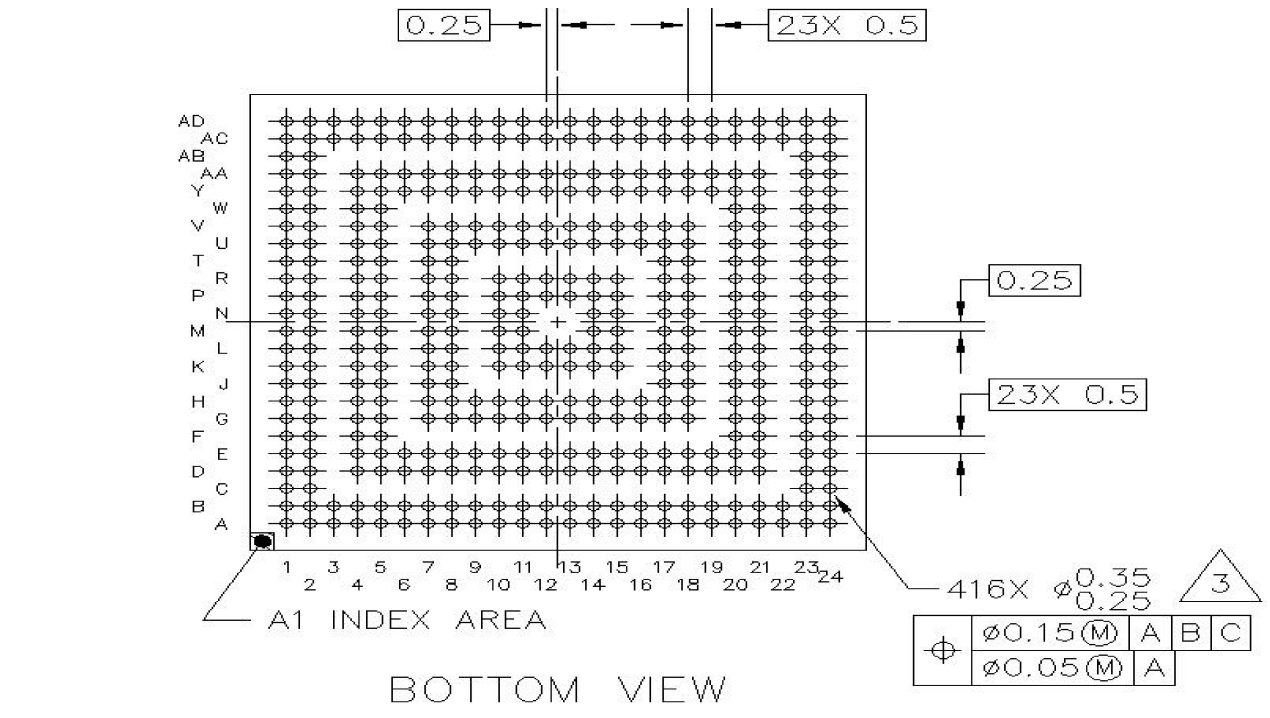

Figure 64. 416 PoPBGA 13 x 13 mm Package Bottom View

The following notes apply to Figure , Figure 63, and Figure 64:

- Unless otherwise specified dimensions are in millimeters.

Table 81. 416 PoPBGA 13 x 13 mm Ball Map (continued)

Y	W	V	U	T	R	P
CKIL	PMIC_ON_REQ	SD3_D0	SD3_D5	SD3_CLK	SD3_D2	SD3_D4
ECKIL	PMIC_STBY_REQ	SD3_D1	SD3_D3	SD3_CMD	SD3_D6	SD1_D0
NC	NC	NC	NC	NC	NC	NC
JTAG_TMS	JTAG_TCK	JTAG_TDO	SD3_D7	SD3_WP	SD1_D3	DRAM_CALIBRATION
VDD_DCDCO	GND_DCDC	JTAG_MOD	DRAM_CS0	DRAM_SDCKE	DRAM_SDCLK_0	DRAM_SDCLK_0_B
VDD_DCDCI	NC	NC	NC	NC	NC	NC
DRAM_A1	NC	DRAM_A0	DRAM_CS1	NVCC_SD1	NVCC_SPI	DRAM_A5
DRAM_A2	NC	NVCC_RESET	NVCC_SD2	NVCC_UART	NVCC_SSI	NVCC_MISC
DRAM_A3	NC	NVCC_NANDF	NVCC_JTAG	NC	NC	NC
DRAM_A4	NC	NVCC_NANDF	NVCC_EPDC	NC	NVCC_EPDC	NVCC_EPDC
DRAM_D17	NC	DRAM_D16	NVCC_LCD	NC	VSS	VSS
DRAM_D19	NC	DRAM_D18	VSS	NC	VSS	VSS
DRAM_D21	NC	DRAM_D20	VSS	NC	VSS	VSS
DRAM_D23	NC	DRAM_D22	VSS	NC	VSS	VSS
DRAM_SDQS2	NC	DRAM_SDQS2_B	VSS	NC	VDDAL1	VDDAL1
DRAM_DQM2	NC	DRAM_D0	VSS	NC	NC	NC
DRAM_D1	NC	DRAM_D2	VSS	VSS	VDDA	VDDA
NVCC_EMI_DRAM	NC	NVCC_EMI_DRAM	DRAM_D5	DRAM_D6	DRAM_D7	DRAM_SDQS0_B
NVCC_EMI_DRAM	NC	NC	NC	NC	NC	NC
NVCC_EMI_DRAM	NVCC_EMI_DRAM	NVCC_EMI_DRAM	DRAM_D3	DRAM_D4	NVCC_EMI_DRAM	NVCC_EMI_DRAM
EPDC_BDR0	EPDC_VCOM1	EPDC_SDOE	EPDC_SDOEZ	EPDC_D9	EPDC_D11	EPDC_D15
NC	NC	NC	NC	NC	NC	NC
EPDC_BDR1	EPDC_D8	EPDC_D10	EPDC_D2	EPDC_D7	EPDC_SDOED	EPDC_GDSP
EPDC_D0	EPDC_D1	EPDC_D3	EPDC_D6	EPDC_D5	EPDC_D4	EPDC_SDCE1

Table 82. 416 PoPBGA 13 x 13 mm Ground, Power, Sense, and Reference Contact Signals (continued)

VDD2P5	AD4	—
VDD3P0	AD3	—
VDDA	P17, R17	—
VDDAL1	P15, R15	—
VDDGP	G10, G8, G9, H10, H7, H8, H9, J7, J8, K10, K7, K8, L10, L7, L8	—
VDDO25	N23	—
VSS	A1, A24, AA11, AA18, AA2, AA9, AC18, AC3, AC4, AC6, AC7, AD1, AD18, AD24, E17, E18, E21, E8, E9, F21, G11, G12, G13, G21, G23, H11, H12, H13, K11, K12, K13, L11, L12, L13, L14, L17, M11, M14, M15, M17, N11, N14, N15, N17, P11, P12, P13, P14, R11, R12, R13, R14, T17, U12, U13, U14, U15, U16, U17	—

5.3 17 x 17 mm, 0.8 mm Pitch, 400 Pin MAPBGA Package Information

This section contains the outline drawing, signal assignment map, ground, power, reference ID (by ball grid location) for the 17 x 17 mm, 0.8 mm pitch, 400 pin MAPBGA package.

5.3.1 400 MAPBGA 17 x 17 mm Package Views

Figure 65 shows the top view of the 17 x 17 mm package, Figure 66 shows the bottom view of the package, and Figure 67 shows the side view of the package.

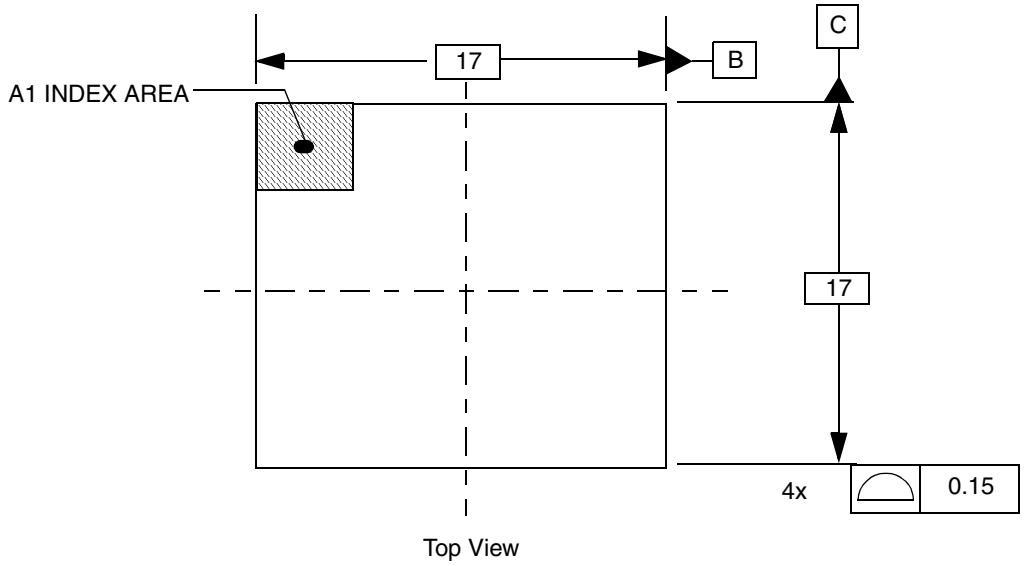

Figure 65. 400 MAPBGA 17x17 mm Package Top view

Table 84. 400 MAPBGA 17x17 Ground, Power, Sense, and Reference Contact Signals (continued)

VDD_DCDCI	R7
VDD_DCDCO	T6
GND_DCDC	R6

5.4 Signal Assignments

Table 85. Alphabetical List of Signal Assignments

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
BOOT_MODE0	AB1	AB1	V3	NVCC_RESET	LVIO	ALT0	IN	100K PU
BOOT_MODE1	AB2	AB2	U3	NVCC_RESET	LVIO	ALT0	IN	100K PU
CHGR_DET_B	V11	AA15	T10	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG25	—	OUT-OD	—
CKIH	AA6	AA6	V4	NVCC_JTAG	ANALOG	—	—	—
CKIL	Y1	Y1	Y4	NVCC_SRTC	ANALOG	—	—	—
CSPI_MISO	M5	H2	K4	NVCC_SPI	HVIO	ALT1	IN	Keeper
CSPI_MOSI	M2	J1	L3	NVCC_SPI	HVIO	ALT1	IN	Keeper
CSPI_SCLK	M1	H1	M1	NVCC_SPI	HVIO	ALT1	IN	Keeper
CSPI_SS0	M4	J2	J4	NVCC_SPI	HVIO	ALT1	IN	Keeper
DISP_BUSY	AC12	AA21	U11	NVCC_LCD	HVIO	ALT1	IN	Keeper
DISP_CS	AD14	AC21	T12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D0	AA12	AC17	V11	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D1	Y12	AC16	T11	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D10	Y17	AD22	Y16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D11	V12	AD19	W14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D12	V13	AC22	V14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D13	V14	AC23	T13	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D14	V15	AB23	U14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D15	V16	AD21	Y15	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D2	AA13	AD15	W12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D3	Y13	AC15	W13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D4	AA14	AC24	Y13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D5	Y14	AB24	U13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
DRAM_D10	G24	G20	E17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D11	H23	H18	D19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D12	F23	G18	D18	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D13	F24	F20	E18	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D14	E24	E20	C18	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D15	E23	E19	C17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D16	AC19	V11	Y19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D17	AD19	Y11	Y18	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D18	AC20	V12	V19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D19	AD20	Y12	W19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D2	W23	V17	P20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D20	AC22	V13	W20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D21	AD22	Y13	W18	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D22	AC23	V14	V20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D23	AD23	Y14	U19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D24	B23	G15	B19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D25	A23	E15	B18	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D26	A22	E14	A16	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D27	B22	G14	B17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D28	B20	E13	A17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D29	A20	E12	A18	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D3	W24	U20	P19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D30	A19	E11	A19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D31	B19	E10	B20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D4	V24	T20	N20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D5	U23	U18	N18	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D6	T23	T18	M20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D7	U24	R18	N19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D8	J23	J18	D17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D9	H24	H20	F18	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
DRAM_DQM0	T24	M18	N17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_DQM1	J24	L18	F17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_DQM2	AC24	Y16	U20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_DQM3	B24	G17	D20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_OPEN	J18	—	H18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_OPENFB	H18	—	H17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_RAS	H21	—	E20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	Keeper
DRAM_SDBA0	K18	—	J20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDBA1	L18	—	H20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDBA2	N18	—	M19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDCKE	U20	T5	R18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDCLK_0	N24	R5	J17	NVCC_EMI_DRAM	DRAMCLK	ALT0	OUT-LO	Keeper
DRAM_SDCLK_0_B	M24	P5	J18	NVCC_EMI_DRAM	DRAMCLK	ALT0	OUT-HI	—
DRAM_SDCLK_1	T20	—	—	NVCC_EMI_DRAM	DRAMCLK	ALT0	OUT-LO	Keeper
DRAM_SDCLK_1_B	R20	—	—	NVCC_EMI_DRAM	DRAMCLK	ALT0	OUT-HI	—
DRAM_SDODT0	G18	—	K18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDODT1	R18	—	—	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDQS0	P23	N18	M17	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS0_B	P24	P18	M18	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS1	L23	J20	G17	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS1_B	L24	K18	G18	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS2	AB23	Y15	T19	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS2_B	AB24	V15	T20	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS3	C23	E16	C19	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS3_B	C24	G16	C20	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDWE	P18	—	L18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	Keeper
ECKIL	Y2	Y2	W4	NVCC_SRTC	ANALOG	—	—	—
ECSPI1_MISO	N7	K4	M3	NVCC_SPI	HVIO	ALT1	IN	Keeper
ECSPI1_MOSI	N2	N4	M4	NVCC_SPI	HVIO	ALT1	IN	Keeper

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
JTAG_TDI	AA4	AA4	U8	NVCC_JTAG	GPIO	ALT0	IN	47K PU
JTAG_TDO	U7	V4	T9	NVCC_JTAG	GPIO	ALT0	OUT-LO	Keeper
JTAG_TMS	Y4	Y4	R9	NVCC_JTAG	GPIO	ALT0	IN	47K PU
JTAG_TRSTB	AA5	AA5	U7	NVCC_JTAG	GPIO	ALT0	IN	47K PU
KEY_COL0	B1	A9	B1	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_COL1	B2	A10	B2	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_COL2	C1	B9	C1	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_COL3	C2	B10	C2	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW0	D1	A8	D1	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW1	D2	B8	D2	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW2	D4	D7	C3	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
KEY_ROW3	E4	A7	D3	NVCC_KEYPAD	HVIO	ALT1	IN	Keeper
OWIRE	G7	D12	E5	NVCC_MISC	HVIO	ALT1	IN	Keeper
PMIC_ON_REQ	W1	W1	Y3	NVCC_SRTC	GPIO	ALT0	OUT-LO	—
PMIC_STBY_REQ	W2	W2	Y2	NVCC_SRTC	GPIO	ALT0	OUT-LO	—
POR_B	AD2	AD2	Y5	NVCC_RESET	LVIO	ALT0	IN	100K PU
PWM1	F5	D11	E4	NVCC_MISC	HVIO	ALT1	IN	Keeper
PWM2	F4	D10	E3	NVCC_MISC	HVIO	ALT1	IN	Keeper
RESET_IN_B	AC1	AC1	W3	NVCC_RESET	LVIO	ALT0	IN	100K PU
SD1_CLK	P1	M1	R1	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_CMD	R1	N1	P4	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D0	R2	P2	R2	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D1	P2	N2	P1	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D2	R4	M2	P3	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD1_D3	R5	R4	P2	NVCC_SD1	HVIO	ALT1	IN	Keeper
SD2_CD	T4	J4	T1	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_CLK	U1	E1	T3	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_CMD	V5	G1	V1	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D0	T1	D1	R3	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D1	T2	D2	U1	NVCC_SD2	HVIO	ALT1	IN	Keeper

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
SD2_D2	V1	F1	W2	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D3	V2	F2	T4	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D4	V4	G2	V2	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D5	U2	E2	U2	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D6	U4	H4	R4	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D7	U5	F4	W1	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_WP	T5	G4	T2	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD3_CLK	AD16	T1	Y14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_CMD	AD17	T2	U16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D0	AC15	V1	Y17	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D1	AC16	V2	V16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D2	AC17	R1	T16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D3	AA17	U2	U15	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D4	AA18	P1	W17	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D5	Y18	U1	U17	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D6	AA19	R2	V17	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D7	Y19	U4	T15	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_WP	AD15	T4	W16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SSI_RXC	J7	AD12	H4	NVCC_SSI	HVIO	ALT1	IN	Keeper
SSI_RXD	J5	AC14	F3	NVCC_SSI	HVIO	ALT1	IN	Keeper
SSI_RXFS	H7	AD13	G5	NVCC_SSI	HVIO	ALT1	IN	Keeper
SSI_TXC	J4	AC13	G3	NVCC_SSI	HVIO	ALT1	IN	Keeper
SSI_TXD	H5	AD14	G4	NVCC_SSI	HVIO	ALT1	IN	Keeper
SSI_TXFS	H4	AC12	H3	NVCC_SSI	HVIO	ALT1	IN	Keeper
TEST_MODE	AC2	AC2	U4	NVCC_RESET	LVIO	ALT0	IN	100K PD
UART1_CTS	H2	B4	J1	NVCC_UART	HVIO	ALT1	IN	Keeper
UART1_RTS	J2	B3	K2	NVCC_UART	HVIO	ALT1	IN	Keeper
UART1_RXD	J1	A2	K1	NVCC_UART	HVIO	ALT1	IN	Keeper
UART1_TXD	H1	A3	H1	NVCC_UART	HVIO	ALT1	IN	Keeper
UART2_CTS	K2	B2		NVCC_UART	HVIO	ALT1	IN	Keeper

6 Revision History

Table 86 provides a revision history for this data sheet.

Table 86. i.MX50 Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 7	10/2013	• Added new part number information for parts with 1 GHz core frequencies: — MCIMX508CVK1B — MCIMX508CVM1B — MCIMX507CVM1B — MCIMX507CVK1B Updated sections: — Section 1, “Introduction” — Table 1, “Ordering Information” — Table 11, “i.MX50 Operating Ranges” — Table 15, “Maximum Supply Current Consumption—ARM CLK = 1 GHz” (added)
Rev. 6	07/2013	• In Table 11, “i.MX50 Operating Ranges,” added VCC Stop mode ranges.
Rev. 5	05/2013	• In Table 11, “i.MX50 Operating Ranges,” changed VCC peripheral supply (LPM) minimum voltage from 0.9 V to 1 V, and changed nominal voltage from 0.95 V to 1.05 V.
Rev. 4	01/2013	• In Table 1, "Ordering Information," on page 7, added new part number information for MCIMX507CVK8B. • In Figure 27, "DTACK Read Access," on page 67, updated timing of EIM_DTACK.
Rev. 3	10/2012	• In Table 11, "i.MX50 Operating Ranges," on page 24: —Changed DDR clock rate for reduced performance mode (RPM) of VCC from 100 MHz to 133 MHz —Changed DDR clock rate for high performance mode (HPM) of VCC from 200 MHz to 266 MHz
Rev. 2	05/2012	• In Table 1, "Ordering Information," on page 7, added the following new part numbers: MCIMX508CZK8B, MCIMX503CVK8B, MCIMX503EVM8B, MCIMX502CVK8B, and MCIMX502EVM8B. • In Table 1, "Ordering Information," on page 7, added a new column, $T_{junction}$. • In Table 3, "Package Feature Comparison," on page 9, added a new row for 416 PoPBGA package. • Updated Figure 1, "i.MX50 System Block Diagram," on page 10 by removing “LDOx3” and “DC-DC 1.2V.” • In Table 5, "Special Signal Considerations," on page 17, updated details for the following signals: DRAM_OPEN/DRAM_OPENFB and DRAM_SDODT0/DRAM_SDODT1 • In Table 5, "Special Signal Considerations," on page 17, added new rows for the following signals: POP_EMMC_RST, POP_LPDDR2_ZQ0/ZQ1, POP_LPDDR2_1.8V, and POP_NAND_VCC. • Added Section 4.1.2.1, “13 x 13 mm MAPBGA Package Thermal Resistance Data.” • Added Section 4.1.2.2, “13 x 13 mm PoPBGA Package Thermal Resistance Data.” • Added Section 4.1.2.3, “17 x 17 mm MAPBGA Package Thermal Resistance Data.” • In Table 11, "i.MX50 Operating Ranges," on page 24, added footnotes for USB_OTG_VDDA25 and USB_OTG_VDDA33. • In Table 78, "VBUS Comparators Thresholds," on page 101, changed VBUS input max current to 350 µA. • Added Section 5.2, “13 x 13 mm, 0.5 mm Pitch, 416 Pin PoPBGA Package Information.” • In Table 85, "Alphabetical List of Signal Assignments," on page 124: —Added a new column “416 PoPBGA Ball Number” —Changed “USB_H1_VDDA” to “USB_H1_VDDA25, USB_H1_VDDA33” —Changed “USB_OTG_VDDA” to “USB_OTG_VDDA25, USB_OTG_VDDA33” • Replace mDDR with LPDDR1 throughout the document.