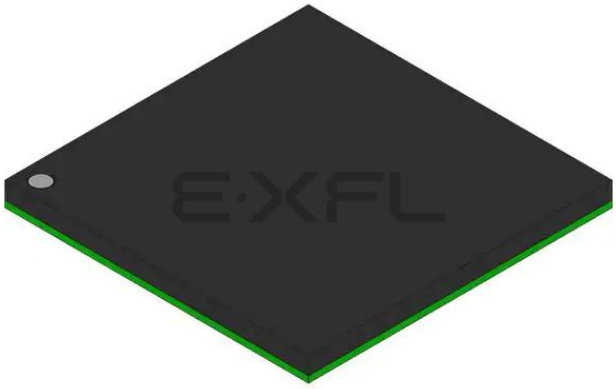

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	EPDC, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Boot Security, Cryptography, Secure JTAG
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx508cvm8b

- NEON coprocessor (SIMD Media Processing Architecture) and Vector Floating Point (VFP-Lite) coprocessor supporting VFPv3

The memory system consists of the following components:

- Level 1 cache:
  - Instruction (32 Kbyte)
  - Data (32 Kbyte)
- Level 2 cache:
  - Unified instruction and data (256 Kbyte)
- Level 2 (internal) memory:
  - Boot ROM, including HAB (96 Kbyte)
  - Internal multimedia/shared, fast access RAM (128 Kbyte)
- External memory interfaces:
  - 16/32-bit DDR2-533, LPDDR2-533, or LPDDR1-400 up to a total of 2 GByte
  - 8-bit NAND SLC/MLC Flash with up to 100 MHz synchronous clock rate and up to 32-bit hardware ECC for 1 Kbyte block size
  - 16/32-bit NOR Flash with a dedicated 16-bit muxed-mode interface. I/O muxing logic selects EIMv2 port as primary muxing at system boot.
  - 16-bit PSRAM, Cellular RAM
  - Managed NAND, including eMMC up to rev 4.4

The i.MX50 introduces a next generation system bus fabric architecture that aggregates various sub-system buses and masters for access to system peripherals and memories. The various bus-systems and components are as follows:

- 64-bit AXI Fabric (266 MHz)—This bus-fabric is the SoC's central bus aggregation point.
  - Provides access to all slave targets in the SoC:
    - ROM (ROMCP)
    - On-chip RAM (OCRAM)
    - External DRAM (DRAM MC)
    - External static RAM (EIM)
    - Interrupt controller (TZIC)
    - Decode into the AHB MAX crossbar second level AHB fabric.
  - Provides arbitration to the following masters in the system:
    - ARM CPU complex
    - Pixel processing pipeline (ePXP)
    - Electrophoretic display controller (EPDC)
    - eLCDIF LCD display controller
    - DCP Crypto engine
    - BCH ECC engine
    - MAX AHB crossbar

Table 4. i.MX50 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SSI-1 SSI-2	I2S/SSI/AC97 Interface	Slave Connectivity Peripherals	The SSI is a full-duplex synchronous interface used on the i.MX50 processor to provide connectivity with off-chip audio peripherals. The SSI interfaces connect internally to the AUDMUX for mapping to external ports. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock/frame sync options. Each SSI has two pairs of 8 x 24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream, which reduces CPU overhead in use cases where two time slots are being used simultaneously.
Temperature Monitor	Temp Sensor	Analog	The temperature sensor is an internal module to the i.MX50 that monitors the die temperature.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface, ver. 2	Slave Connectivity Peripherals	Each of the UARTv2 modules supports the following serial data transmit/receive protocols and configurations: • 7 or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none) • Programmable bit-rates up to 4 Mbps. This is a higher max baud rate relative to the 1.875 Mbps, which is specified by the TIA/EIA-232-F standard. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps)
USB-OH-1	USB 2.0 High-Speed OTG-capable and Host ports	Master Connectivity Peripherals	USB-OH-1 supports USB2.0 HS/FS/LS, and contains: • One high-speed OTG-capable module with integrated HS USB PHY • One high-speed Host module with integrated HS USB PHY
WDOG-1	Watch Dog	Timer Peripherals	The Watchdog (WDOG) timer module protects against system failures by providing a method of escaping from unexpected events or programming errors. The WDOG Timer supports two comparison points during each counting period. Each of the comparison points is configurable to invoke an interrupt to the ARM core, and a second point invokes an external event on the WDOG line.
XTALOSC	Crystal Oscillator I/F	Clocking	The XTALOSC module combined with an external 24 MHz crystal with load capacitors implements a crystal oscillator.

3.1 Special Signal Considerations

Table 5 lists special signal considerations for the i.MX50. The signal names are listed in alphabetical order. The package contact assignments are found in Section 5, "Package Information and Contact Assignments." The signal descriptions are defined in the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM).

Table 5. Special Signal Considerations

Signal Name	Remarks
BOOT_MODE0, BOOT_MODE1	These two input pins are sampled out of reset and set the boot mode. For Internal boot, they should be set to 00. For Internal Fuse Only boot, they should be set to 10. For USB downloader, they should be set to 11. The BOOTMODE pins are in the NVCC_RESET domain and include an internal 100K pull-up resistor at start-up.
BOOT_CONFIG1[7:0], BOOT_CONFIG2[7:0], BOOT_CONFIG3[7:0]	These 24 pins are the GPIO boot override pins and may be driven at power up to select the boot mode. They are sampled 4 x CKIL clock cycles after POR is de-asserted. Consult the "System Boot" chapter of the Reference Manual for more details. Note that these are not dedicated pins: the BOOT_CONFIG pins appear over 24 pins of the EIM interface.
BT_LPB_FREQ[1:0]	If the LOW_BATT_GPIO (UART4_TXD) is asserted at power up, the BT_LPB_FREQ[1:0] pins will be sampled to determine the ARM core frequency. Consult the "System Boot" chapter of the Reference Manual for more details. Note that these are not dedicated pins: BT_LPB_FREQ0 appears on SSI_TXFS and BT_LPB_FREQ1 appears on SSI_TXC.
CHGR_DET_B	This is the USB Charger Detect pin. It is an open drain output pin that expects a 100 K pull-up. This pin is asserted low when a USB charger is detected on the OTG PHY DP and DM. This detection occurs with the application of VBUS. This pin is a raw sensor output and care must be taken to follow the system timings outlined in the USB charger specification Rev 1.1. The maximum current leakage at this pin is 8.5 μA. This pin can be controlled by software control as well. If not used, this pin should be tied to ground or left floating.
CKIH	This is an input to the CAMPs (Clock Amplifiers), which include on-chip AC-coupling precluding the need for external coupling capacitors. The CAMPs are enabled by default, but the main clocks feeding the on-chip clock tree are sourced from XTAL/EXTAL by default. Optionally, the use of a low jitter external oscillators to feed CKIH (while not required) can be an advantage if low jitter or special frequency clock sources are required by modules sourced by CKIH. See CCM chapter in the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM) for details on the respective clock trees. After initialization, the CAMPs may be disabled if not used by programming the CCR CAMPx_EN field. If disabled, the on-chip CAMP output is low and the input is irrelevant. CKIH is on the NVCC_JTAG power domain, so the input clock amplitude should not exceed NVCC_JTAG. If unused, the user should tie CKIH to GND for best practice.
CKIL/ECKIL	The user must tie a fundamental mode 32.768 K crystal across ECKIL and CKIL. The target ESR should be 50 K or less. The bias resistor for the amplifier is integrated and approximately 14 MΩ. The target load capacitance for the crystal is approximately 10 pF. The load capacitors on the board should be slightly less than double this value after taking parasitics into account. While driving in an external 32 KHz signal into ECKIL, CKIL should be left floating so that it biases. A differential amplifier senses these two pins to propagate the clock inside the i.MX508. Care must be taken to minimize external leakages on ECKIL and CKIL. If they are significant to the 14 MΩ feedback or 1 μA, then loss of oscillation margin or cessation of oscillation may result.

Table 5. Special Signal Considerations (continued)

Signal Name	Remarks
USB_H1_VBUS, USB_OTG_VBUS	These inputs are used by the i.MX50 to detect the presence and level of USB 5 V. If either VBUS input pin is connected to an external USB connector, there is a possibility that a fast 5 V edge rate during a cable attach could trigger the VBUS input ESD protection, which could result in damage to the i.MX50 silicon. To prevent this, the system should use some circuitry to prevent the 5 V edge rate from exceeding 5.25 V / 1 μs. Freescale recommends the use of a low pass filter consisting of 100 Ω resistor in series and a 1 μF capacitor close to the i.MX50 pin. In the case when the USB interface is connected on an on-board USB device (for example, 3G modem), the corresponding USB_VBUS pin may be left floating.
VREF	This pin is the DRAM MC reference voltage input. For LPDDR2 and DDR2, this pin should be connected to ½ of NVCC_EMI_DRAM. For LPDDR1, this pin should be left floating. The user may generate VREF using a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_EMI_DRAM. Shunt each resistor with a closely-mounted 0.1 μF capacitor.
WDOG_B	This output can be used to reset the system PMIC when the i.MX50 processor is locked up. This output is in the NVCC_MISC domain.
WDOG_RST_B_DEB	This output may be used to drive out the internal system reset signal to the system reset controller. This is only intended for debug purposes.
XTAL/EXTAL	These pins are the 24 MHz crystal driver as well as the external 24 MHz clock input. If using these pins to directly drive a 24 MHz crystal: • The user should tie a 24 MHz fundamental-mode crystal across XTAL and EXTAL. • The crystal must be rated for a maximum drive level of 100 μW or higher. • The recommended crystal ESR (equivalent series resistance) is 80 Ω or less. If using these pins as a clock input from an external 24 MHz oscillator: • The crystal may be eliminated and EXTAL driven directly driven by the external oscillator. The clock signal level on EXTAL must swing from NVCC_SRTC to GND. • In this configuration, the XTAL pin must be floated and the COSC_EN bit (bit 12 in the CCR register in the Clock Control Module) must be cleared to put the on-chip oscillator circuit in bypass mode which allows EXTAL to be externally driven. • Note there are strict jitter requirements if using an external oscillator in a USB application: < 50 ps peak-to-peak below 1.2 MHz and < 100 ps peak-to-peak above 1.2 MHz for the USB PHY.

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics of the i.MX50 processor.

NOTE

These electrical specifications are preliminary. These specifications are not fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications are published after thorough characterization and device qualifications have been completed.

Table 7. Absolute Maximum Ratings (continued)

Parameter Description	Symbol	Min	Max	Unit
ESD damage immunity: Human Body Model (HBM) Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	V
Storage temperature range	$T_{STORAGE}$	–40	125	°C

1 The term OVDD in this section refers to the associated supply rail of an input or output. The maximum range can be superseded by the DC tables.

4.1.2 Thermal Resistance Data

4.1.2.1 13 x 13 mm MAPBGA Package Thermal Resistance Data

Table 8 provides thermal resistance data for a 13 x 13 mm MAPBGA package.

Table 8. 13 x 13 mm MAPBGA Package Thermal Resistance Data

Rating	Board	Symbol	Value	Unit
Junction to Ambient (natural convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	51	°C/W
Junction to Ambient (natural convection)[1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	28	°C/W
Junction to Ambient (at 200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	40	°C/W
Junction to Ambient (at 200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	24	°C/W
Junction to Board[4]	—	$R_{\theta JB}$	14	°C/W
Junction to Case[5]	—	$R_{\theta JC}$	9	°C/W
Junction to Package Top (natural convection)[6]	—	Ψ_{JT}	2	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per JEDEC JESD51-2 with the single layer board horizontal. The thermal test board meets JESD51-9 specification.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by using the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

[1] Vin(dc) specifies the allowable dc excursion of each differential input.

[2] Vid(dc) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “pure” input level and Vcp is the “complementary” input level. the minimum value is equal to Vih(dc) - Vil(dc).

[3] Typ condition: typ model, 1.8 V, and 25 °C. Max condition: BCS model, 1.9 V, and 105 °C. Min condition: WCS model, 1.7 V, and -20 °C.

4.3.5 Low Voltage I/O (LVIO) DC Parameters

The parameters in Table 22 are guaranteed per the operating ranges in Table 11, unless otherwise noted.

Table 22. LVIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	MIN	Typ	MAX	Units
High-level output voltage	Voh	Ioh=-1mA Ioh=spec’ed Drive	OVDD-0.15 0.8*OVDD	—	—	V
Low-level output voltage	Vol	Iol=1mA Iol=specified Drive	—	—	0.15 0.2*OVDD	V
High-level output current	I Ioh	Voh=0.8*OVDD Low Drive Medium Drive High Drive Max Drive	 -2.1 -4.2 -6.3 -8.4	—	—	 mA
Low-level output current	I Iol	Vol=0.2*OVDD Low Drive Medium Drive High Drive Max Drive	 2.1 4.2 6.3 8.4	—	—	 mA
High-Level DC input voltage [1]	VIH	—	0.7*OVDD	—	OVDD	V
Low-Level DC input voltage	VIL	—	0V	—	0.3*OVDD	V
Input Hysteresis	VHYS	OVDD=1.875 OVDD=2.775	0.35	0.62 1.27	—	V
Schmitt trigger VT+ [2]	VT+	—	0.5*OVDD	—	—	V
Schmitt trigger VT-	VT-	—	—	—	0.5*OVDD	V
Pull-up resistor (22 KΩ PU)	Rpu	Vi=OVDD/2	20	24	28	KΩ
Pull-up resistor (47 KΩ PU)	Rpu	Vi=OVDD/2	43	51	59	KΩ
Pull-up resistor (100 KΩ PU)	Rpu	Vi=OVDD/2	91	108	125	KΩ
Pull-down resistor (100 KΩ PD)	Rpd	Vi=OVDD/2	91	108	126	KΩ
Input current (no pull-up/down)	IIN	VI = 0 VI=OVDD	—	1.7	250 120	nA
Input current (22 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	161 0.12	µA
Input current (47 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	76 0.12	µA
Input current (100 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	36 0.12	µA

4.4.3 HVIO Output Buffer Impedance

Table 26 shows the HVIO output buffer impedance of the i.MX50 processor.

Table 26. HVIO Output Buffer Impedance

Parameter	Symbol	Test Conditions	Min		Typ		Max		Unit
			OVDD 1.95 V	OVDD 3.3 V	OVDD 1.875 V	OVDD 3.30V	OVDD 1.65 V	OVDD 2.68 V	
Output driver impedance	Rpu	Low drive strength, Ztl = 150 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω	113.5 56.2 37.8	103.8 51.9 35.1	130.6 66 45.9	133 69.2 41	219.4 109.7 73.1	212.2 111.1 71.8	Ω
Output driver impedance	Rpd	Low drive strength, Ztl =1 50 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω	78.5 39.7 26.8	70 34.5 23	113.6 56.8 38.3	102 50 33.3	230.8 115.4 76.9	179.5 89.8 60.7	Ω

NOTE

Output driver impedance is measured with *long* transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 3).

Table 31. HVIO I/O Low Voltage (1.8 V) AC Parameters (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Slew Rate (High Drive)[1]	tr, tf	15 pF 35 pF	0.54/0.50 0.29/0.28			V/ns
Output Pad Slew Rate (Medium Drive)	tr, tf	15 pF 35 pF	0.40/0.38 0.20/0.19			V/ns
Output Pad Slew Rate (Low Drive)	tr, tf	15 pF 35 pF	0.22/0.21 0.10/0.10			V/ns
Output Pad di/dt (High Drive)	tdit				34	mA/ns
Output Pad di/dt (Medium drive)	tdit				22	mA/ns
Output Pad di/dt (Low drive)	tdit				11	mA/ns
Input Transition Times[2]	trm				25	ns

1 tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

2 Hysteresis mode is recommended for inputs with transition time greater than 25 ns.

4.5.6 HVIO I/O High Voltage (3.0 V) AC Parameters

Table 32 shows the AC parameters for HVIO I/O High Voltage (3.0 V).

Table 32. HVIO I/O High Voltage (3.0 V) AC Parameters

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (High Drive)	tpr	15 pF 35 pF			2.16/1.79 3.75/3.28	ns
Output Pad Transition Times (Medium Drive)	tpr	15 pF 35 pF			2.81/2.40 5.06/4.58	ns
Output Pad Transition Times (Low Drive)	tpr	15 pF 35 pF			4.69/4.15 8.91/8.51	ns
Output Pad Slew Rate (High Drive)[1]	tps	15 pF 35 pF	0.75/0.90 0.43/0.49			V/ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0.57/0.67 0.32/0.35			V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0.34/0.39 0.18/0.19			V/ns
Output pad di/dt (High drive)	tdit	—	—	—	55	mA/ns
Output pad di/dt (Medium drive)	tdit	—	—	—	36	mA/ns
Output pad di/dt (Low drive)	tdit	—	—	—	16	mA/ns
Input transition times[2]	trm	—	—	—	25	ns

1 tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

2 Hysteresis mode is recommended for inputs with transition time greater than 25 ns.

Table 37. WDOG_RST_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC5	Duration of WDOG_RST_B Assertion	1	—	T_{CKIL}

NOTE

CKIL is approximately 32 kHz. T_{CKIL} is one period or approximately 30 µs.

4.6.3 Clock Amplifier Parameters (CKIH)

The input to clock amplifier (CAMP) is internally ac-coupled allowing direct interface to a square wave or sinusoidal frequency source. No external series capacitors are required.

Table 38 shows the electrical parameters of CAMP.

Table 38. CAMP Electrical Parameters (CKIH)

Parameter	Min	Typ	Max	Unit
Input frequency	8.0	—	40.0	MHz
VIL (for square wave input)	0	—	0.3	V
VIH (for square wave input)	(VCC[1] – 0.25)	—	3	V
Sinusoidal input amplitude	0.4 [2]	—	VDD	Vp-p
Output duty cycle	45	50	55	%

1 VCC is the supply voltage of CAMP.

2 This value of the sinusoidal input is determined during characterization.

4.6.4 DPLL Electrical Parameters

Table 39 shows the electrical parameters of digital phase-locked loop (DPLL).

Table 39. DPLL Electrical Parameters

Parameter	Test Conditions/Remarks	Min	Typ	Max	Unit
Reference clock frequency range[1]	—	10	—	100	MHz
Reference clock frequency range after pre-divider	—	10	—	40	MHz
Output clock frequency range (dpdck_2)	—	300	—	1025	MHz
Pre-division factor[2]	—	1	—	16	—
Multiplication factor integer part	—	5	—	15	—
Multiplication factor numerator[3]	Should be less than denominator	–67108862	—	67108862	—
Multiplication factor denominator[2]	—	1	—	67108863	—
Output duty cycle	—	48.5	50	51.5	%

Table 41. Source Synchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF24	postamble delay	t_{POST}	POST_DELAY*t_{CK}	—	ns
NF25	CLE and ALE setup time	t_{CALS}	0.5*t_{CK}	—	ns
NF26	CLE and ALE hold time	t_{CALH}	0.5*t_{CK}	—	ns
NF27	Data input to first DQS latching transition	t_{DQSS}	t_{CK}	—	ns

1 GPMI's sync mode output timing could be controlled by module's internal register, say HW_GPMI_TIMING2_CE_DELAY, HW_GPMI_TIMING_PREAMBLE_DELAY, and HW_GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers' setting. In the above table, we use CE_DELAY/PRE_DELAY/POST_DELAY representing these settings each.

4.6.5.3 Samsung Toggle Mode AC Timing

4.6.5.3.1 Command and Address Timing

NOTE

Samsung Toggle Mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. Please refer to the above chapter for details.

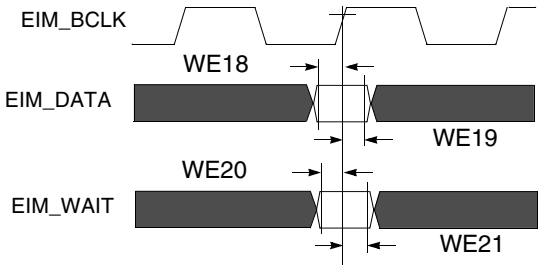

Figure 18. EIM Inputs Timing Diagram

4.9.2.2 CSPI Slave Mode Timing

Figure 33 depicts the timing of CSPI in slave mode. Table 51 lists the CSPI slave mode timing characteristics.

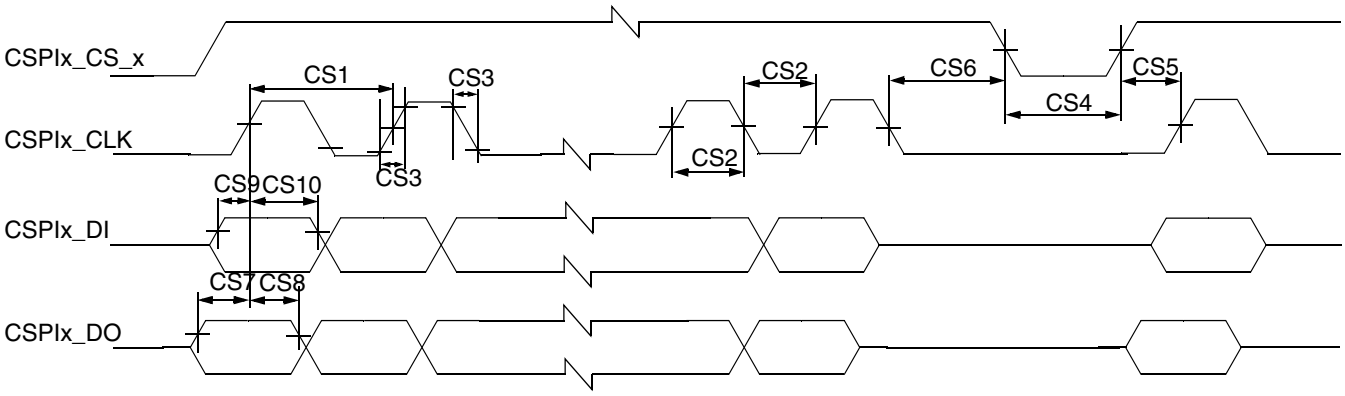

Figure 33. CSPI Slave Mode Timing Diagram

Table 51. CSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	CSPIx_CLK Cycle Time	t_{clk}	60	—	ns
CS2	CSPIx_CLK High or Low Time	t_{SW}	15	—	ns
CS3	CSPIx_CLK Rise or Fall	$t_{RISE/FALL}$	—	—	ns
CS4	CSPIx_CS_x pulse width	t_{CSLH}	30	—	ns
CS5	CSPIx_CS_x Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	CSPIx_CS_x Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	CSPIx_DO Setup Time	t_{Smosi}	5	—	ns
CS8	CSPIx_DO Hold Time	t_{Hmosi}	5	—	ns
CS9	CSPIx_DI Setup Time	t_{Smiso}	5	—	ns
CS10	CSPIx_DI Hold Time	t_{Hmiso}	5	—	ns

4.9.2.3 eCSPI Master Mode Timing

Figure 34 depicts the timing of eCSPI in master mode and Table 52 lists the eCSPI master mode timing characteristics.

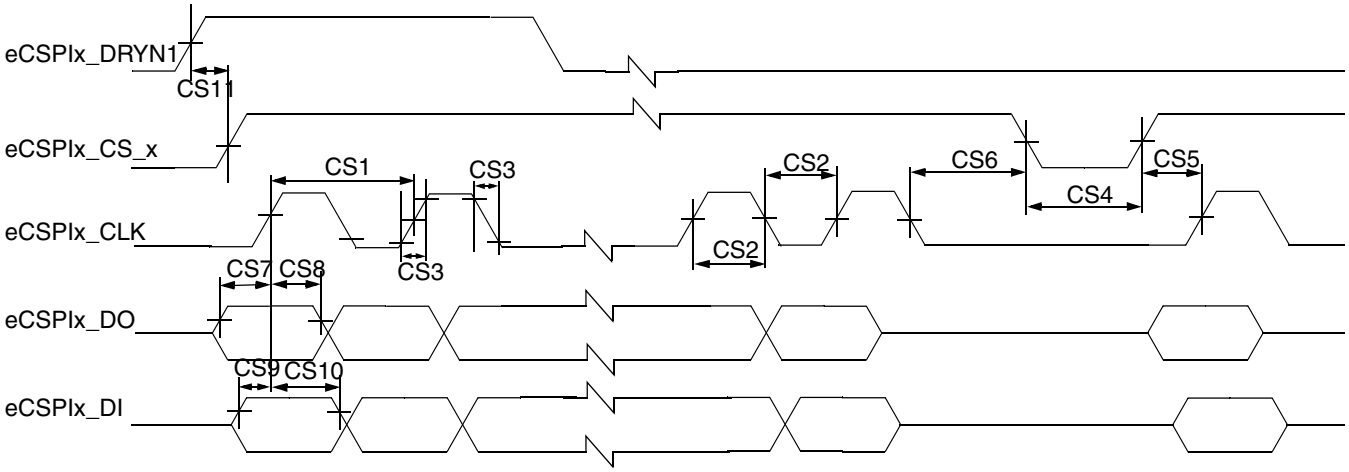

Figure 34. eCSPI Master Mode Timing Diagram

Table 52. eCSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	eCSPIx_CLK Cycle Time–Read eCSPIx_CLK Cycle Time–Write	t_{clk}	60 15	—	ns
CS2	eCSPIx_CLK High or Low Time	t_{SW}	6	—	ns
CS3	eCSPIx_CLK Rise or Fall	$t_{RISE/FALL}$	—	—	ns
CS4	eCSPIx_CS_x pulse width	t_{CSLH}	15	—	ns
CS5	eCSPIx_CS_x Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	eCSPIx_CS_x Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	eCSPIx_DO Setup Time	t_{Smosi}	5	—	ns
CS8	eCSPIx_DO Hold Time	t_{Hmosi}	5	—	ns
CS9	eCSPIx_DI Setup Time	t_{Smiso}	5	—	ns
CS10	eCSPIx_DI Hold Time	t_{Hmiso}	5	—	ns
CS11	eCSPIx_DRYN Setup Time	t_{SDRY}	5	—	ns

4.9.9.4 SSI Receiver Timing with External Clock

Figure 54 depicts the SSI receiver external clock timing and Table 69 lists the timing parameters for the receiver timing with external clock.

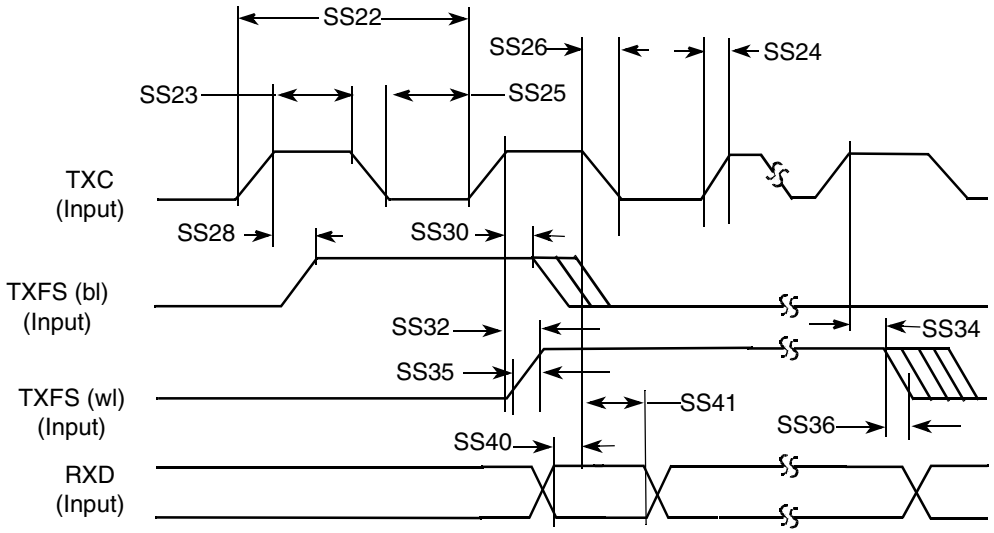

Figure 54. SSI Receiver External Clock Timing Diagram

Table 69. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	(Rx) CK high to FS (bl) high	–10	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10	—	ns
SS32	(Rx) CK high to FS (wl) high	–10	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10	—	ns
SS41	SRXD hold time after (Rx) CK low	2	—	ns

5.3.1 400 MAPBGA 17 x 17 mm Package Views

Figure 65 shows the top view of the 17 x 17 mm package, Figure 66 shows the bottom view of the package, and Figure 67 shows the side view of the package.

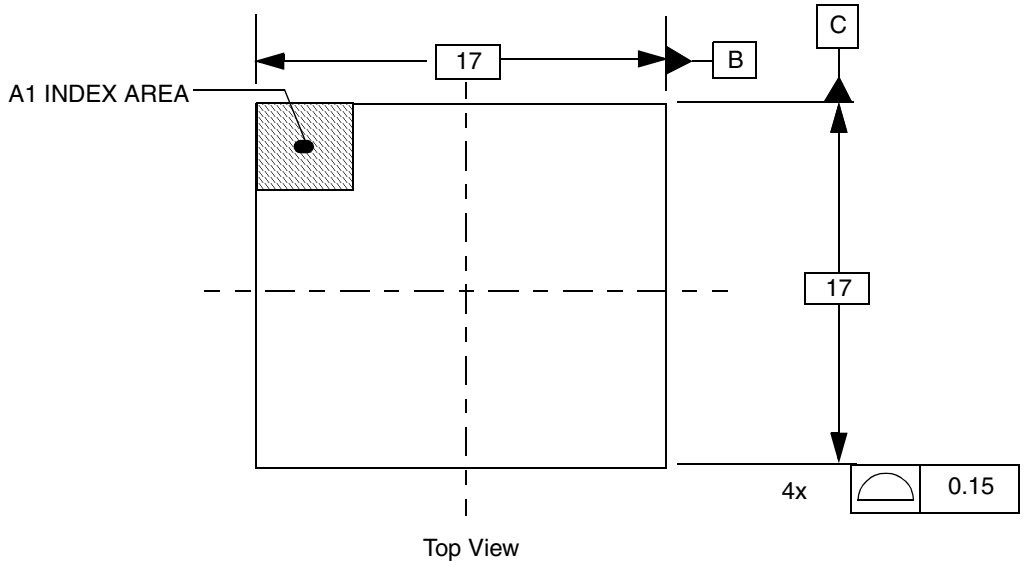

Figure 65. 400 MAPBGA 17x17 mm Package Top view

5.3.3 400 MAPBGA 17 x 17 Power Rails

Table 84. 400 MAPBGA 17x17 Ground, Power, Sense, and Reference Contact Signals

Pin Name	Ball Number
NC	A1 Y1 A20 Y20
NVCC_EIM	F6 F7 F8
NVCC_EMI_DRAM	K14 N14 J15 K15 L15 N15 P15 H16 J16 K16 L16 M16 N16 P16 R16
NVCC_EPDC	F9 F10 F11 F12
NVCC_JTAG	P9
NVCC_KEYPAD	H5
NVCC_LCD	P10
NVCC_MISC	J5
NVCC_NANDF	P11 P12
NVCC_RESET	P6
NVCC_SD1	N5
NVCC_SD2	P5
NVCC_SPI	M5
NVCC_SRTC	R5
NVCC_SSI	K5
NVCC_UART	L5
USB_H1_VDDA25	Y9
USB_H1_VDDA33	W11
USB_OTG_VDDA25	W9
USB_OTG_VDDA33	Y11
VCC	K10 L10 M10 K11 L11 M11 J12 K12 L12
VDD1P2	U6
VDD1P8	V6
VDD2P5	V5
VDD3P0	U5
VDDA	K9 J11
VDDAL1	J9 J10
VDDGP	G6 H6 J6 K6 L6 G7 H7 J7 K7 G8 H8 G9 H9 G10 H10
VDDO25	L17
VSS	T5 W5 M6 N6 L7 M7 N7 P7 J8 K8 L8 M8 N8 P8 L9 M9 N9 N10 R10 G11 H11 N11 R11 G12 H12 M12 N12 R12 G13 H13 J13 K13 L13 M13 N13 P13 R13 G14 H14 J14 L14 M14 P14 R14 H15 M15 R15

Table 84. 400 MAPBGA 17x17 Ground, Power, Sense, and Reference Contact Signals (continued)

VDD_DCDCI	R7
VDD_DCDCO	T6
GND_DCDC	R6

5.4 Signal Assignments

Table 85. Alphabetical List of Signal Assignments

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
BOOT_MODE0	AB1	AB1	V3	NVCC_RESET	LVIO	ALT0	IN	100K PU
BOOT_MODE1	AB2	AB2	U3	NVCC_RESET	LVIO	ALT0	IN	100K PU
CHGR_DET_B	V11	AA15	T10	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG25	—	OUT-OD	—
CKIH	AA6	AA6	V4	NVCC_JTAG	ANALOG	—	—	—
CKIL	Y1	Y1	Y4	NVCC_SRTC	ANALOG	—	—	—
CSPI_MISO	M5	H2	K4	NVCC_SPI	HVIO	ALT1	IN	Keeper
CSPI_MOSI	M2	J1	L3	NVCC_SPI	HVIO	ALT1	IN	Keeper
CSPI_SCLK	M1	H1	M1	NVCC_SPI	HVIO	ALT1	IN	Keeper
CSPI_SS0	M4	J2	J4	NVCC_SPI	HVIO	ALT1	IN	Keeper
DISP_BUSY	AC12	AA21	U11	NVCC_LCD	HVIO	ALT1	IN	Keeper
DISP_CS	AD14	AC21	T12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D0	AA12	AC17	V11	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D1	Y12	AC16	T11	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D10	Y17	AD22	Y16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D11	V12	AD19	W14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D12	V13	AC22	V14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D13	V14	AC23	T13	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D14	V15	AB23	U14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D15	V16	AD21	Y15	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D2	AA13	AD15	W12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D3	Y13	AC15	W13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D4	AA14	AC24	Y13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D5	Y14	AB24	U13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
DRAM_DQM0	T24	M18	N17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_DQM1	J24	L18	F17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_DQM2	AC24	Y16	U20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_DQM3	B24	G17	D20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_OPEN	J18	—	H18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_OPENFB	H18	—	H17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_RAS	H21	—	E20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	Keeper
DRAM_SDBA0	K18	—	J20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDBA1	L18	—	H20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDBA2	N18	—	M19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDCKE	U20	T5	R18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDCLK_0	N24	R5	J17	NVCC_EMI_DRAM	DRAMCLK	ALT0	OUT-LO	Keeper
DRAM_SDCLK_0_B	M24	P5	J18	NVCC_EMI_DRAM	DRAMCLK	ALT0	OUT-HI	—
DRAM_SDCLK_1	T20	—	—	NVCC_EMI_DRAM	DRAMCLK	ALT0	OUT-LO	Keeper
DRAM_SDCLK_1_B	R20	—	—	NVCC_EMI_DRAM	DRAMCLK	ALT0	OUT-HI	—
DRAM_SDODT0	G18	—	K18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDODT1	R18	—	—	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDQS0	P23	N18	M17	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS0_B	P24	P18	M18	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS1	L23	J20	G17	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS1_B	L24	K18	G18	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS2	AB23	Y15	T19	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS2_B	AB24	V15	T20	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS3	C23	E16	C19	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS3_B	C24	G16	C20	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDWE	P18	—	L18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	Keeper
ECKIL	Y2	Y2	W4	NVCC_SRTC	ANALOG	—	—	—
ECSPI1_MISO	N7	K4	M3	NVCC_SPI	HVIO	ALT1	IN	Keeper
ECSPI1_MOSI	N2	N4	M4	NVCC_SPI	HVIO	ALT1	IN	Keeper

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
EPDC_PWRCTRL2	G14	F23	E12	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_PWRCTRL3	G15	L21	F15	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_PWRSTAT	G16	F24	C12	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE0	D13	N24	B12	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE1	E13	P24	A12	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE2	D12	H21	C11	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE3	E12	J21	E8	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE4	D11	K21	D10	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCE5	E11	D18	E6	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCLK	A13	K24	B13	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDCLKN	B13	L24	D12	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDLE	D18	M24	C15	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDOE	E18	V21	C13	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDOED	D19	R23	G16	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDOEZ	E19	U21	F16	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_SDSHR	A10	H23	A8	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_VCOM0	G17	H24	B14	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPDC_VCOM1	D20	W21	G15	NVCC_EPDC	HVIO	ALT1	IN	Keeper
EPITO	G4	D8	F5	NVCC_MISC	HVIO	ALT1	IN	Keeper
EXTAL	AC5	AC5	W6	VDD2P5	ANALOG	—	—	—
GND_KEL	AA7	AA7	T7	VDD2P5	ANALOG	—	—	—
I2C1_SCL	E1	A6	E1	NVCC_MISC	HVIO	ALT1	IN	Keeper
I2C1_SDA	E2	B7	E2	NVCC_MISC	HVIO	ALT1	IN	Keeper
I2C2_SCL	F1	A5	F1	NVCC_MISC	HVIO	ALT1	IN	Keeper
I2C2_SDA	F2	B6	F2	NVCC_MISC	HVIO	ALT1	IN	Keeper
I2C3_SCL	G1	A4	G1	NVCC_MISC	HVIO	ALT1	IN	Keeper
I2C3_SDA	G2	B5	G2	NVCC_MISC	HVIO	ALT1	IN	Keeper
JTAG_MOD	V7	V5	T8	NVCC_JTAG	GPIO	ALT0	IN	100K PU
JTAG_TCK	W4	W4	R8	NVCC_JTAG	GPIO	ALT0	IN	100K PD

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
UART2_RTS	L2	C2		NVCC_UART	HVIO	ALT1	IN	Keeper
UART2_RXD	L1	C1	L2	NVCC_UART	HVIO	ALT1	IN	Keeper
UART2_TXD	K1	B1	L1	NVCC_UART	HVIO	ALT1	IN	Keeper
UART3_RXD	L4	E4	K3	NVCC_UART	HVIO	ALT1	IN	Keeper
UART3_TXD	K4	D4	J2	NVCC_UART	HVIO	ALT1	IN	Keeper
UART4_RXD	L5	D5	J3	NVCC_UART	HVIO	ALT1	IN	Keeper
UART4_TXD	K5	D6	H2	NVCC_UART	HVIO	ALT1	IN	Keeper
USB_H1_DN	AC10	AC10	W10	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	—	—
USB_H1_DP	AD10	AD10	Y10	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	—	—
USB_H1_GPANAIO	Y11	AA17	U10	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG25	—	—	—
USB_H1_RREFEXT	AA10	AA10	U9	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG25	—	—	—
USB_H1_VBUS	Y10	AA16	V9	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	—	—
USB_OTG_DN	AC8	AC8	W8	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG50	—	—	—
USB_OTG_DP	AD8	AD8	Y8	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG50	—	—	—
USB_OTG_GPANAIO	Y7	AA14	V7	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	—	—
USB_OTG_ID	Y8	AA12	Y7	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	—	—
USB_OTG_RREFEXT	AA8	AA8	W7	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	—	—
USB_OTG_VBUS	Y9	AA13	V8	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG50	—	—	—
VREF	M23	M23	K17	VDDO25	ANALOG	—	—	—
WDOG	G5	D9	F4	NVCC_MISC	HVIO	ALT1	IN	—
XTAL	AD5	AD5	Y6	VDD2P5	ANALOG	—	—	—