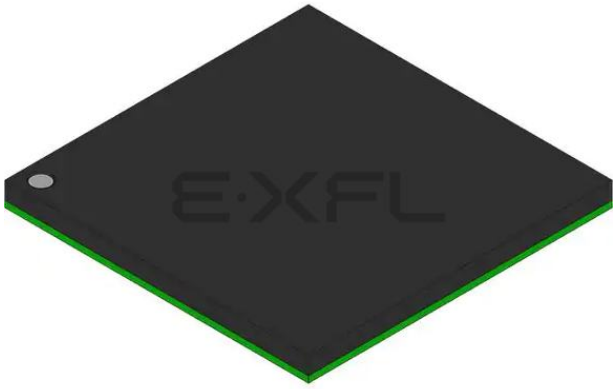

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	EPDC, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Boot Security, Cryptography, Secure JTAG
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx508cvm8br2

Table 4. i.MX50 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SDMA	Smart Direct Memory Access	Master Connectivity Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by offloading various cores in dynamic data routing. The SDMA features list is as follows: • Powered by a 16-bit instruction-set micro-RISC engine • Multi-channel DMA supports up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM Cortex-A8 and SDMA • Very fast context-switching with two-level priority-based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle uni-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers for EMI • Support of byte-swapping and CRC calculations • A library of scripts and API is available
SJC	Secure JTAG Controller	System Control Peripherals	The Secure JTAG Controller provides a mechanism for regulating JTAG access, preventing unauthorized JTAG usage while allowing JTAG access for manufacturing tests and software debugging. The i.MX50 JTAG port provides debug access to several hardware blocks including the ARM processor and the system bus, therefore, it must be accessible for initial laboratory bring-up, manufacturing tests and troubleshooting, and for software debugging by authorized entities. However, if the JTAG port is left unsecured it provides a method for executing unauthorized program code, getting control over secure applications, and running code in privileged modes. The Secure JTAG controller provides three different security modes that can be selected through an e-fuse configuration to prevent unauthorized JTAG access.
SPBA	Shared Peripheral Bus Arbiter	System Control Peripherals	SPBA (Shared Peripheral Bus Arbiter) is a two-to-one IP bus interface (IP bus) arbiter.
SRTC	Secure Real Time Clock	Security Peripherals	The SRTC incorporates a special System State Retention Register (SSRR) that stores system parameters during system shutdown modes. This register and all SRTC counters are powered by dedicated supply rail NVCC_SRTC. The NVCC_SRTC can be energized separately even if all other supply rails are shut down. This register is helpful for storing warm boot parameters. The SSRR also stores the system security state. In case of a security violation, the SSRR marks the event (security violation indication).

Table 4. i.MX50 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SSI-1 SSI-2	I2S/SSI/AC97 Interface	Slave Connectivity Peripherals	The SSI is a full-duplex synchronous interface used on the i.MX50 processor to provide connectivity with off-chip audio peripherals. The SSI interfaces connect internally to the AUDMUX for mapping to external ports. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock/frame sync options. Each SSI has two pairs of 8 x 24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream, which reduces CPU overhead in use cases where two time slots are being used simultaneously.
Temperature Monitor	Temp Sensor	Analog	The temperature sensor is an internal module to the i.MX50 that monitors the die temperature.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface, ver. 2	Slave Connectivity Peripherals	Each of the UARTv2 modules supports the following serial data transmit/receive protocols and configurations: • 7 or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none) • Programmable bit-rates up to 4 Mbps. This is a higher max baud rate relative to the 1.875 Mbps, which is specified by the TIA/EIA-232-F standard. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps)
USB-OH-1	USB 2.0 High-Speed OTG-capable and Host ports	Master Connectivity Peripherals	USB-OH-1 supports USB2.0 HS/FS/LS, and contains: • One high-speed OTG-capable module with integrated HS USB PHY • One high-speed Host module with integrated HS USB PHY
WDOG-1	Watch Dog	Timer Peripherals	The Watchdog (WDOG) timer module protects against system failures by providing a method of escaping from unexpected events or programming errors. The WDOG Timer supports two comparison points during each counting period. Each of the comparison points is configurable to invoke an interrupt to the ARM core, and a second point invokes an external event on the WDOG line.
XTALOSC	Crystal Oscillator I/F	Clocking	The XTALOSC module combined with an external 24 MHz crystal with load capacitors implements a crystal oscillator.

Table 5. Special Signal Considerations (continued)

Signal Name	Remarks
USB_H1_VBUS, USB_OTG_VBUS	These inputs are used by the i.MX50 to detect the presence and level of USB 5 V. If either VBUS input pin is connected to an external USB connector, there is a possibility that a fast 5 V edge rate during a cable attach could trigger the VBUS input ESD protection, which could result in damage to the i.MX50 silicon. To prevent this, the system should use some circuitry to prevent the 5 V edge rate from exceeding 5.25 V / 1 μs. Freescale recommends the use of a low pass filter consisting of 100 Ω resistor in series and a 1 μF capacitor close to the i.MX50 pin. In the case when the USB interface is connected on an on-board USB device (for example, 3G modem), the corresponding USB_VBUS pin may be left floating.
VREF	This pin is the DRAM MC reference voltage input. For LPDDR2 and DDR2, this pin should be connected to ½ of NVCC_EMI_DRAM. For LPDDR1, this pin should be left floating. The user may generate VREF using a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_EMI_DRAM. Shunt each resistor with a closely-mounted 0.1 μF capacitor.
WDOG_B	This output can be used to reset the system PMIC when the i.MX50 processor is locked up. This output is in the NVCC_MISC domain.
WDOG_RST_B_DEB	This output may be used to drive out the internal system reset signal to the system reset controller. This is only intended for debug purposes.
XTAL/EXTAL	These pins are the 24 MHz crystal driver as well as the external 24 MHz clock input. If using these pins to directly drive a 24 MHz crystal: • The user should tie a 24 MHz fundamental-mode crystal across XTAL and EXTAL. • The crystal must be rated for a maximum drive level of 100 μW or higher. • The recommended crystal ESR (equivalent series resistance) is 80 Ω or less. If using these pins as a clock input from an external 24 MHz oscillator: • The crystal may be eliminated and EXTAL driven directly driven by the external oscillator. The clock signal level on EXTAL must swing from NVCC_SRTC to GND. • In this configuration, the XTAL pin must be floated and the COSC_EN bit (bit 12 in the CCR register in the Clock Control Module) must be cleared to put the on-chip oscillator circuit in bypass mode which allows EXTAL to be externally driven. • Note there are strict jitter requirements if using an external oscillator in a USB application: < 50 ps peak-to-peak below 1.2 MHz and < 100 ps peak-to-peak above 1.2 MHz for the USB PHY.

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics of the i.MX50 processor.

NOTE

These electrical specifications are preliminary. These specifications are not fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications are published after thorough characterization and device qualifications have been completed.

4.3.3 Low Power DDR2 I/O DC Parameters

The LPDDR2 interface fully complies with JEDEC standard release April, 2008. The parameters in Table 20 are guaranteed per the operating ranges in Table 11, unless otherwise noted.

Table 20. LPDDR2 I/O DC Electrical Parameters

DC Electrical Characteristics	Symbol	Test Conditions	MIN	TYP	MAX	Units
High-level output voltage	Voh	—	0.9*ovdd	—	—	V
Low-level output voltage	Vol	—	—	—	0.1*ovdd	V
Input reference voltage	Vref	—	0.49*ovdd	0.5*ovdd	0.51*ovdd	—
DC input high voltage	Vih(dc)	—	Vref+0.13	—	ovdd	V
DC input low voltage	Vil(dc)	—	ovss	—	Vref-0.13	V
Differential input logic high[1]	Vih(diff)	—	0.26	—	—	V
Differential input logic low[1]	Vil(diff)	—	—	—	-0.26	V
Input current (no pull-up/down)	Iin	VI = 0 VI=ovdd	—	0.02 1.5	12.8 290	nA
Tri-state I/O supply current[2]	Icc-ovdd	VI = ovdd or 0	—	1.85	400	nA
Tri-state 2.5 V predrivers supply current[2]	Icc-vdd2p5	VI = ovdd or 0	—	5	700	nA
Tri-state core supply current[2]	Icc-vddi	VI = ovdd or 0	—	3	700	nA
Pullup/Pulldown impedance mismatch[2]	—	—	-15	—	+15	%
240 Ω unit calibration resolution	—	—	—	—	10	Ω

1 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

2 Typ condition: typ model, 1.2V, and 25 °C. Max condition: BCS model, 1.3V, and 125 °C. Min condition: WCS model, 1.14V, and -40 °C.

4.3.4 Low Power DDR1 I/O DC Parameters

The LPDDR1 interface fully complies with JEDEC standard release April, 2008. The parameters in Table 21 are guaranteed per the operating ranges in Table 11, unless otherwise noted.

Table 21. LPDDR1 Mode DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	MIN	TYP	MAX	Units
High-level output voltage	Voh	Ioh=-0.1mA	0.9*ovdd	—	—	V
Low-level output voltage	Vol	Iol=0.1mA	—	—	0.1*ovdd	V
DC input high voltage (data pins)	Vihd(dc)	—	0.7*ovdd	—	ovdd+0.3	V
DC input low voltage (data pins)	Vild(dc)	—	-0.3	—	0.3*ovdd	V
DC input voltage[1] (clk pins)	Vin(dc)	—	-0.3	—	ovdd+0.3	V
DC input differential voltage[2]	Vid(dc)	—	0.4*ovdd	—	ovdd+0.6	V
Input current[3] (no pull-up/down)	Iin	VI = 0 VI=ovdd	—	0.07 2	5 360	nA
Tri-state I/O supply current[3]	Icc-ovdd	VI = ovdd or 0	—	2.3	480	nA
Tri-state 2.5V predrivers supply current[3]	Icc-vdd2p5	VI = ovdd or 0	—	5.3	680	nA
Tri-state core supply current[3]	Icc-vddi	VI = ovdd or 0	—	3.1	720	nA

[1] Vin(dc) specifies the allowable dc excursion of each differential input.

[2] Vid(dc) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “pure” input level and Vcp is the “complementary” input level. the minimum value is equal to Vih(dc) - Vil(dc).

[3] Typ condition: typ model, 1.8 V, and 25 °C. Max condition: BCS model, 1.9 V, and 105 °C. Min condition: WCS model, 1.7 V, and -20 °C.

4.3.5 Low Voltage I/O (LVIO) DC Parameters

The parameters in Table 22 are guaranteed per the operating ranges in Table 11, unless otherwise noted.

Table 22. LVIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	MIN	Typ	MAX	Units
High-level output voltage	Voh	Ioh=-1mA Ioh=spec’ed Drive	OVDD-0.15 0.8*OVDD	—	—	V
Low-level output voltage	Vol	Iol=1mA Iol=specified Drive	—	—	0.15 0.2*OVDD	V
High-level output current	I Ioh	Voh=0.8*OVDD Low Drive Medium Drive High Drive Max Drive	 -2.1 -4.2 -6.3 -8.4	—	—	 mA
Low-level output current	I Iol	Vol=0.2*OVDD Low Drive Medium Drive High Drive Max Drive	 2.1 4.2 6.3 8.4	—	—	 mA
High-Level DC input voltage [1]	VIH	—	0.7*OVDD	—	OVDD	V
Low-Level DC input voltage	VIL	—	0V	—	0.3*OVDD	V
Input Hysteresis	VHYS	OVDD=1.875 OVDD=2.775	0.35	0.62 1.27	—	V
Schmitt trigger VT+ [2]	VT+	—	0.5*OVDD	—	—	V
Schmitt trigger VT-	VT-	—	—	—	0.5*OVDD	V
Pull-up resistor (22 KΩ PU)	Rpu	Vi=OVDD/2	20	24	28	KΩ
Pull-up resistor (47 KΩ PU)	Rpu	Vi=OVDD/2	43	51	59	KΩ
Pull-up resistor (100 KΩ PU)	Rpu	Vi=OVDD/2	91	108	125	KΩ
Pull-down resistor (100 KΩ PD)	Rpd	Vi=OVDD/2	91	108	126	KΩ
Input current (no pull-up/down)	IIN	VI = 0 VI=OVDD	—	1.7	250 120	nA
Input current (22 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	161 0.12	µA
Input current (47 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	76 0.12	µA
Input current (100 KΩ PU)	IIN	VI = 0 VI=OVDD	—	—	36 0.12	µA

4.4.1 GPIO Output Buffer Impedance

Table 24 shows the GPIO output buffer impedance of the i.MX50 processor.

Table 24. GPIO Output Buffer Impedance

Parameter	Symbol	Test Conditions	Min	Typ		Max	Unit
				OVDD 2.775 V	OVDD 1.875V		
Output driver impedance	Rpu	Low drive strength, Ztl = 150 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω Max drive strength, Ztl = 37.5 Ω	80 40 27 20	104 52 35 26	150 75 51 38	250 125 83 62	Ω
Output driver impedance	Rpd	Low drive strength, Ztl = 150 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω Max drive strength, Ztl = 37.5 Ω	64 32 21 16	88 44 30 22	134 66 44 34	243 122 81 61	Ω

4.4.2 LVIO Output Buffer Impedance

Table 25 shows the LVIO output buffer impedance of the i.MX50 processor.

Table 25. LVIO Output Buffer Impedance

Parameter	Symbol	Test Conditions	Min	Typ		Max	Unit
				OVDD 2.775 V	OVDD 1.875V		
Output driver impedance	Rpu	Low drive strength, Ztl = 150 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω Max drive strength, Ztl = 37.5 Ω	80 40 27 20	104 52 35 26	150 75 51 38	250 125 83 62	Ω
Output driver impedance	Rpd	Low drive strength, Ztl = 150 Ω Medium drive strength, Ztl = 75 Ω High drive strength, Ztl = 50 Ω Max drive strength, Ztl = 37.5 Ω	64 32 21 16	88 44 30 22	134 66 44 34	243 122 81 61	Ω

Table 40. Asynchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T[2] = GPMI Clock Cycle[3]		Example Timing for GPMI Clock ≈ 100MHz T = 10ns		Unit
			Min.	Max.	Min.	Max.	
NF5	$\overline{WE}$ pulse width	tWP	DS*T		10		ns
NF6	ALE setup time	tALS	(AS+1)*T	—	10	—	ns
NF7	ALE hold time	tALH	(DH+1)*T	—	20	—	ns
NF8	Data setup time	tDS	DS*T	—	10	—	ns
NF9	Data hold time	tDH	DH*T	—	10	—	ns
NF10	Write cycle time	tWC	(DS+DH)*T		20		ns
NF11	$\overline{WE}$ hold time	tWH	DH*T		10		ns
NF12	Ready to $\overline{RE}$ low	tRR	(AS+1)*T	—	10	—	ns
NF13	$\overline{RE}$ pulse width	tRP	DS*T	—	10	—	ns
NF14	READ cycle time	tRC	(DS+DH)*T	—	20	—	ns
NF15	$\overline{RE}$ high hold time	tREH	DH*T		10	—	ns
NF16	Data setup on read	tDSR	N/A		10	—	ns
NF17	Data hold on read	tDHR	N/A		10	—	ns

1 GPMI's Async Mode output timing could be controlled by module's internal register, say HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers' setting. In the above table, we use AS/DS/DH representing these settings each.

2 T represents for the GPMI clock period.

3 AS minimum value could be 0, while DS/DH minimum value is 1.

Table 41. Source Synchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF24	postamble delay	t_{POST}	POST_DELAY*t_{CK}	—	ns
NF25	CLE and ALE setup time	t_{CALS}	0.5*t_{CK}	—	ns
NF26	CLE and ALE hold time	t_{CALH}	0.5*t_{CK}	—	ns
NF27	Data input to first DQS latching transition	t_{DQSS}	t_{CK}	—	ns

1 GPMI's sync mode output timing could be controlled by module's internal register, say HW_GPMI_TIMING2_CE_DELAY, HW_GPMI_TIMING_PREAMBLE_DELAY, and HW_GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers' setting. In the above table, we use CE_DELAY/PRE_DELAY/POST_DELAY representing these settings each.

4.6.5.3 Samsung Toggle Mode AC Timing

4.6.5.3.1 Command and Address Timing

NOTE

Samsung Toggle Mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. Please refer to the above chapter for details.

Table 43. EIM Bus Timing Parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	EIM_BCLK Cycle time[2]	t	—	2t	—	3t	—	4t	—
WE2	EIM_BCLK Low Level Width	0.4t	—	0.8t	—	1.2t	—	1.6t	—
WE3	EIM_BCLK High Level Width	0.4t	—	0.8t	—	1.2t	—	1.6t	—
WE4	Clock rise to address valid[3]	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE5	Clock rise to address invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE6	Clock rise to EIM_CSx valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE7	Clock rise to EIM_CSx invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE8	Clock rise to EIM_RW valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE9	Clock rise to EIM_RW invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE10	Clock rise to EIM_OE valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE11	Clock rise to EIM_OE invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE12	Clock rise to EIM_EBx valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE13	Clock rise to EIM_EBx invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE14	Clock rise to EIM_LBA valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE15	Clock rise to EIM_LBA invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE16	Clock rise to Output Data valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	2t – 1.25	2t + 1.75
WE17	Clock rise to Output Data Invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	2t – 1.25	2t + 1.75
WE18	Input Data setup time to Clock rise	2	—	2	—	2	—	2	—
WE19	Input Data hold time from Clock rise	2.5	—	2.5	—	2.5	—	2.5	—
WE20	EIM_WAIT setup time to Clock rise	2	—	2	—	2	—	2	—
WE21	EIM_WAIT hold time from Clock rise	2.5	—	2.5	—	2.5	—	2.5	—

1 *t* is axi_clk cycle time. The maximum allowed axi_clk frequency is 133 MHz, whereas the maximum allowed EIM_BCLK frequency is 66.5 MHz. As a result, if BCD = 0, axi_clk must be ≤ 66.5 MHz. If BCD = 1, then 133 MHz is allowed for axi_clk, resulting in a EIM_BCLK of 66.5 MHz. When the clock branch to EIM is decreased to 66.5 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM) for a detailed clock tree description.

Table 44. EIM Asynchronous Timing Parameters Table Relative Chip Select (continued)

ID	Parameter	Determination by Synchronous Measured Parameters [1]	Min	Max	Unit
WE34	EIM_RW invalid to EIM_CSx invalid	WE7 – WE9 + (WEN – CSN)	—	3 – (WEN_CSN)	ns
WE35	EIM_CSx valid to EIM_OE valid	WE10 – WE6 + (OEA – CSA)	—	3 + (OEA – CSA)	ns
WE36	EIM_OE invalid to EIM_CSx invalid	WE7 – WE11 + (OEN – CSN)	—	3 – (OEN – CSN)	ns
WE37	EIM_CSx valid to EIM_EBx valid (Read access)	WE12 – WE6 + (RBEA – CSA)	—	3 + (RBEA[4] – CSA)	ns
WE38	EIM_EBx invalid to EIM_CSx invalid (Read access)	WE7 – WE13 + (RBEN – CSN)	—	3 – (RBEN[5] – CSN)	ns
WE39	EIM_CSx valid to EIM_LBA valid	WE14 – WE6 + (ADV – CSA)	—	3 + (ADVA – CSA)	ns
WE40	EIM_LBA invalid to EIM_CSx invalid (ADVL is asserted)	WE7 – WE15 – CSN	—	3 – CSN	ns
WE41	EIM_CSx valid to Output Data valid	WE16 – WE6 – WCSA	—	3 – WCSA	ns
WE42	Output Data invalid to EIM_CSx invalid	WE17 – WE7 – CSN	—	3 – CSN	ns
WE43	Input Data valid to EIM_CSx invalid	MAXCO + MAXDI	MAXCO[6] + MAXDI[7]	—	ns
WE44	EIM_CSx invalid to Input Data invalid	0	0	—	ns
WE45	EIM_CSx valid to EIM_EBx valid (Write access)	WE12 – WE6 + (WBEA – CSA)	—	3 + (WBEA – CSA)	ns
WE46	EIM_EBx invalid to EIM_CSx invalid (Write access)	WE7 – WE13 + (WBEN – CSN)	—	–3 + (WBEN – CSN)	ns
WE47	EIM_DTACK valid to EIM_CSx invalid	MAXCO + MAXDTI	MAXCO[6] + MAXDTI[8]	—	ns
WE48	EIM_CSx invalid to EIM_DTACK invalid	0	0	—	ns

1 Parameters WE4–WE21 value, see in the Table 44.

2 EIM_CSx Assertion. This bit field determines when EIM_CSx signal is asserted during read/write cycles.

3 EIM_CSx Negation. This bit field determines when EIM_CSx signal is negated during read/write cycles.

4 EIM_EBx Assertion. This bit field determines when EIM_EBx signal is asserted during read cycles.

5 EIM_EBx Negation. This bit field determines when EIM_EBx signal is negated during read cycles.

6 Output maximum delay from internal driving the FFs to chip outputs. The maximum delay between all memory controls (EIM_ADDR, EIM_CSx, EIM_OE, EIM_RW, EIM_EBx, and EIM_LBA).

7 Maximum delay from chip input data to internal FFs. The maximum delay between all data input pins.

8 DTACK maximum delay from chip input data to internal FF.

4.8 DRAM Timing Parameters

This section includes descriptions of the electrical specifications of DRAM MC module which interfaces external DDR2, LPDDR1, and LPDDR2 memory devices.

Table 47. DDR Output AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR16 CK >= 200 MHz	DQ & DQM output hold time relative to DQS	tDH	0.5 tCK - 1.3	—	ns
DDR15 CK < 200 MHz	DQ & DQM output setup time relative to DQS	tDS	1	—	ns
DDR16 CK < 200 MHz	DQ & DQM output hold time relative to DQS	tDH	1	—	ns

NOTE

The DDR15,16 could be adjusted by the parameter “DLL_WR_DELAY”;

The ideal case is that SDQS is center aligned to the DRAM_D data valid window;

For this table, HW_DRAM_PHY15[14:8] (DLL_WR_DELAY) = 0x10;

4.8.4 DRAM Data Input Timing

DRAM Data input timing is defined for all DDR types: DDR2, LPDDR1, and LPDDR2.

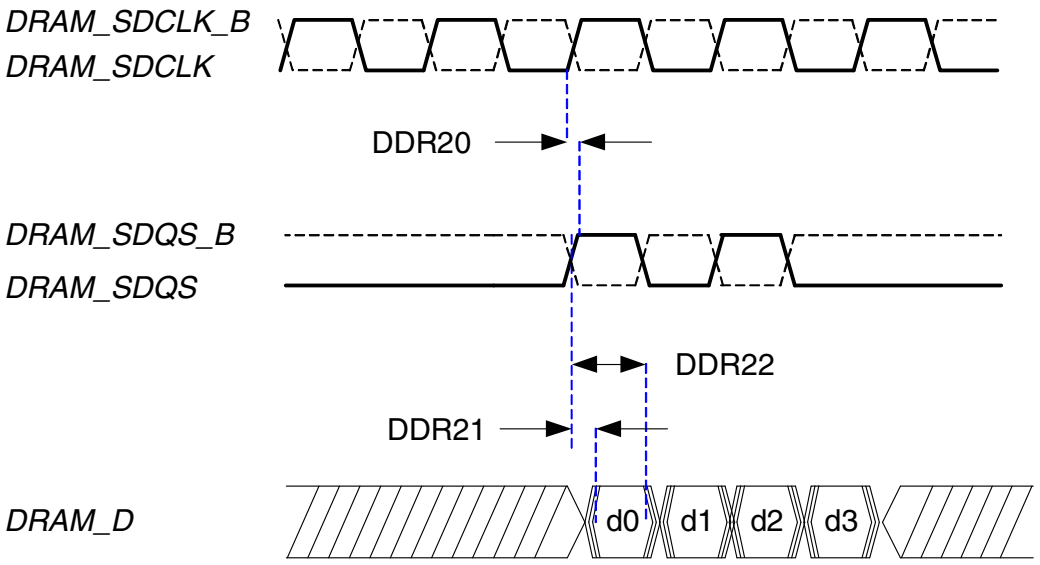

Figure 31. DRAM Data Input Timing

Table 48. DDR2 Input AC Timing

ID	Description	Symbol	Min	Max	Unit
DDR20	Positive DQS latching edge to associated CK edge	tDQSCK	-0.5 tCK	—	ns

Table 55. eMMC4.4 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD2	eSDHC Output Delay	t_{OD}	–5	5	ns
eSDHC Input/Card Outputs CMD, DAT (Reference to CLK)					
SD3	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD4	eSDHC Input Hold Time	t_{IH}	1.5	—	ns

4.9.4 FEC AC Timing Parameters

This section describes the AC timing specifications of the FEC. The i.MX50 FEC supports 10/100 Mbps RMII with MII serial management interface. The RMII and serial management signals are compatible with transceivers operating at a voltage of 3.3 V.

4.9.4.1 RMII Async Inputs Signal Timing (FEC_COL)

Table 56 lists RMII asynchronous inputs signal timing information. Figure 38 shows MII asynchronous input timings listed in Table 56.

Table 56. RMII Async Inputs Signal Timing

Num	Characteristics	Min	Max	Unit
M9	FEC_COL minimum pulse width	1.5	—	FEC_TX_CLK period

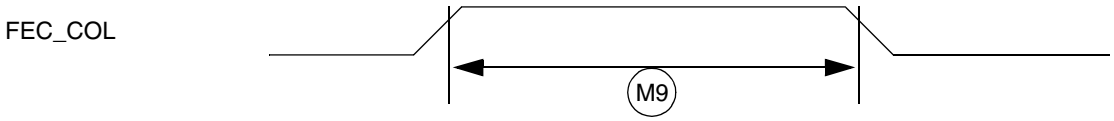

Figure 38. MII Async Inputs Timing Diagram

4.9.4.2 RMII Serial Management Channel Timing (FEC_MDIO and FEC_MDC)

Table 57 lists RMII serial management channel timings. Figure 39 shows RMII serial management channel timings listed in Table 57. The MDC frequency should be equal to or less than 2.5 MHz to be compliant with the IEEE 802.3 RMII specification. However, the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Table 57. RMII Transmit Signal Timing

ID	Characteristics	Min	Max	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns

Table 57. RMII Transmit Signal Timing (continued)

ID	Characteristics	Min	Max	Unit
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

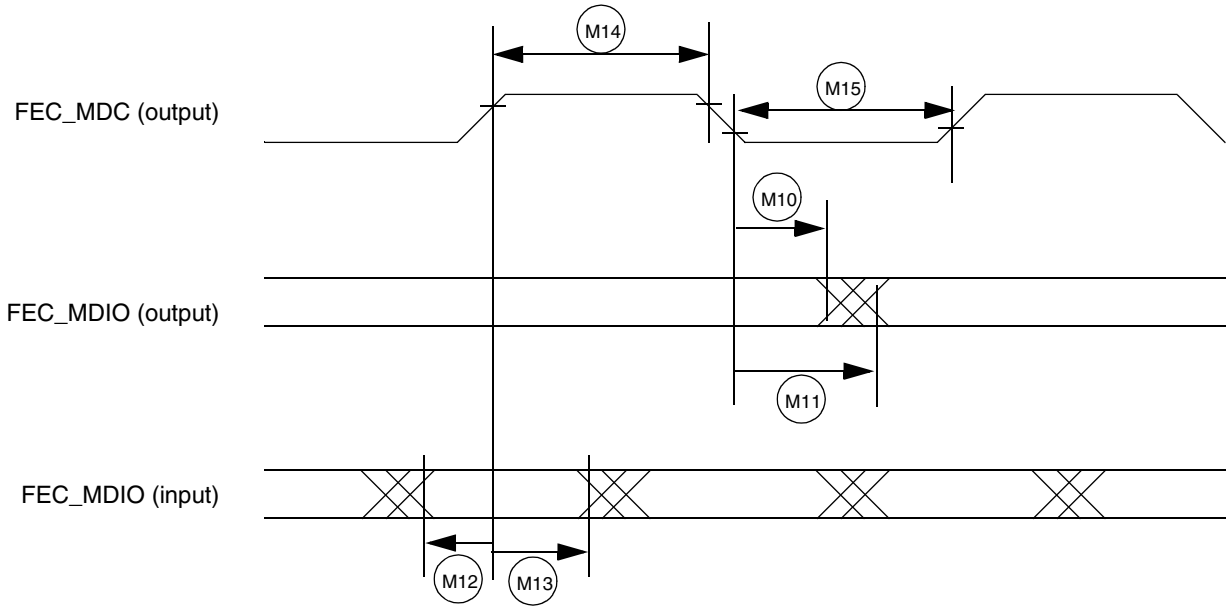

Figure 39. RMII Serial Management Channel Timing Diagram

4.9.4.3 RMII Mode Timing

In RMII mode, FEC_TX_CLK is used as the REF_CLK which is a 50 MHz ± 50 ppm continuous reference clock. FEC_RX_DV is used as the CRS_DV in RMII, and other signals under RMII mode include FEC_TX_EN, FEC_TXD[1:0], FEC_RXD[1:0] and optional FEC_RX_ER.

The RMII mode timings are shown in Table 58 and Figure 40.

Table 58. RMII Signal Timing

No.	Characteristics	Min	Max	Unit
M16	REF_CLK(FEC_TX_CLK) pulse width high	35%	65%	REF_CLK period
M17	REF_CLK(FEC_TX_CLK) pulse width low	35%	65%	REF_CLK period
M18	REF_CLK to FEC_TXD[1:0], FEC_TX_EN invalid	2	—	ns
M19	REF_CLK to FEC_TXD[1:0], FEC_TX_EN valid	—	16	ns
M20	FEC_RXD[1:0], CRS_DV(FEC_RX_DV), FEC_RX_ER to REF_CLK setup	4	—	ns
M21	REF_CLK to FEC_RXD[1:0], FEC_RX_DV, FEC_RX_ER hold	2	—	ns

Table 79. 416 MAPBGA 13x13 mm, 0.5 mm Pitch Ball Map (continued)

AA	Y	W	V	U	T	R
NVCC_SRTC	CKIL	PMIC_ON_REQ	SD2_D2	SD2_CLK	SD2_D0	SD1_CMD
NGND_SRTC	ECKIL	PMIC_STBY_REQ	SD2_D3	SD2_D5	SD2_D1	SD1_D0
NC	NC	NC	NC	NC	NC	NC
JTAG_TDI	JTAG_TMS	JTAG_TCK	SD2_D4	SD2_D6	SD2_CD	SD1_D2
JTAG_TRSTB	VDD_DCDCO	GND_DCDC	SD2_CMD	SD2_D7	SD2_WP	SD1_D3
CKIH	VDD_DCDCI	NC	NC	NC	NC	NC
GND_KEL	USB_OTG_GPANAIO	NC	JTAG_MOD	JTAG_TDO	NVCC_SD1	NVCC_SPI
USB_OTG_RREFEXT	USB_OTG_ID	NC	NVCC_RESET	NVCC_SD2	NVCC_UART	NVCC_SSI
VSS	USB_OTG_VBUS	NC	NVCC_NANDF	NVCC_JTAG	NC	NC
USB_H1_RREFEXT	USB_H1_VBUS	NC	NVCC_NANDF	NVCC_EPDC	NC	NVCC_EPDC
VSS	USB_H1_GPANAIO	NC	CHGR_DET_B	NVCC_LCD	NC	VSS
DISP_D0	DISP_D1	NC	DISP_D11	VSS	NC	VSS
DISP_D2	DISP_D3	NC	DISP_D12	VSS	NC	VSS
DISP_D4	DISP_D5	NC	DISP_D13	VSS	NC	VSS
DISP_D6	DISP_D7	NC	DISP_D14	VSS	NC	VDDAL1
DISP_D8	DISP_D9	NC	DISP_D15	VSS	NC	NC
SD3_D3	DISP_D10	NC	VSS	VSS	VSS	VDDA
SD3_D4	SD3_D5	NC	VSS	VSS	VSS	DRAM_SDODT1
SD3_D6	SD3_D7	NC	NC	NC	NC	NC
DRAM_A4	DRAM_A2	DRAM_A0	VSS	DRAM_SDCKE	DRAM_SDCLK_1	DRAM_SDCLK_1_B
NVCC_EMI_DRAM	DRAM_A3	DRAM_A1	VSS	DRAM_CS1	DRAM_CS0	NVCC_EMI_DRAM
NC	NC	NC	NC	NC	NC	NC
NVCC_EMI_DRAM	DRAM_D1	DRAM_D2	VSS	DRAM_D5	DRAM_D6	NVCC_EMI_DRAM
NVCC_EMI_DRAM	DRAM_D0	DRAM_D3	DRAM_D4	DRAM_D7	DRAM_DQM0	NVCC_EMI_DRAM
AA	Y	W	V	U	T	R

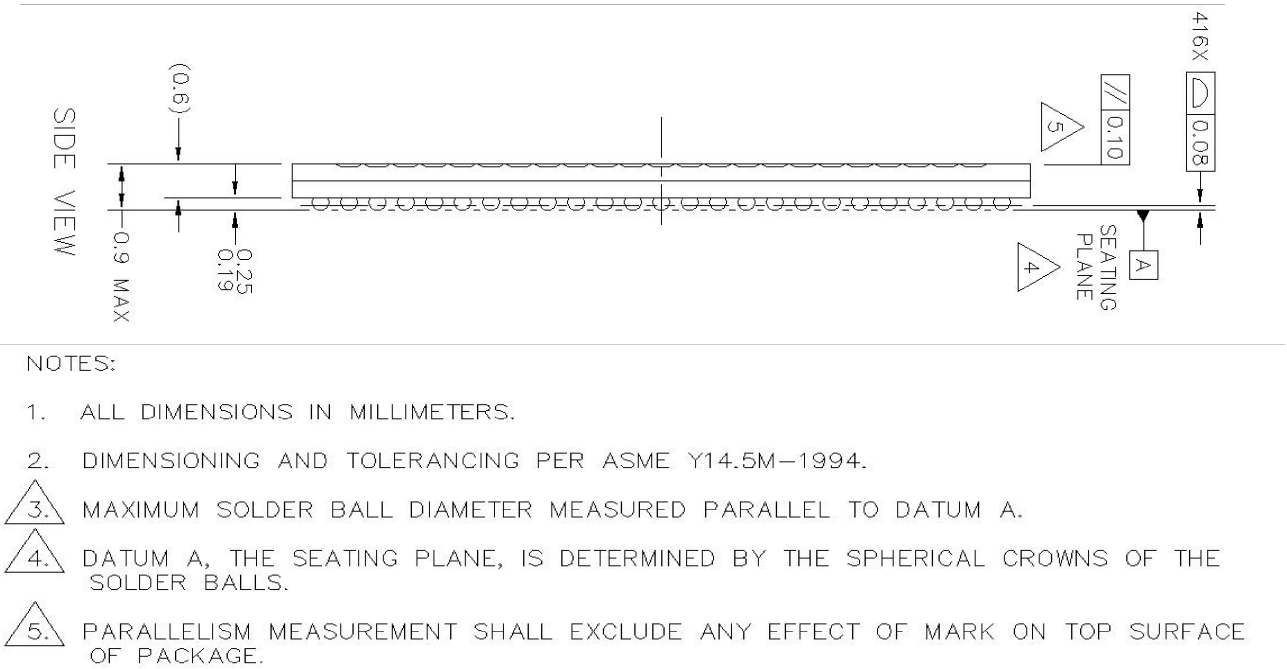

Figure 63. 416 PoPBGA 13 x 13 Package Side View

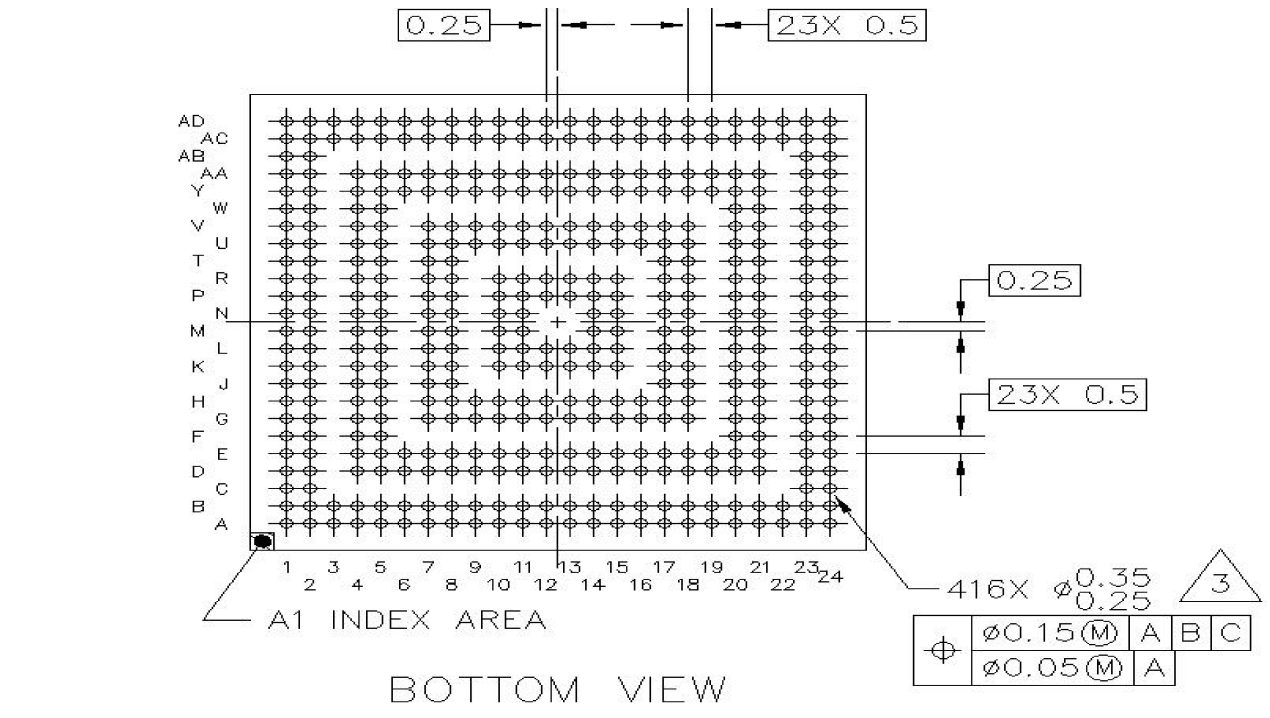

Figure 64. 416 PoPBGA 13 x 13 mm Package Bottom View

The following notes apply to Figure , Figure 63, and Figure 64:

- Unless otherwise specified dimensions are in millimeters.

Table 81. 416 PoPBGA 13 x 13 mm Ball Map (continued)

Y	W	V	U	T	R	P
CKIL	PMIC_ON_REQ	SD3_D0	SD3_D5	SD3_CLK	SD3_D2	SD3_D4
ECKIL	PMIC_STBY_REQ	SD3_D1	SD3_D3	SD3_CMD	SD3_D6	SD1_D0
NC	NC	NC	NC	NC	NC	NC
JTAG_TMS	JTAG_TCK	JTAG_TDO	SD3_D7	SD3_WP	SD1_D3	DRAM_CALIBRATION
VDD_DCDCO	GND_DCDC	JTAG_MOD	DRAM_CS0	DRAM_SDCKE	DRAM_SDCLK_0	DRAM_SDCLK_0_B
VDD_DCDCI	NC	NC	NC	NC	NC	NC
DRAM_A1	NC	DRAM_A0	DRAM_CS1	NVCC_SD1	NVCC_SPI	DRAM_A5
DRAM_A2	NC	NVCC_RESET	NVCC_SD2	NVCC_UART	NVCC_SSI	NVCC_MISC
DRAM_A3	NC	NVCC_NANDF	NVCC_JTAG	NC	NC	NC
DRAM_A4	NC	NVCC_NANDF	NVCC_EPDC	NC	NVCC_EPDC	NVCC_EPDC
DRAM_D17	NC	DRAM_D16	NVCC_LCD	NC	VSS	VSS
DRAM_D19	NC	DRAM_D18	VSS	NC	VSS	VSS
DRAM_D21	NC	DRAM_D20	VSS	NC	VSS	VSS
DRAM_D23	NC	DRAM_D22	VSS	NC	VSS	VSS
DRAM_SDQS2	NC	DRAM_SDQS2_B	VSS	NC	VDDAL1	VDDAL1
DRAM_DQM2	NC	DRAM_D0	VSS	NC	NC	NC
DRAM_D1	NC	DRAM_D2	VSS	VSS	VDDA	VDDA
NVCC_EMI_DRAM	NC	NVCC_EMI_DRAM	DRAM_D5	DRAM_D6	DRAM_D7	DRAM_SDQS0_B
NVCC_EMI_DRAM	NC	NC	NC	NC	NC	NC
NVCC_EMI_DRAM	NVCC_EMI_DRAM	NVCC_EMI_DRAM	DRAM_D3	DRAM_D4	NVCC_EMI_DRAM	NVCC_EMI_DRAM
EPDC_BDR0	EPDC_VCOM1	EPDC_SDOE	EPDC_SDOEZ	EPDC_D9	EPDC_D11	EPDC_D15
NC	NC	NC	NC	NC	NC	NC
EPDC_BDR1	EPDC_D8	EPDC_D10	EPDC_D2	EPDC_D7	EPDC_SDOED	EPDC_GDSP
EPDC_D0	EPDC_D1	EPDC_D3	EPDC_D6	EPDC_D5	EPDC_D4	EPDC_SDCE1

Table 82. 416 PoPBGA 13 x 13 mm Ground, Power, Sense, and Reference Contact Signals (continued)

NVCC_RESET	V8	—
NVCC_SD1	T7	—
NVCC_SD2	U8	—
NVCC_SPI	R7	—
NVCC_SRTC	AA1	—
NVCC_SSI	R8	—
NVCC_UART	T8	—
POP_EMMC_RST	A19	This is PoP eMMC 4.4 NAND Reset input pin. This pin does not connect to the i.MX50. If using eMMC 4.4 NAND, this pin can be connected to a GPIO. For non 4.4 eMMC applications, leave floating.
POP_LPDDR2_1.8V	A20, B19, B20, M5, N5	This is the 1.8V supply for the PoP LPDDR2. These pins do not connect to the i.MX50.
POP_LPDDR2_ZQ0	AA24	This is the PoP LPDDR2 ZQ0 pin. This pin does not connect to the i.MX50. This should be connected on the PCB to a 240 Ω 1% resistor to ground
POP_LPDDR2_ZQ1	AA23	This is the PoP LPDDR2 ZQ1 pin. This pin does not connect to the i.MX50. If used, this should be connected on the PCB to a 240 Ω 1% resistor to ground
POP_NAND_VCC	D19, D20	This is the 3.3V I/O and memory supply for the PoP eMMC NAND. Note that because the eMMC memory and I/O domains are shorted together, it is not possible to support 1.8 V I/O for the PoP eMMC NAND.
USB_VDDA25	AC9, AD9	Note that on the PoPBGA package, USB_OTG_VDDA25 and USB_H1_VDDA25 are shorted together.
USB_VDDA33	AC11, AD11	Note that on the PoPBGA package, USB_OTG_VDDA33 and USB_H1_VDDA33 are shorted together.
VCC	H14, H15, H16, H17, J17, K14, K15, K17, L15	—
VDD_DCDCI	Y6	—
VDD_DCDCO	Y5	—
VDD1P2	AD6	—
VDD1P8	AD7	—

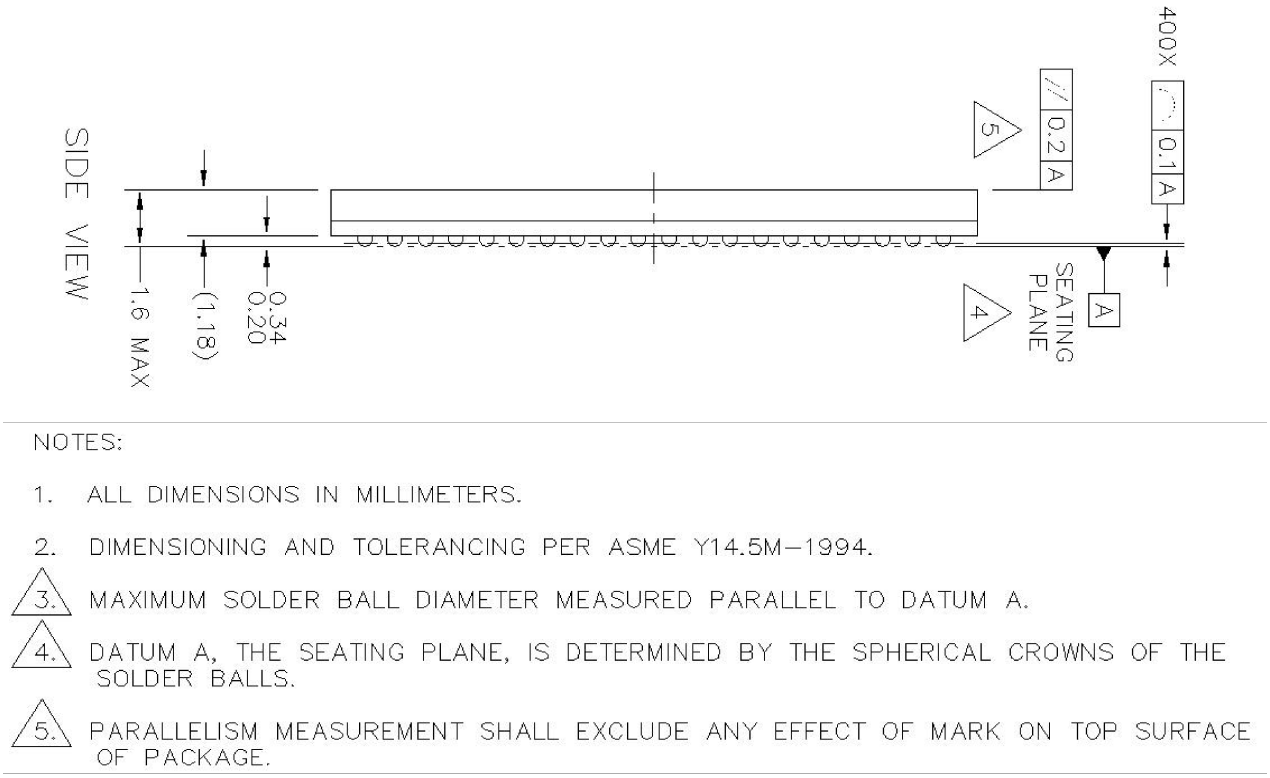

Figure 67. 400 MAPBGA 17x17 mm Package Side View

The following notes apply to Figure 65, Figure 66, and Figure 67:

- Unless otherwise specified dimensions are in millimeters.
- All dimensions and tolerances conform to ASME Y14.5M-1994.
- Parallelism measurement shall exclude any effect of mark on top surface of package.

5.3.2 400 MAPBGA 17 x 17 mm Ball Map

Table 83 shows the 400 MAPBGA 17 x 17 mm ball map.

Table 83. 400 MAPBGA 17 x 17 mm Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	NC	EIM_RDY	EIM_CRE	EIM_EB0	EIM_BCLK	EIM_DA12	EIM_DA8	EPDC_SDSHR	EIM_DA4	EPDC_GDRL	EPDC_GDCLK	EPDC_SDCE1	EPDC_D5	EPDC_D1	EPDC_BDR0	DRAM_D26	DRAM_D28	DRAM_D29	DRAM_D30	NC
B	KEY_COL0	KEY_COL1	EIM_OE	EIM_EB1	EIM_RW	EIM_DA13	EIM_DA9	EIM_DA5	EIM_DA1	EIM_DA0	EIM_CS0	EPDC_SDCE0	EPDC_SDCLK	EPDC_VCOM0	EPDC_D0	EPDC_D2	DRAM_D27	DRAM_D25	DRAM_D24	DRAM_D31

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
DRAM_DQM0	T24	M18	N17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_DQM1	J24	L18	F17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_DQM2	AC24	Y16	U20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_DQM3	B24	G17	D20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_OPEN	J18	—	H18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_OPENFB	H18	—	H17	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_RAS	H21	—	E20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	Keeper
DRAM_SDBA0	K18	—	J20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDBA1	L18	—	H20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDBA2	N18	—	M19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDCKE	U20	T5	R18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDCLK_0	N24	R5	J17	NVCC_EMI_DRAM	DRAMCLK	ALT0	OUT-LO	Keeper
DRAM_SDCLK_0_B	M24	P5	J18	NVCC_EMI_DRAM	DRAMCLK	ALT0	OUT-HI	—
DRAM_SDCLK_1	T20	—	—	NVCC_EMI_DRAM	DRAMCLK	ALT0	OUT-LO	Keeper
DRAM_SDCLK_1_B	R20	—	—	NVCC_EMI_DRAM	DRAMCLK	ALT0	OUT-HI	—
DRAM_SDODT0	G18	—	K18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDODT1	R18	—	—	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_SDQS0	P23	N18	M17	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS0_B	P24	P18	M18	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS1	L23	J20	G17	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS1_B	L24	K18	G18	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS2	AB23	Y15	T19	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS2_B	AB24	V15	T20	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS3	C23	E16	C19	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDQS3_B	C24	G16	C20	NVCC_EMI_DRAM	DRAMCLK	ALT0	IN	—
DRAM_SDWE	P18	—	L18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	Keeper
ECKIL	Y2	Y2	W4	NVCC_SRTC	ANALOG	—	—	—
ECSPI1_MISO	N7	K4	M3	NVCC_SPI	HVIO	ALT1	IN	Keeper
ECSPI1_MOSI	N2	N4	M4	NVCC_SPI	HVIO	ALT1	IN	Keeper

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Document Number: IMX50CEC
Rev. 7
10/2013