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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, LPDDR2, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	EPDC, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Boot Security, Cryptography, Secure JTAG
Package / Case	416-VFBGA
Supplier Device Package	416-VFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx508czk8b

Table 5. Special Signal Considerations (continued)

Signal Name	Remarks
USB_H1_VBUS, USB_OTG_VBUS	These inputs are used by the i.MX50 to detect the presence and level of USB 5 V. If either VBUS input pin is connected to an external USB connector, there is a possibility that a fast 5 V edge rate during a cable attach could trigger the VBUS input ESD protection, which could result in damage to the i.MX50 silicon. To prevent this, the system should use some circuitry to prevent the 5 V edge rate from exceeding 5.25 V / 1 μs. Freescale recommends the use of a low pass filter consisting of 100 Ω resistor in series and a 1 μF capacitor close to the i.MX50 pin. In the case when the USB interface is connected on an on-board USB device (for example, 3G modem), the corresponding USB_VBUS pin may be left floating.
VREF	This pin is the DRAM MC reference voltage input. For LPDDR2 and DDR2, this pin should be connected to ½ of NVCC_EMI_DRAM. For LPDDR1, this pin should be left floating. The user may generate VREF using a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_EMI_DRAM. Shunt each resistor with a closely-mounted 0.1 μF capacitor.
WDOG_B	This output can be used to reset the system PMIC when the i.MX50 processor is locked up. This output is in the NVCC_MISC domain.
WDOG_RST_B_DEB	This output may be used to drive out the internal system reset signal to the system reset controller. This is only intended for debug purposes.
XTAL/EXTAL	These pins are the 24 MHz crystal driver as well as the external 24 MHz clock input. If using these pins to directly drive a 24 MHz crystal: • The user should tie a 24 MHz fundamental-mode crystal across XTAL and EXTAL. • The crystal must be rated for a maximum drive level of 100 μW or higher. • The recommended crystal ESR (equivalent series resistance) is 80 Ω or less. If using these pins as a clock input from an external 24 MHz oscillator: • The crystal may be eliminated and EXTAL driven directly driven by the external oscillator. The clock signal level on EXTAL must swing from NVCC_SRTC to GND. • In this configuration, the XTAL pin must be floated and the COSC_EN bit (bit 12 in the CCR register in the Clock Control Module) must be cleared to put the on-chip oscillator circuit in bypass mode which allows EXTAL to be externally driven. • Note there are strict jitter requirements if using an external oscillator in a USB application: < 50 ps peak-to-peak below 1.2 MHz and < 100 ps peak-to-peak above 1.2 MHz for the USB PHY.

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics of the i.MX50 processor.

NOTE

These electrical specifications are preliminary. These specifications are not fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications are published after thorough characterization and device qualifications have been completed.

Table 14 shows the maximum supply current consumption of the i.MX50 for PMIC specification purposes.

Table 14. Maximum Supply Current Consumption—ARM CLK = 800 MHz

Condition	Supply	Voltage (V)	Current (mA)	Power (mW)
• T_a = 70°C • ARM core in Run mode • ARM CLK = 800 MHz • SYS CLK = 266 MHz • AHB CLK = 133 MHz • DDR CLK = 266 MHz • All voltages operating at maximum levels • External (MHz) crystal and on-chip oscillator enabled • All modules enabled	VDDGP	1.15	628	723
	VCC	1.275	185	236
	VDDA/VDDAL1	1.275	40	51
	VDD1P2	1.3	5.92	7.70
	VDD1P8	1.95	1.53	2.99
	VDD2P5[1]	2.75	1.13	3.11
	VDD3P0	3.3	1.61	5.32
	NVCC_EMI_DRAM	1.95	8.3	16.17
	VDD_DCDCI	1.95	0.021	0.041
	USB_OTG_VDDA33 + USB_H1_VDDA33	3.6	10.8	38.8
	VDDO25 + USB_OTG_VDDA25 + USB_H1_VDDA25	2.75	12.45	34.239
	NVCC_RESET	3.1	0.226	0.701
	NVCC_SRTC	1.3	0.0035	0.0045
	Total	—	—	1120

[1] During eFuse programming, the maximum current on VDD2P5 will exceed these values. See Table 13 on page 26 for the maximum VDD2P5 current during eFuse programming.

- All other supply voltages at nominal levels
- External (MHz) crystal and on-chip oscillator disabled
- CKIL input ON with 32 kHz signal present
- All PLLs OFF, all CCM-generated clocks OFF
- All modules disabled
- No external resistive loads that cause current

4.1.6 USB-OH-1 (OTG + 1 Host Port) Current Consumption

Table 17 shows the USB interface current consumption.

Table 17. USB Interface Current Consumption

Parameter	Conditions		Typical @ 25 °C	Max	Unit
Analog supply 3.3 V USB_H1_VDDA33 USB_OTG_VDDA33	Full speed	RX	5.5	6	mA
		TX	7	8	
	High speed	RX	5	6	
		TX	5	6	
Analog supply 2.5 V USB_H1_VDDA25 USB_OTG_VDDA25	Full speed	RX	6.5	7	mA
		TX	6.5	7	
	High speed	RX	12	13	
		TX	21	22	
Digital supply VCC (1.2 V)	Full speed	RX	6	7	mA
		TX	6	7	
	High speed	RX	6	7	
		TX	6	7	

4.2 Supply Power-Up/Power-Down Requirements and Restrictions

The system design must comply with the power-up and power-down sequence guidelines as described in this section to guarantee reliable operation of the device. Any deviation from these sequences can result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the i.MX50 processor (worst-case scenario)

4.5.7 DDR2 I/O AC Parameters

Table 33 shows the AC parameters for DDR2 I/O.

Table 33. DDR2 I/O AC Parameters

Parameter	Symbol	Min	Max	Unit
AC input logic high	Vih(ac)	Vref+0.25	-	V
AC input logic low	Vil(ac)	-	Vref-0.25	
AC differential input voltage[1]	Vid(ac)	0.5	ovdd	
AC Input differential cross point voltage[2]	Vix(ac)	0.5*ovdd -0.175	0.5*ovdd + 0.175	
AC output differential cross point voltage [3]	Vox(ac)	0.5*ovdd -0.125	0.5*ovdd+ 0.125	
Output propagation delay high to low	t_{POHLD}		3.5	ns
Output propagation delay low to high	t_{POLHD}		3.5	
Input propagation delay high to low	t_{PIHLD}		1.5	
Input propagation delay low to high	t_{PILHD}		1.5	
Single output slew rate	tsr	0.4	2	V/ns

[1]Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac)-Vil(ac)

[2]The typical value of Vix(ac) is expected to be about 0.5*OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

[3]The typical value of Vox(ac) is expected to be about 0.5*OVDD and Vox(ac) is expected to track variation in OVDD. Vox(ac) indicates the voltage at which differential output signal must cross.

Table 35. LPDDR2 I/O AC Parameters (continued)

Parameter	Symbol	Min	Max	Unit
Single output slew rate (Driver impedance =40Ω+/-30%)	tsr	1.5	3.5	V/ns
Single output slew rate (Driver impedance =60Ω+/-30%	tsr	1	2.5	V/ns

[1]Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the "true" input signal and Vcp is the "complementary" input signal. The Minimum value is equal to Vih(ac)-Vil(ac).
[2]The typical value of Vix(ac) is expected to be about 0.5*OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.6 System Modules Timing

This section contains the timing and electrical parameters for the modules in the i.MX50 processor.

4.6.1 Reset Timings Parameters

Figure 6 shows the reset timing and Table 36 lists the timing parameters.

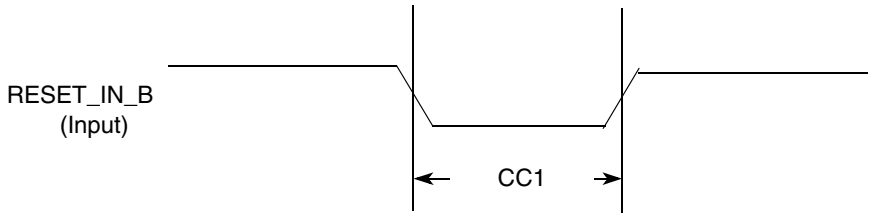

Figure 6. Reset Timing Diagram

Table 36. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of RESET_IN_B assertion to be qualified as valid (input slope = 5 ns)	50	—	ns

4.6.2 WDOG Reset Timing Parameters

Figure 7 shows the WDOG reset timing and Table 37 lists the timing parameters.

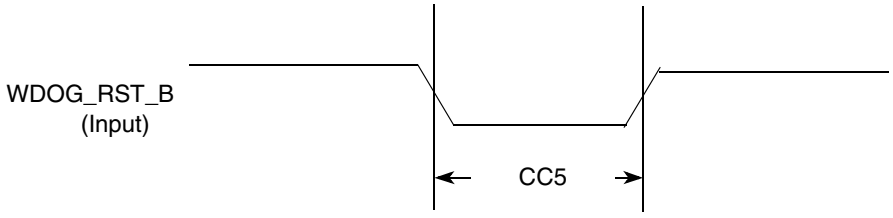

Figure 7. WDOG_RST_B Timing Diagram

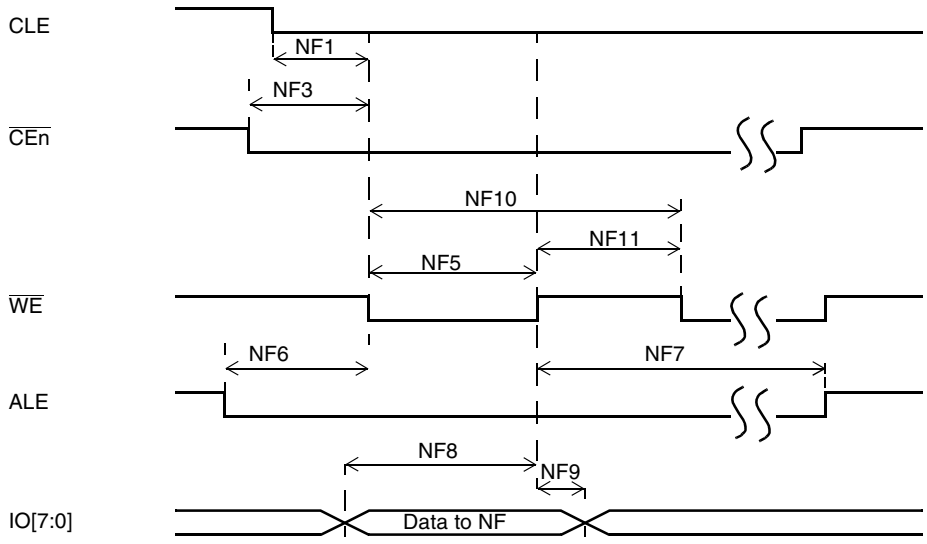

Figure 10. Write Data Latch Cycle Timing Diagram

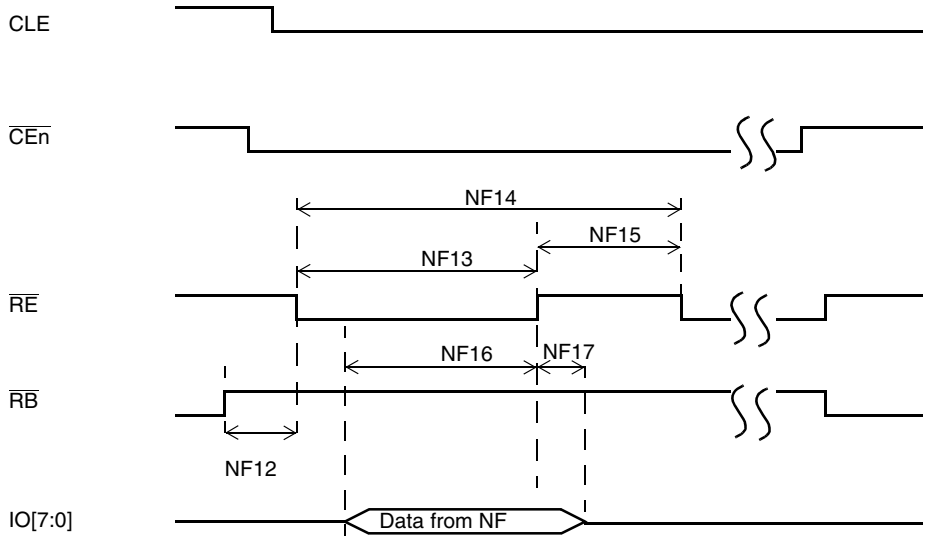

Figure 11. Read Data Latch Cycle Timing Diagram

Table 40. Asynchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T[2] = GPMI Clock Cycle[3]		Example Timing for GPMI Clock ≈ 100MHz T = 10ns		Unit
			Min.	Max.	Min.	Max.	
NF1	CLE setup time	tCLS	(AS+1)*T	—	10	—	ns
NF2	CLE hold time	tCLH	(DH+1)*T	—	20	—	ns
NF3	$\overline{\text{CEn}}$ setup time	tCS	(AS+1)*T	—	10	—	ns
NF4	$\overline{\text{CE}}$ hold time	tCH	(DH+1)*T	—	20	—	ns

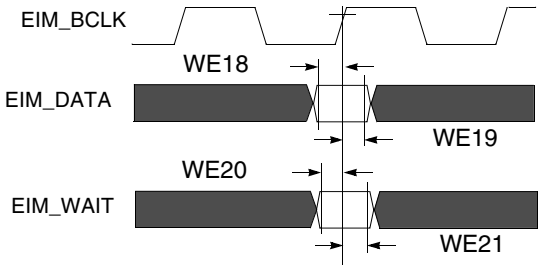

Figure 18. EIM Inputs Timing Diagram

Table 43. EIM Bus Timing Parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	EIM_BCLK Cycle time[2]	t	—	2t	—	3t	—	4t	—
WE2	EIM_BCLK Low Level Width	0.4t	—	0.8t	—	1.2t	—	1.6t	—
WE3	EIM_BCLK High Level Width	0.4t	—	0.8t	—	1.2t	—	1.6t	—
WE4	Clock rise to address valid[3]	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE5	Clock rise to address invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE6	Clock rise to EIM_CSx valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE7	Clock rise to EIM_CSx invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE8	Clock rise to EIM_RW valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE9	Clock rise to EIM_RW invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE10	Clock rise to EIM_OE valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE11	Clock rise to EIM_OE invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE12	Clock rise to EIM_EBx valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE13	Clock rise to EIM_EBx invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE14	Clock rise to EIM_LBA valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE15	Clock rise to EIM_LBA invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	3t – 1.25	3t + 1.75
WE16	Clock rise to Output Data valid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	2t – 1.25	2t + 1.75
WE17	Clock rise to Output Data Invalid	0.5t – 1.25	0.5t + 1.75	t – 1.25	t + 1.75	2t – 1.25	2t + 1.75	2t – 1.25	2t + 1.75
WE18	Input Data setup time to Clock rise	2	—	2	—	2	—	2	—
WE19	Input Data hold time from Clock rise	2.5	—	2.5	—	2.5	—	2.5	—
WE20	EIM_WAIT setup time to Clock rise	2	—	2	—	2	—	2	—
WE21	EIM_WAIT hold time from Clock rise	2.5	—	2.5	—	2.5	—	2.5	—

1 *t* is axi_clk cycle time. The maximum allowed axi_clk frequency is 133 MHz, whereas the maximum allowed EIM_BCLK frequency is 66.5 MHz. As a result, if BCD = 0, axi_clk must be ≤ 66.5 MHz. If BCD = 1, then 133 MHz is allowed for axi_clk, resulting in a EIM_BCLK of 66.5 MHz. When the clock branch to EIM is decreased to 66.5 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM) for a detailed clock tree description.

[2] EIM_BCLK parameters are being measured from the 50% point that is, high is defined as 50% of signal value and low is defined as 50% as signal value.

[3] For signal measurements *High* is defined as 80% of signal value and *Low* is defined as 20% of signal value.

4.7.2 Examples of EIM Accesses

Figure 19, Figure 20, Figure 21, Figure 22, Figure 23, and Figure 24 give a few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

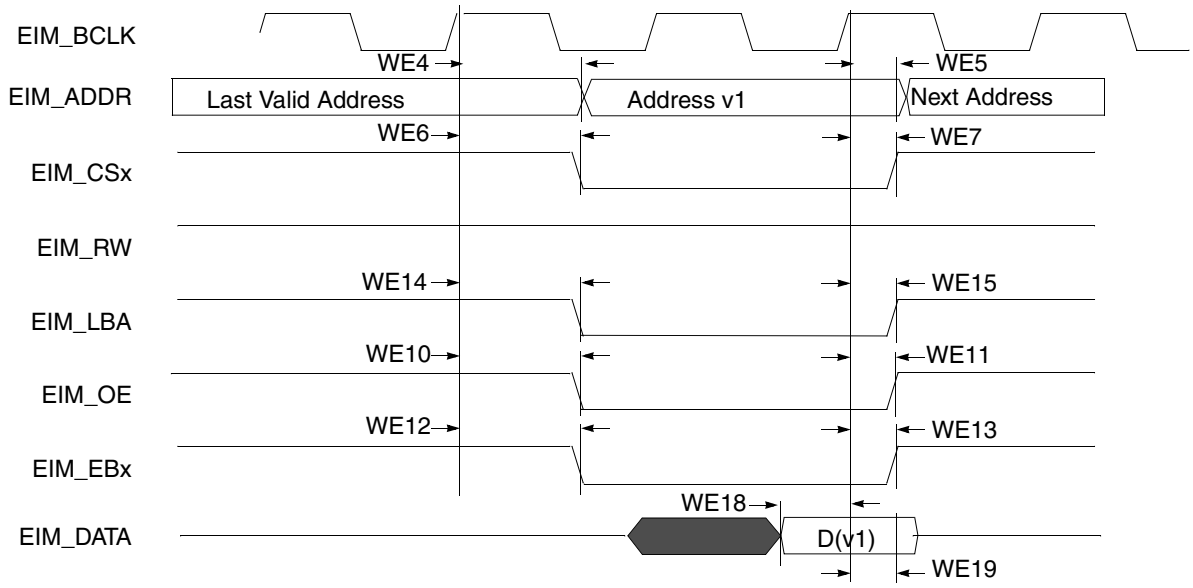

Figure 19. Synchronous Memory Read Access, WSC=1

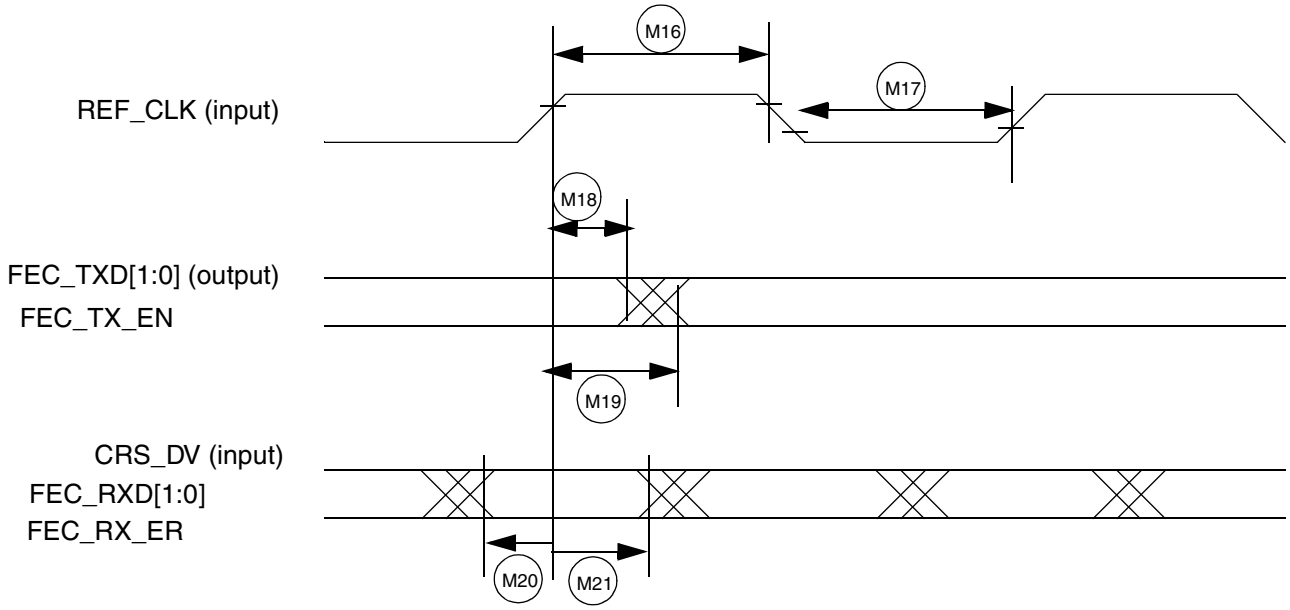

Figure 40. RMII Mode Signal Timing Diagram

4.9.5 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 41 depicts the timing of I²C module, and Table 59 lists the I²C module timing characteristics.

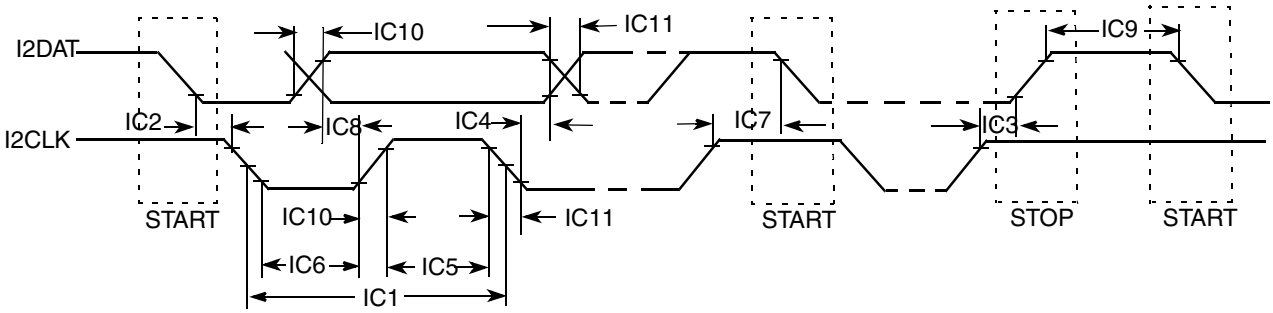

Figure 41. I²C Bus Timing

Table 59. I²C Module Timing Parameters

ID	Parameter	Standard Mode Supply Voltage = 1.65 V–1.95 V, 2.7 V–3.3 V		Fast Mode Supply Voltage = 2.7 V–3.3 V		Unit
		Min	Max	Min	Max	
IC1	I2CLK cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs

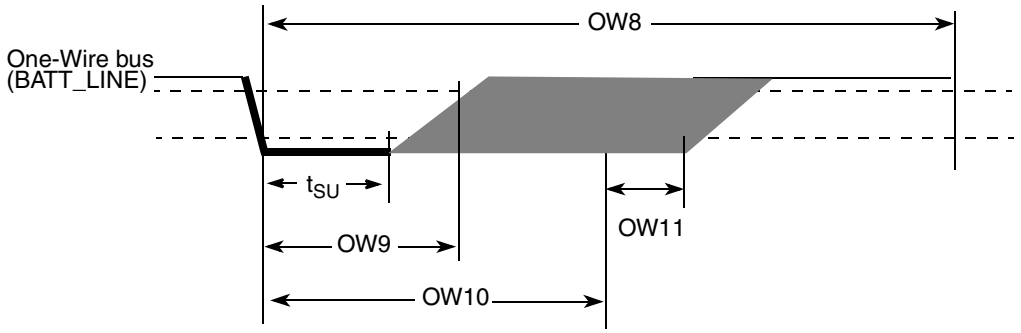

Figure 45. Read Sequence Timing Diagram

Table 62. WR1 /RD Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Unit
OW7	Write 1 Low Time	t_{LOW1}	1	5	15	µs
OW8	Transmission Time Slot	t_{SLOT}	60	117	120	µs
—	Read Data Setup	t_{SU}	—	—	1	µs
OW9	Read Low Time	t_{LOWR}	1	5	15	µs
OW10	Read Data Valid	t_{RDV}	—	15	—	µs
OW11	Release Time	$t_{RELEASE}$	0	—	45	µs

4.9.7 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 46 depicts the timing of the PWM, and Table 63 lists the PWM timing parameters.

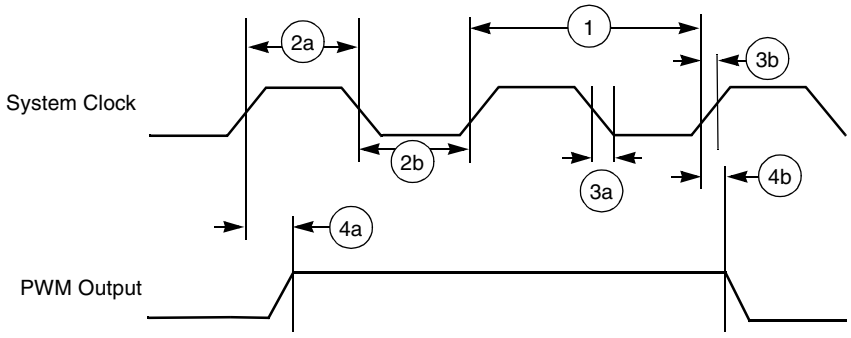

Figure 46. PWM Timing

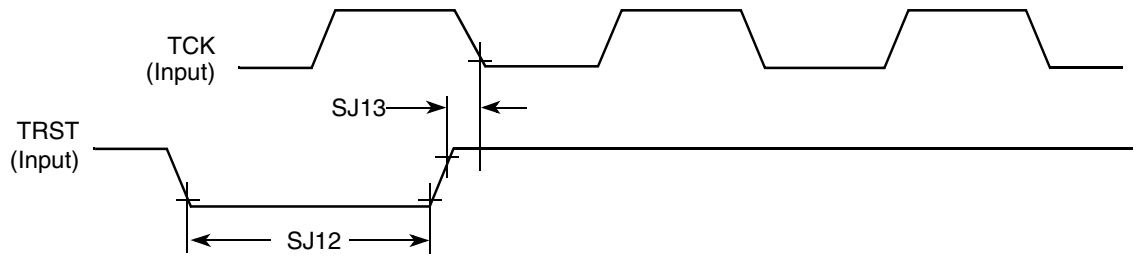

Figure 50. $\overline{\text{TRST}}$ Timing Diagram

Table 64. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	TCK frequency of operation $1/(3 \bullet T_{DC})$[1]	0.001	22	MHz
SJ1	TCK cycle time in crystal mode	45	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	TCK low to output data valid	—	40	ns
SJ7	TCK low to output high impedance	—	40	ns
SJ8	TMS, TDI data set-up time	5	—	ns
SJ9	TMS, TDI data hold time	25	—	ns
SJ10	TCK low to TDO data valid	—	44	ns
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

1 T_{DC} = target frequency of SJC

2 V_M = mid-point voltage

Table 79. 416 MAPBGA 13x13 mm, 0.5 mm Pitch Ball Map (continued)

P	N	M	L	K	J	H
SD1_CLK	ECSPI1_SCLK	CSPI_SCLK	UART2_RXD	UART2_TXD	UART1_RXD	UART1_TXD
SD1_D1	ECSPI1_MOSI	CSPI_MOSI	UART2_RTS	UART2_CTS	UART1_RTS	UART1_CTS
NC	NC	NC	NC	NC	NC	NC
ECSPI2_SCLK	ECSPI2_SS0	CSPI_SS0	UART3_RXD	UART3_TXD	SSI_TXC	SSI_TXFS
ECSPI2_MOSI	ECSPI2_MISO	CSPI_MISO	UART4_RXD	UART4_TXD	SSI_RXD	SSI_TXD
NC	NC	NC	NC	NC	NC	NC
ECSPI1_SS0	ECSPI1_MISO	NVCC_EIM	NVCC_EIM	VDDGP	SSI_RXC	SSI_RXFS
NVCC_MISC	NVCC_KEYPAD	NVCC_EIM	VDDGP	VDDGP	VDDGP	VDDGP
NC	NC	NC	NC	NC	NC	VDDGP
NVCC_EPDC	NVCC_EPDC	NVCC_EPDC	VDDGP	VDDGP	NC	VDDGP
VSS	VSS	VSS	VDDGP	VDDGP	NC	VDDGP
VSS	NC	NC	VSS	VSS	NC	VSS
VSS	NC	NC	VSS	VSS	NC	VSS
VSS	VSS	VSS	VSS	VCC	NC	VCC
VDDAL1	VSS	VSS	VCC	VCC	NC	VCC
NC	NC	NC	NC	NC	NC	VCC
VDDA	VSS	VSS	VSS	VCC	VCC	VCC
DRAM_SDWE	DRAM_SDBA2	VSS	DRAM_SDBA1	DRAM_SDBA0	DRAM_OPEN	DRAM_OPENFB
NC	NC	NC	NC	NC	NC	NC
DRAM_A5	DRAM_A7	VSS	DRAM_CALIBRATION	DRAM_A10	DRAM_A11	DRAM_A12
DRAM_A6	DRAM_A8	VSS	DRAM_A9	NVCC_EMI_DRAM	DRAM_CAS	DRAM_RAS
NC	NC	NC	NC	NC	NC	NC
DRAM_SDQS0	VDDO25	VREF	DRAM_SDQS1	NVCC_EMI_DRAM	DRAM_D8	DRAM_D11
DRAM_SDQS0_B	DRAM_SDCLK_0	DRAM_SDCLK_0_B	DRAM_SDQS1_B	NVCC_EMI_DRAM	DRAM_DQM1	DRAM_D9
P	N	M	L	K	J	H

Table 79. 416 MAPBGA 13x13 mm, 0.5 mm Pitch Ball Map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
AB	BOOT_MODE0	BOOT_MODE1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	DRAM_SDQS2	DRAM_SDQS2_B	AB
AC	RESET_IN_B	TEST_MODE	GND3P0	GND2P5	EXTAL	GND1P2	GND1P8	USB_OTG_DN	USB_OTG_VDDA25_1	USB_H1_DN	USB_H1_VDDA33	DISP_BUSY	DISP_RS	DISP_RESET	SD3_D0	SD3_D1	SD3_D2	VSS	DRAM_D16	DRAM_D18	NVCC_EMI_DRAM	DRAM_D20	DRAM_D22	DRAM_DQM2	AC
AD	VSS	POR_B	VDD3P0	VDD2P5	XTAL	VDD1P2	VDD1P8	USB_OTG_DP	USB_H1_VDDA25_1	USB_H1_DP	USB_OTG_VDDA33	DISP_WR	DISP_RD	DISP_CS	SD3_WP	SD3_CLK	SD3_CMD	VSS	DRAM_D17	DRAM_D19	NVCC_EMI_DRAM	DRAM_D21	DRAM_D23	VSS	AD

5.1.3 416 MAPBGA 13 x 13 Power Rails

Table 80. 416 MAPBGA 13x13 Ground, Power, Sense, and Reference Contact Signals

Pin Name	Ball Number	Comments
GND_DCDC	W5	—
NVCC_EIM	L7, M7, M8	—
NVCC_EMI_DRAM	A21, AA21, AA23, AA24, AC21, AD21, B21, D21, D23, D24, K21, K23, K24, R21, R23, R24	—
NVCC_EPDC	M10, N10, P10, R10, U10	—
NVCC_JTAG	U9	—
NVCC_KEYPAD	N8	—
NVCC_LCD	U11	—
NVCC_MISC	P8	—
NVCC_NANDF	V9, V10	—
NVCC_RESET	V8	—
NVCC_SD1	T7	—
NVCC_SD2	U8	—
NVCC_SPI	R7	—

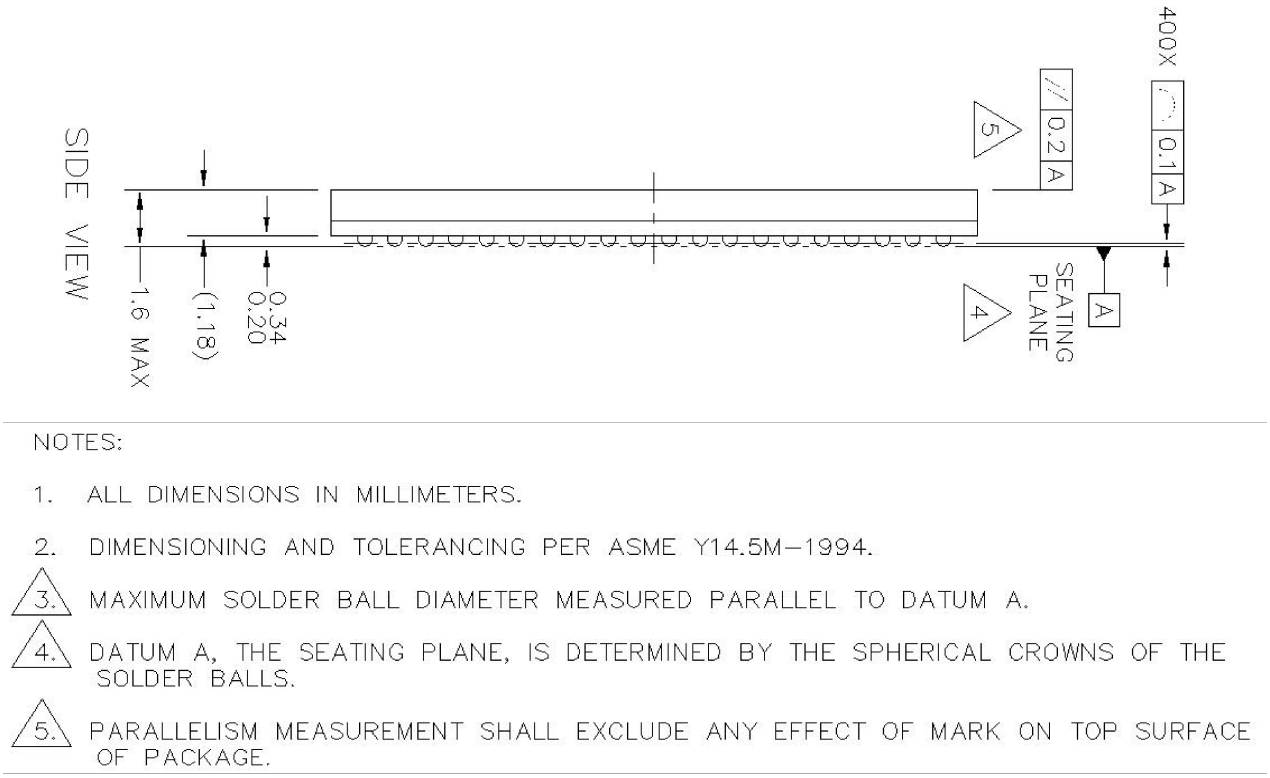

Figure 67. 400 MAPBGA 17x17 mm Package Side View

The following notes apply to Figure 65, Figure 66, and Figure 67:

- Unless otherwise specified dimensions are in millimeters.
- All dimensions and tolerances conform to ASME Y14.5M-1994.
- Parallelism measurement shall exclude any effect of mark on top surface of package.

5.3.2 400 MAPBGA 17 x 17 mm Ball Map

Table 83 shows the 400 MAPBGA 17 x 17 mm ball map.

Table 83. 400 MAPBGA 17 x 17 mm Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	NC	EIM_RDY	EIM_CRE	EIM_EB0	EIM_BCLK	EIM_DA12	EIM_DA8	EPDC_SDSHR	EIM_DA4	EPDC_GDRL	EPDC_GDCLK	EPDC_SDCE1	EPDC_D5	EPDC_D1	EPDC_BDR0	DRAM_D26	DRAM_D28	DRAM_D29	DRAM_D30	NC
B	KEY_COL0	KEY_COL1	EIM_OE	EIM_EB1	EIM_RW	EIM_DA13	EIM_DA9	EIM_DA5	EIM_DA1	EIM_DA0	EIM_CS0	EPDC_SDCE0	EPDC_SDCLK	EPDC_VCOM0	EPDC_D0	EPDC_D2	DRAM_D27	DRAM_D25	DRAM_D24	DRAM_D31

Table 83. 400 MAPBGA 17 x 17 mm Ball Map (continued)

J	H	G	F	E	D	C
UART1_CTS	UART1_TXD	I2C3_SCL	I2C2_SCL	I2C1_SCL	KEY_ROW0	KEY_COL2
UART3_TXD	UART4_TXD	I2C3_SDA	I2C2_SDA	I2C1_SDA	KEY_ROW1	KEY_COL3
UART4_RXD	SSI_TXFS	SSI_TXC	SSI_RXD	PWM2	KEY_ROW3	KEY_ROW2
CSPI_SS0	SSI_RXC	SSI_TXD	WDOG	PWM1	EIM_LBA	EIM_WAIT
NVCC_MISC	NVCC_KEYPAD	SSI_RXFS	EPITO	OWIRE	EIM_DA15	EIM_DA14
VDDGP	VDDGP	VDDGP	NVCC_EIM	EPDC_SDCE5	EIM_DA11	EIM_DA10
VDDGP	VDDGP	VDDGP	NVCC_EIM	EPDC_PWRCOM	EIM_DA7	EIM_DA6
VSS	VDDGP	VDDGP	NVCC_EIM	EPDC_SDCE3	EIM_DA3	EIM_DA2
VDDAL1	VDDGP	VDDGP	NVCC_EPDC	EPDC_PWRCTRL1	EIM_CS2	EIM_CS1
VDDAL1	VDDGP	VDDGP	NVCC_EPDC	EPDC_PWRCTRL0	EPDC_SDCE4	EPDC_GDOE
VDDA	VSS	VSS	NVCC_EPDC	EPDC_D14	EPDC_GDSP	EPDC_SDCE2
VCC	VSS	VSS	NVCC_EPDC	EPDC_PWRCTRL2	EPDC_SDCLKN	EPDC_PWRSTAT
VSS	VSS	VSS	EPDC_D12	EPDC_D15	EPDC_D10	EPDC_SDOE
VSS	VSS	VSS	EPDC_D11	EPDC_D13	EPDC_D7	EPDC_D6
NVCC_EMI_DRAM	VSS	EPDC_VCOM1	EPDC_PWRCTRL3	EPDC_D8	EPDC_D4	EPDC_SDLE
NVCC_EMI_DRAM	NVCC_EMI_DRAM	EPDC_SDOED	EPDC_SDOEZ	EPDC_D9	EPDC_BDR1	EPDC_D3
DRAM_SDCLK_0	DRAM_OPENFB	DRAM_SDQS1	DRAM_DQM1	DRAM_D10	DRAM_D8	DRAM_D15
DRAM_SDCLK_0_B	DRAM_OPEN	DRAM_SDQS1_B	DRAM_D9	DRAM_D13	DRAM_D12	DRAM_D14
DRAM_A10	DRAM_A11	DRAM_A9	DRAM_A13	DRAM_A12	DRAM_D11	DRAM_SDQS3
DRAM_SDBA0	DRAM_SDBA1	DRAM_CAS	DRAM_CALIBRATION	DRAM_RAS	DRAM_DQM3	DRAM_SDQS3_B

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
DISP_D6	AA15	AD16	U12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D7	Y15	AC19	V13	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_D8	AA16	AD17	W15	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_D9	Y16	AC20	V15	NVCC_NANDF	HVIO	ALT1	IN	Keeper
DISP_RD	AD13	AA20	V12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_RESET	AC14	AA19	T14	NVCC_LCD	HVIO	ALT1	IN	Keeper
DISP_RS	AC13	AD23	Y12	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DISP_WR	AD12	AD20	V10	NVCC_LCD	HVIO	ALT3	OUT-LO	100K PU
DRAM_A0	W20	V7	T17	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A1	W21	Y7	T18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A10	K20	—	J19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A11	J20	—	H19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A12	H20	—	E19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A13	F21	—	F19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A14	F20	—	—	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A2	Y20	Y8	U18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A3	Y21	Y9	V18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A4	AA20	Y10	R17	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A5	P20	P7	K19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A6	P21	L5	L19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A7	N20	K5	K20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A8	N21	J5	L20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_A9	L21	H5	G19	NVCC_EMI_DRAM	DRAM	ALT0	OUT-LO	Keeper
DRAM_CALIBRATION	L20	P4	F20	NVCC_EMI_DRAM	DRAMCALIB	—	—	—
DRAM_CAS	J21	—	G20	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	Keeper
DRAM_CS0	T21	U5	P17	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	Keeper
DRAM_CS1	U21	U7	P18	NVCC_EMI_DRAM	DRAM	ALT0	OUT-HI	Keeper
DRAM_D0	Y24	V16	R20	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper
DRAM_D1	Y23	Y17	R19	NVCC_EMI_DRAM	DRAM	ALT0	IN	Keeper

Table 85. Alphabetical List of Signal Assignments (continued)

Pin Name	416 MAPBGA Ball Number	416 PoPBGA Ball Number	400 MAPBGA Ball Number	Pin Power Domain	Pad Type	IOMUX MUX CTL After Reset	Direction After Reset	IOMUX PAD CTL After Reset
SD2_D2	V1	F1	W2	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D3	V2	F2	T4	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D4	V4	G2	V2	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D5	U2	E2	U2	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D6	U4	H4	R4	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_D7	U5	F4	W1	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD2_WP	T5	G4	T2	NVCC_SD2	HVIO	ALT1	IN	Keeper
SD3_CLK	AD16	T1	Y14	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_CMD	AD17	T2	U16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D0	AC15	V1	Y17	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D1	AC16	V2	V16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D2	AC17	R1	T16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D3	AA17	U2	U15	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D4	AA18	P1	W17	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D5	Y18	U1	U17	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D6	AA19	R2	V17	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_D7	Y19	U4	T15	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SD3_WP	AD15	T4	W16	NVCC_NANDF	HVIO	ALT1	IN	Keeper
SSI_RXC	J7	AD12	H4	NVCC_SSI	HVIO	ALT1	IN	Keeper
SSI_RXD	J5	AC14	F3	NVCC_SSI	HVIO	ALT1	IN	Keeper
SSI_RXFS	H7	AD13	G5	NVCC_SSI	HVIO	ALT1	IN	Keeper
SSI_TXC	J4	AC13	G3	NVCC_SSI	HVIO	ALT1	IN	Keeper
SSI_TXD	H5	AD14	G4	NVCC_SSI	HVIO	ALT1	IN	Keeper
SSI_TXFS	H4	AC12	H3	NVCC_SSI	HVIO	ALT1	IN	Keeper
TEST_MODE	AC2	AC2	U4	NVCC_RESET	LVIO	ALT0	IN	100K PD
UART1_CTS	H2	B4	J1	NVCC_UART	HVIO	ALT1	IN	Keeper
UART1_RTS	J2	B3	K2	NVCC_UART	HVIO	ALT1	IN	Keeper
UART1_RXD	J1	A2	K1	NVCC_UART	HVIO	ALT1	IN	Keeper
UART1_TXD	H1	A3	H1	NVCC_UART	HVIO	ALT1	IN	Keeper
UART2_CTS	K2	B2		NVCC_UART	HVIO	ALT1	IN	Keeper

Table 86. i.MX50 Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 1	10/2011	• Table 5, "Special Signal Considerations," on page 17 changed CHRG_DET_B to CHGR_DET_B. • Table 5, "Special Signal Considerations," on page 17 in the CHGR_DET_B signal remarks, added “The maximum current leakage at this pin is 8.5 μA.” • Table 5, "Special Signal Considerations," on page 17 in the JTAG_MOD remarks, changed “pull-down” to “pull-up, by default” and added “If JTAG port is not needed, the internal pull-up can be disabled in order to reduce supply current to the pin.” • Table 14, "Maximum Supply Current Consumption—ARM CLK = 800 MHz," on page 27 in the 11th row under the Supply column, changed VDDO2P5 to VDDO25. • Table 78, "VBUS Comparators Thresholds," on page 101 changed CHRG_DET_B to CHGR_DET_B. • Table 5, "Special Signal Considerations," on page 17 for 416 MAPBGA, DRAM_SDCLK_0 pin number was changed to N24 and DRAM_SDCLK_0_B pin number was changed to M24. • Table 5, "Special Signal Considerations," on page 17 for 416 MAPBGA, DRAM_SDCLK_1 pin number was changed to T20 and DRAM_SDCLK_1_B pin number was changed to R20. • Table 5, "Special Signal Considerations," on page 17 for 416 MAPBGA, DRAM_SDQS0 pin number was changed to P23 and DRAM_SDQS0_B pin number was changed to P24. • Table 5, "Special Signal Considerations," on page 17 changed pad type of pin DRAM_CALIBRATION to DRAMCALIB. • Table 5, "Special Signal Considerations," on page 17 changed pad type of pins DRAM_SDCLK_0, DRAM_SDCLK_0_B, DRAM_SDCLK_1, DRAM_SDCLK_1_B, DRAM_SDQS0, DRAM_SDQS0_B, DRAM_SDQS1, DRAM_SDQS1_B, DRAM_SDQS2, DRAM_SDQS2_B, DRAM_SDQS3, and DRAM_SDQS3_B to DRAMCLK.
Rev. 0	07/2011	Initial release.

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