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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	SPI, 3-Wire Serial
Clock Rate	20MHz
Non-Volatile Memory	OTP (16kB)
On-Chip RAM	1kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8927320vsc00tr

External Bus and External Registers. The following is made to clarify naming conventions used in this specification. The external bus and external registers are external to the DSP core, and are used to access internal and external peripherals.

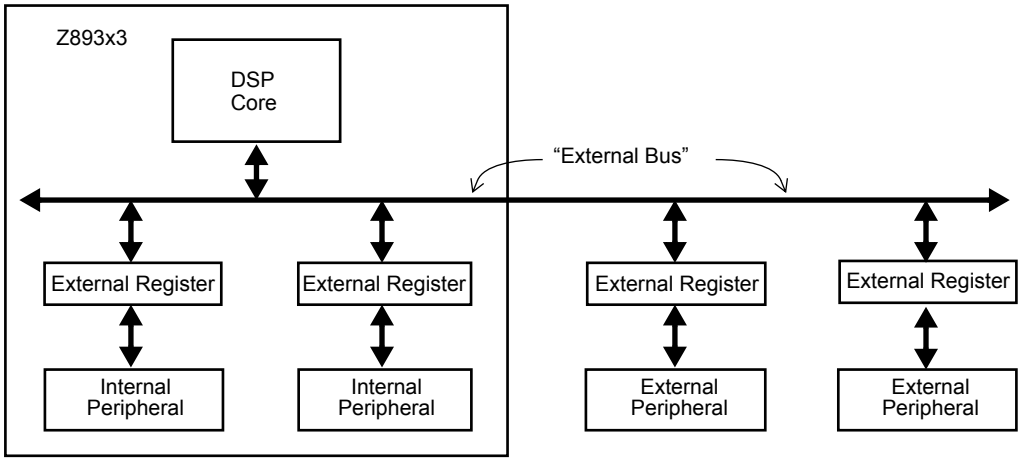


Figure 2. "External" Bus

PIN FUNCTIONS

EA2–EA0. External Address Bus (output, latched). These pins provide the External Register Address. This address bus is driven during both internal and external accesses. One of up to seven user-defined external registers is selected by the processor for reads or writes. EXT7 is always reserved for use by the processor.

ED15–ED0. External Data Bus (input/output). These pins are the data bus for the user-defined external registers, and are shared by Port0. These pins are normally tristated, except when these registers are specified as destination registers in a write instruction to an external peripheral, or when Port0 is enabled for output. This bus uses the control signals RD/$\overline{WR}$, $\overline{DS}$, and $\overline{WAIT}$, and address pins EA2–EA0.

$\overline{DS}$. Data Strobe (output). This pin provides the data strobe signal for the ED Bus. $\overline{DS}$ is active for transfers to/from external peripherals only.

RD/$\overline{WR}$. Read/$\overline{Write}$ Select (output). This pin controls the data direction signal for the External Data Bus. Data is available from the processor on ED15–ED0 when this signal and $\overline{DS}$ are both Low.

$\overline{WAIT}$. Wait State (input). This pin is sampled at the rising edge of the clock with appropriate setup and hold times. A single wait-state can be generated internally by setting the appropriate bits in the wait state register. The user must drive this line if multiple wait states are required. This pin is shared with Port2.

CLKI. Clock (input). This pin is the clock circuit input. It can be driven by a signal or connected to a 32 KHz crystal.

CLKO. Clock (output). This pin is the clock circuit output. It is used for operation with a 32 KHz crystal and the PLL to generate the system clock.

$\overline{HALT}$. Halt State (input). This pin stops program execution. The processor continuously executes NOPs and the program counter remains constant while this pin is held Low. This pin offers an internal pull-up.

$\overline{RESET}$. Reset (input). This pin resets the processor. It pushes the contents of the Program Counter (PC) onto the stack and then fetches a new PC value from program memory address 0FFCH after the $\overline{RESET}$ signal is released. The Status register is set to all zeros. At power-up RAM and other registers are undefined, however, they are left unchanged with subsequent resets. $\overline{RESET}$ can be asserted asynchronously.

AN0–AN3. Analog Inputs (input). These are the analog input pins. The analog input signal should be between VALO and VAHI for accurate conversions.

VAHI. Analog High Reference Voltage (input). This pin provides the reference for the full scale voltage of the analog input signals.

VALO. Analog Low Reference Voltage (input). This pin provides the reference for the zero voltage of the analog input signals.

AV_{CC}–AGND. Filtered Analog Power and Ground must be provided on separate pins to reduce digital noise in the analog circuits.

Multifunction Pins. The Z89223/273/323/373 DSP family offers a user-configurable I/O structure, which means that most of the I/O pins offer dual functions. The function, direction (input or output), and for output, the characteristics (push-pull or open drain) are all under user-control, by programming the configuration registers appropriately as described in the I/O Ports section. The following share I/O Port pins:

INT0–INT2. External Interrupts (input, edge-triggered). These pins provide three of the eight interrupt sources to the Interrupt Controller. Each is programmable to be rising-edge or falling-edge triggered. The other five interrupt sources are from the on-chip peripherals.

CLKOUT. System Clock (output). This pin provides access to the internal processor clock.

SDI. Serial Data In (input). This pin is the SPI serial data input.

SDO. Serial Data Out (output). This pin is the SPI serial data output.

SS. Slave Select (input). This pin is used in SPI Slave Mode only. SS advises the SPI that it is the target of a serial transfer from an external Master.

SCLK. SPI Clock (output/input). This pin is an output in Master mode and an input in Slave mode.

UI0, UI1. User inputs (input). These general-purpose input pins are directly tested by the conditional branch instructions. They can also be read as bits in the status register. These are asynchronous input signals that require no special clock synchronization. Counter/Timer0 and Counter/Timer1 may use either of these pins as input.

UI2. User Input (input). This pin is the input to Counter/Timer 2.

TMO0/UO0. Counter/Timer Output or User Output 0 (output). Counter/Timer 0 and Counter/Timer 1 can be programmed to provide output on this pin. When User Outputs are enabled, and the Counter/Timer is disabled, this pin provides the complement of Status Register bit 5.

Table 3. 64-Pin TQFP Z89223/273 Pin Description

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	ED3/P0.3	External Data Bus/Port0	Input/Output	33	$\overline{HALT}$	Halt Execution	Input
2	ED4/P0.4	External Data Bus/Port0	Input/Output	34	EA0	Ext Address 0	Output
3	V_{SS}	Ground		35	EA1	Ext Address 1	Output
4	V_{DD}	Power Supply		36	EA2	Ext Address 2	Output
5	ED5/P0.5	External Data Bus/Port0	Input/Output	37	V_{DD}	Power Supply	
6	P1.3/SDO	Port 1.3/Serial Output	Input/Output	38	P2.3/TMO1	Port2.3/Timer Output 1	Input/Output
7	ED6/P0.6	External Data Bus/Port0	Input/Output	39	$\overline{DS}$	Ext Data Strobe	Output
8	P1.4/SS	Port 1.4/Slave Select	Input/Output	40	P2.4/$\overline{WAIT}$	Port 2.4/Wait for ED	Input/Output
9	ED7/P0.7	External Data Bus/Port0	Input/Output	41	CLKI	Clock/Crystal In	Input
10	P1.5/SCLK	Port 1.5/Serial Clock	Input/Output	42	CLKO	Clock/Crystal Out	Output
11	P2.7	Port 2.7	Input/Output	43	P2.6/TMO2	Port 2.6/Timer Output 2	Input/Output
12	ED8/P0.8	External Data Bus/Port0	Input/Output	44	P2.2/TMO0	Port 2.2/Timer Output 0	Input/Output
13	ED9/P0.9	External Data Bus/Port0	Input/Output	45	P2.5/UI2	Port 2.5/User Input 2	Input/Output
14	V_{SS}	Ground		46	LPF	PLL Low Pass Filter	Input
15	ED10/P0.10	External Data Bus/Port0	Input/Output	47	$\overline{RESET}$	Reset	Input
16	V_{SS}	Ground		48	V_{SS}	Ground	
17	ED11/P0.11	External Data Bus/Port0	Input/Output	49	V_{DD}	Power Supply	
18	VAHI	Analog High Ref. Voltage	Input	50	V_{SS}	Ground	
19	V_{SS}	Ground		51	ED0/P0.0	External Data Bus/Port0	Input/Output
20	P1.6/UI0	Port 1.6/User Input 0	Input/Output	52	ED1/P0.1	External Data Bus/Port0	Input/Output
21	VALO	Analog Low Ref. Voltage	Input	53	ED2/P0.2	External Data Bus/Port0	Input/Output
22	P1.7/UI1	Port 1.7/User Input 1	Input/Output	54	P1.0/INT2	Port 1.0/Interrupt 2	Input/Output
23	AGND	Analog Ground		55	V_{SS}	Ground	
24	AN0	A/D Input 0	Input	56	P1.1/CLKOUT	Port 1.1/Clock Output	Input/Output
25	AN1	A/D Input 1	Input	57	P1.2/SDI	Port 1.2/Serial Input	Input/Output
26	AN2	A/D Input 2	Input	58	P2.0/INT0	Port 2.0/Interrupt 0	Input/Output
27	AN3	A/D Input 3	Input	59	ED12/P0.12	External Data Bus/Port0	Input/Output
28	V_{SS}	Ground		60	ED13/P0.13	External Data Bus/Port0	Input/Output
29	P2.1/INT1	Port 2.1/Interrupt 1	Input/Output	61	V_{DD}	Power Supply	
30	AVCC	Analog Power		62	ED14/P0.14	External Data Bus/Port0	Input/Output
31	V_{DD}	Power Supply		63	V_{SS}	Ground	
32	RD/$\overline{WR}$	R/W External Bus	Output	64	ED15/P0.15	External Data Bus/Port0	Input/Output

PIN CONFIGURATIONS (Continued)

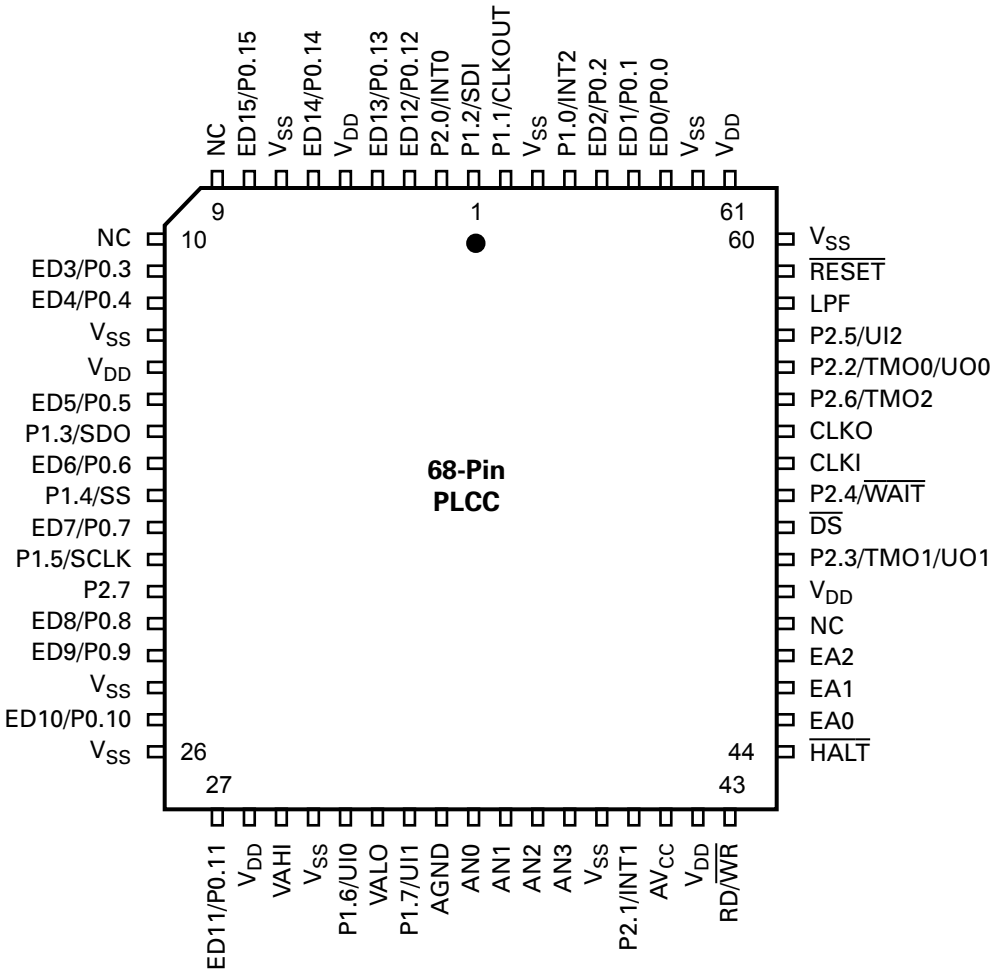


Figure 6. 68-Pin PLCC Z89323/373 Pin Configuration

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage	–0.3	7.0	V
T_{STG}	Storage Temperature	–65	150	°C
T_A	Ambient Operating Temperature			
	"S" device	0	70	°C
	"E" device	–40	85	°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin.

Positive current $I_{(+)}$ flows in to the referenced pin.

Negative current $I_{(-)}$ flows out of the referenced pin.

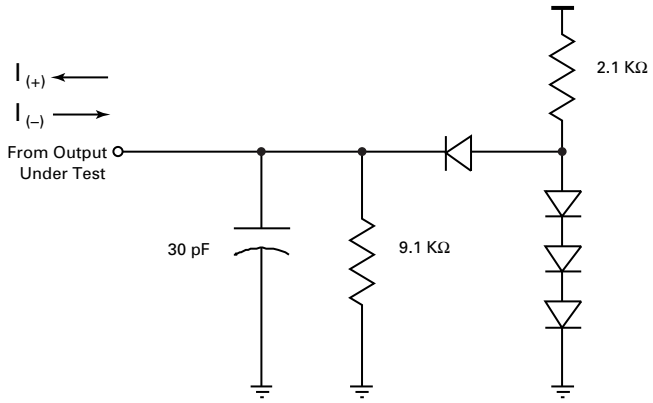


Figure 8. Test Load Diagram

DC ELECTRICAL CHARACTERISTICS (Continued)

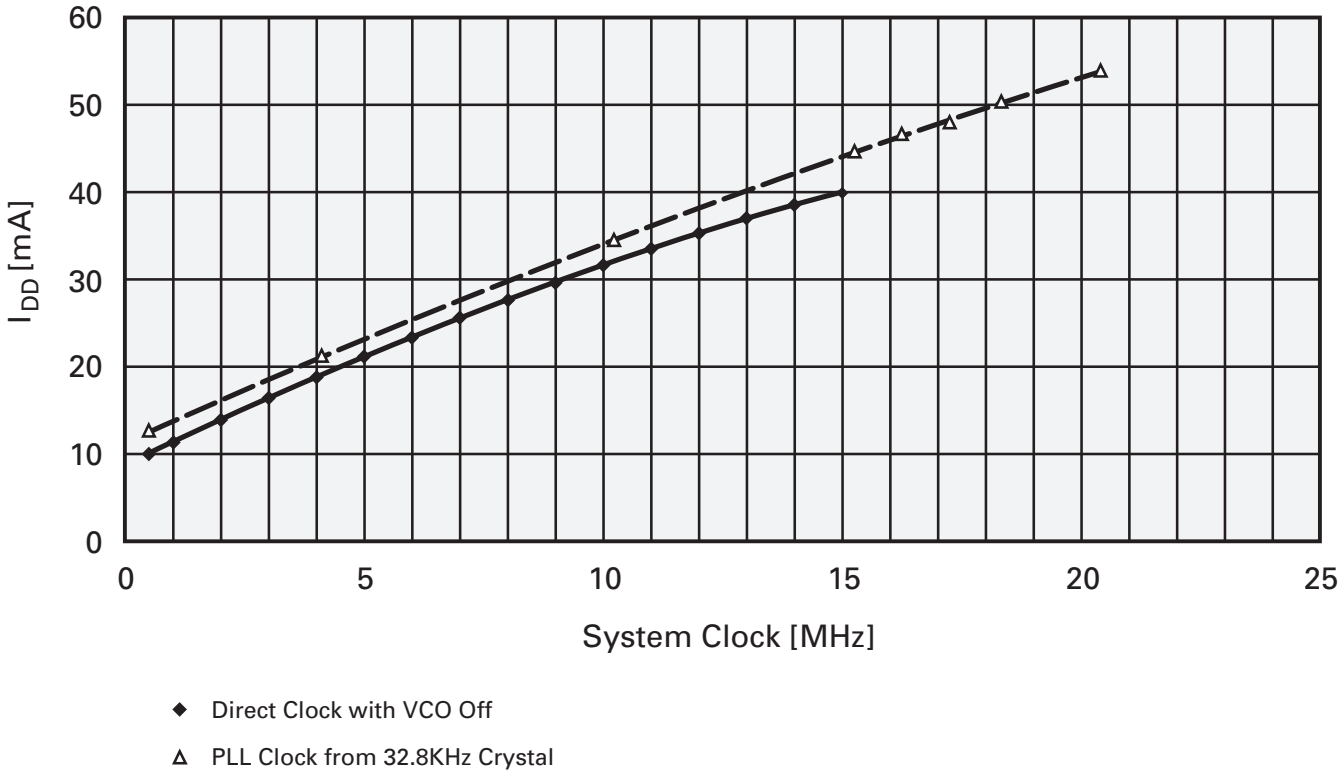


Figure 9. Z89373 Typical OTP Current Consumption

TIMING DIAGRAMS

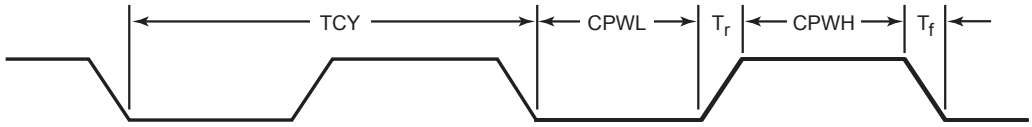


Figure 10. Clock Timing

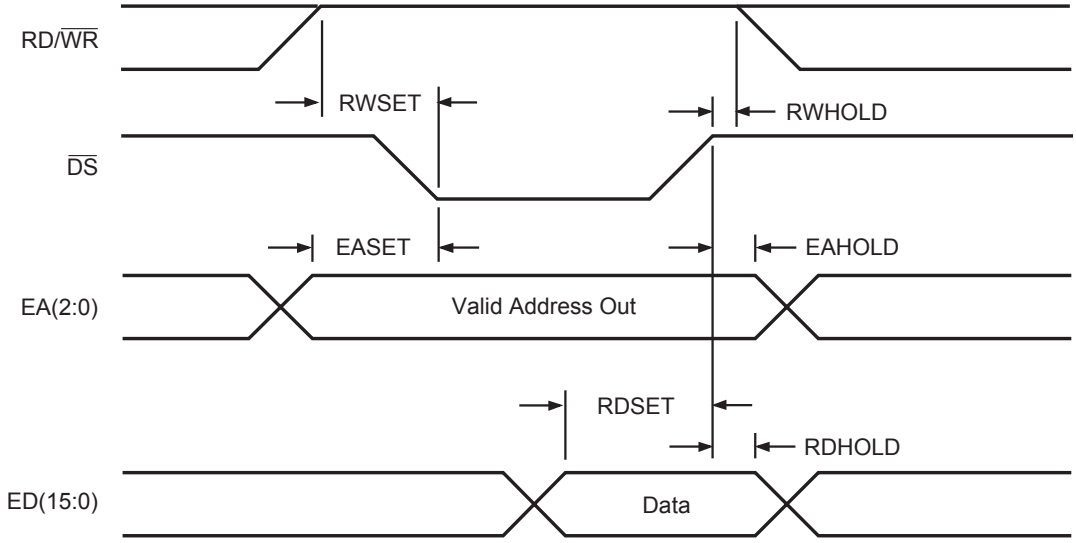


Figure 11. Read Timing

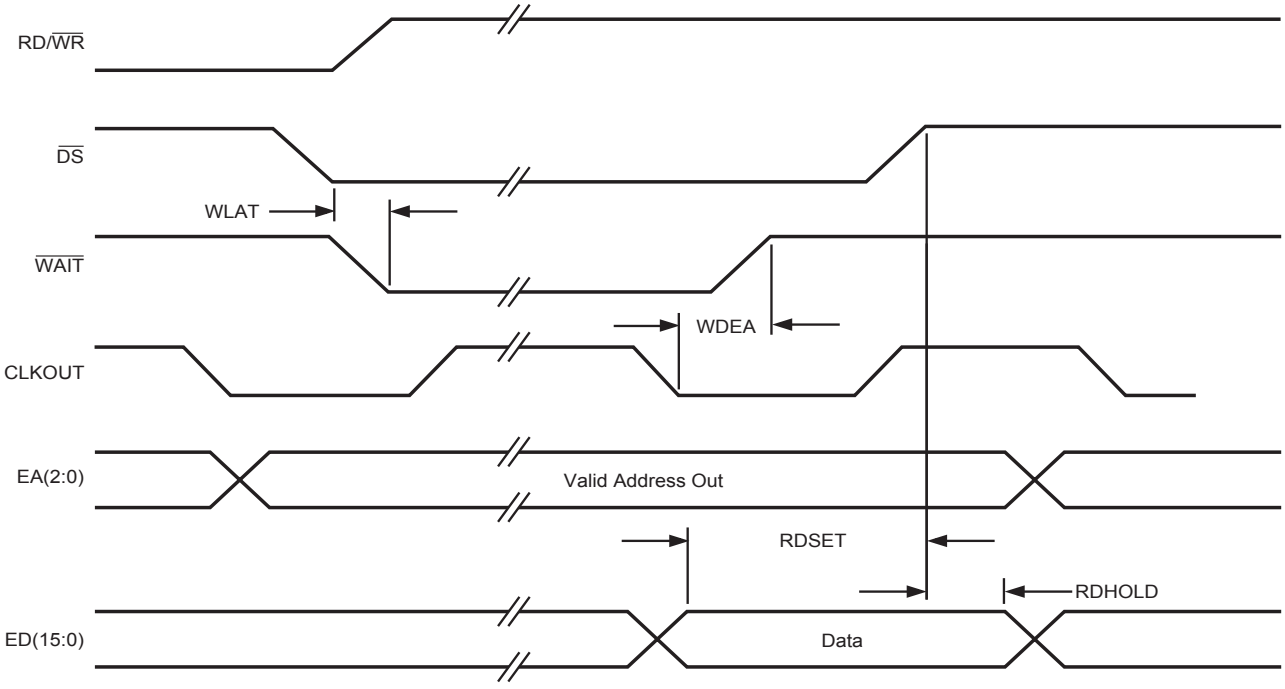


Figure 12. Read Timing Using $\overline{WAIT}$ Pin

BANK/EXT REGISTER ASSIGNMENTS

There are 16 different Banks of EXT registers. Control of the bank switching is done via the EXT7 register. The same EXT7 register exists in all Banks.

Banks 0–5 support different combinations of external registers for external peripherals, and external registers for internal (on-chip) peripherals. Use the bank that offers the optimum combination of internal and external registers to support the application. Use it as a preferred working bank to minimize bank switching.

Banks 6–12 only decode EXT6 and EXT7. Do not use EXT0–5 for Banks 6–12.

Banks 13–15 are control register banks. These banks are used in the initialization routines and whenever a configuration change is required. Refer to the sections on I/O Ports and Peripherals for details.

Table 13. EXT Register Assignments Banks 0–4

	Bank0	Bank1	Bank2	Bank3	Bank4
EXT0	User	User	User	User	User
EXT1	User	User	User	User	User
EXT2	User	User	User	User	User
EXT3	SPI Data	User	User	SPI Data	User
EXT4	Port0 Data	Port0 Data	User	User	User
EXT5	Port2–Port1 Data	Port2–Port1 Data	Port3 Data	User	User
EXT6	A/D_Ch0 Data	A/D_Ch1 Data	A/D_Ch2 Data	A/D_Ch3 Data	User
EXT7	Interrupt status/ Bank Select	Interrupt status/ Bank Select	Interrupt status/ Bank Select	Interrupt status/ Bank Select	Interrupt status/ Bank Select

Table 14. EXT Register Assignments Banks 5–15

	Bank5	Bank6–12	Bank13	Bank14	Bank15
EXT0	A/D_Ch1 Data	not defined	A/D Control	C/T2 Load/Read	Port0 Control
EXT1	A/D_Ch2 Data	not defined	C/T0 Control	C/T1 Control	Port1 Ctrl/Port0 Alloc
EXT2	A/D_Ch3 Data	not defined	C/T0 Load	C/T1 Load	Ports 2, 3, & C/T2 Control
EXT3	SPI Data	not defined	C/T0 Counter	C/T1 Counter	Wait State Control
EXT4	Port0 Data	not defined	C/T0 Prescaler Ld	C/T1 Prescaler Ld	SPI Control
EXT5	Port2–Port1 Data	not defined	C/T0 Prescaler	C/T1 Prescaler	System Clock Control
EXT6	A/D_Ch0 Data	A/D_Ch0 Data	A/D_Ch0 Data	Interrupt Polarity	Interrupt Allocation
EXT7	Interrupt status/ Bank Select	Interrupt status/ Bank Select	Interrupt status/ Bank Select	Interrupt status/ Bank Select	Interrupt status/ Bank Select

BANK/EXT REGISTER ASSIGNMENTS (Continued)

Interrupt Status/Bank Select Register—EXT7

Following is a description of EXT7. It contains both a Bank Select Field and Interrupt Status Bits.

Bank Select Field. The four LSBs of EXT7 denote which bank is selected as the current working bank.

Interrupt Status Bits. These bits can be read to identify which interrupts are pending. A "1" denotes interrupt pending, and a "0" denotes no interrupt. This ability to identify interrupts is particularly useful in polled interrupt operation or when servicing ISR2, which may come from several sources.

Note: Write "1" to a particular status bit to clear that bit. Before exiting an interrupt service routine, the relevant interrupt bit(s) should be cleared. To clear a bit efficiently:

- Load the value of EXT7 into a register or memory location
- Then load that value back into EXT7

Performing these steps clear all of the interrupts that were pending, but leave the Register Bank Select unchanged.

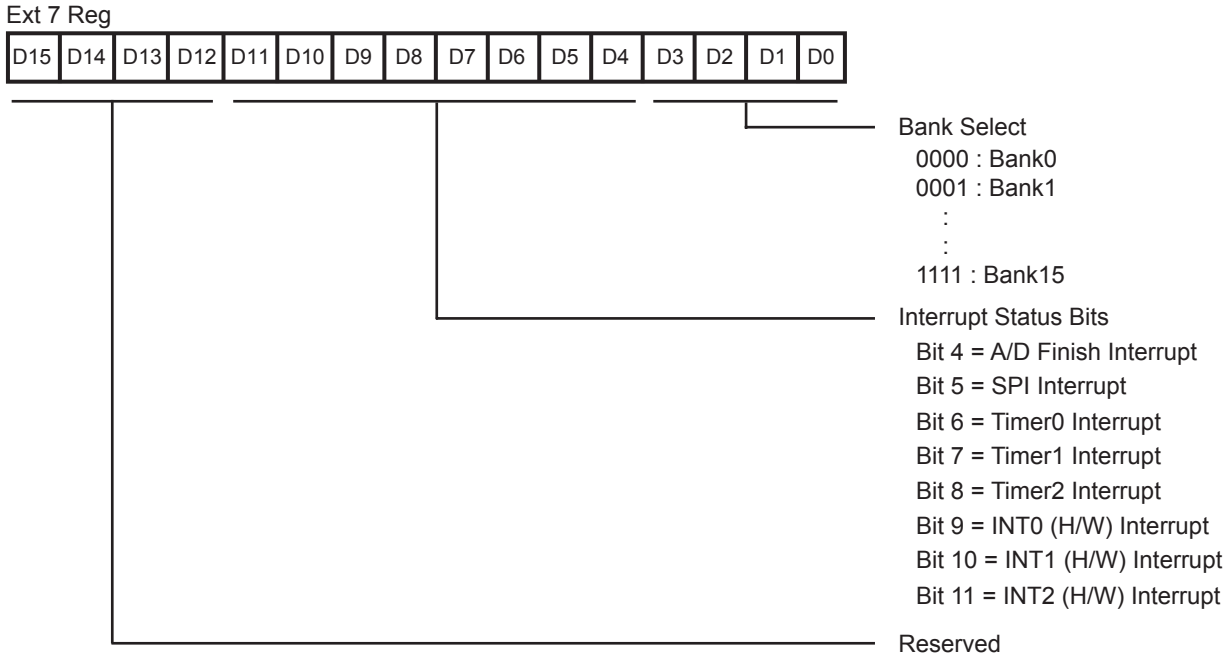


Figure 20. EXT7 Register

I/O PORTS

I/O pin allocation of ports for the different package types is designed to provide configuration flexibility. Each port line of Ports 0, 1, and 2 can be independently selected as an input or an output. Each port's output lines can be globally selected as push-pull or as open-drain outputs

Table 15. I/O Port Bit Allocations

Device Pins	44-Pin PLCC, 44-Pin PQFP	64-Pin TQFP, 68-Pin PLCC	80-Pin PQFP
P0 MSB	ED15–ED8, or P0.15–P0.8, or P1.7–P1.0	ED15–ED8, or P0.15–P0.8	ED15–ED8, or P0.15–P0.8
P0 LSB	ED7–ED0, or P0.7–P0.0	ED7–ED0, or P0.7–P0.0	ED7–ED0, or P0.7–P0.0
P1		P1.7–P1.0	P1.7–P1.0
P2	P2.4–P2.0	P2.7–P2.0	P2.7–P2.0
P3			P3.7–P3.0

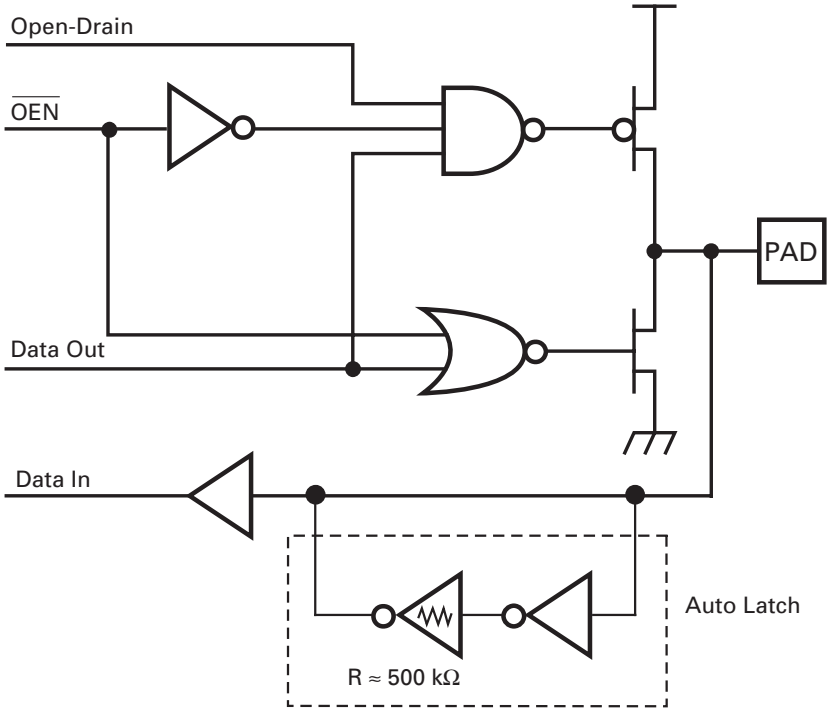


Figure 24. Port 0, 1 and 2 Configuration

Port1—8-Bit Programmable I/O

Bank15/EXT1 is the Port1 control register. The MSB is the Port1 direction control. Port1 data is accessed as the LSB of EXT5 in Banks 0, 1, or 5. The Port1 pins can also be mapped to internal functions. When INT2, CLKOUT, UI0 and UI1, or the SPI are enabled, they use Port1 pins. The 44-pin packages do not feature Port1 pins, however, Port1 and its internal functions can be mapped to the MSB of the ED Bus/Port0 pins. See bits 2–0 of Bank15/EXT1.

Table 16. Port1 Bit Function Allocation

Port Pin	IF	Condition	Then	Else
P1.0/INT2	Bank15/EXT1 Bit 3 = 1	Enable INT2	INT2	P1.0
P1.1/CLKOUT	Bank15/EXT1 Bit 5 = 1	Enable CLKOUT	CLKOUT	P1.1
P1.2/SDI	Bank15/EXT4 Bit 0 = 1	Enable SPI	SDI	P1.2
P1.3/SDO	Bank15/EXT4 Bit 0 = 1	Enable SPI	SDO	P1.3
P1.4/SS	Bank15/EXT4 Bit 0 = 1	Enable SPI	SS	P1.4
P1.5/SCLK	Bank15/EXT4 Bit 0 = 1	Enable SPI	SCLK	P1.5
P1.6/UI0	Bank13/EXT1 Bits [2,1] = 10, or Bank14/EXT1 Bits [2,1] = 10	Enable UI0	UI0	P1.6
P1.7/UI1	Bank13/EXT1 Bits [2,1] = 11, or Bank14/EXT1 Bits [2,1] = 11	Enable UI1	UI1	P1.7

PERIPHERALS

Analog to Digital Converter (A/D)

The A/D is a 4-channel 8-bit half-flash converter. It uses two reference resistor ladders, one for the upper 5 bits, and another for the lower 3 bits. Two external reference voltage input pins, VAHI and VALO, set the input voltage measurement conversion range. The converter is auto-zeroed prior to each sampling period. Bank13/EXT0 is the A/D control register.

The conversion time depends on the system clock frequency and the selection of the A/D prescaler value, bits DIV2–DIV0. The clock prescaler can be programmed to derive a 2 µs conversion time. For example, when deriving the A/D clock from a 20-MHz system clock, the A/D prescaler value should be set to divide by 40.

Bits ADST1–ADST0 determine one of the following start conversion options:

- Writing to the ADCTL control register
- ISR1
- C/T2 time-out
- C/T0 time-out

The start conversion operation may begin at any time. If a conversion is in progress, and a new start conversion signal is received, the conversion in progress will abort, and a new conversion will initiate.

Bits QUAD and SCAN determine one of the following Modes of operation:

- One channel is converted four times, with the results sequentially written to result registers 0, 1, 2 and 3.
- One channel is converted one time, with the respective result register updated.
- Four channels are converted one time each, with the respective four result registers updated.
- Four channels are converted repeatedly, with the respective four result registers constantly updated.

When one of the two four-channel modes is selected, the channel specified by CSEL1–CSEL0 will convert first. The other three channels will convert in sequence. In the sequence, AN0 follows AN3.

Bit ADIE enables the A/D to generate interrupts at the end of a conversion. Bit ADIT determines whether an interrupt occurs after the first or fourth conversion.

To reduce power consumption the A/D can be disabled by clearing the ADE bit.

Though the A/D will function with smaller input signals and reference voltages, the noise and offsets remain constant. The relative error of the converter will increase and the conversion time will also take longer.

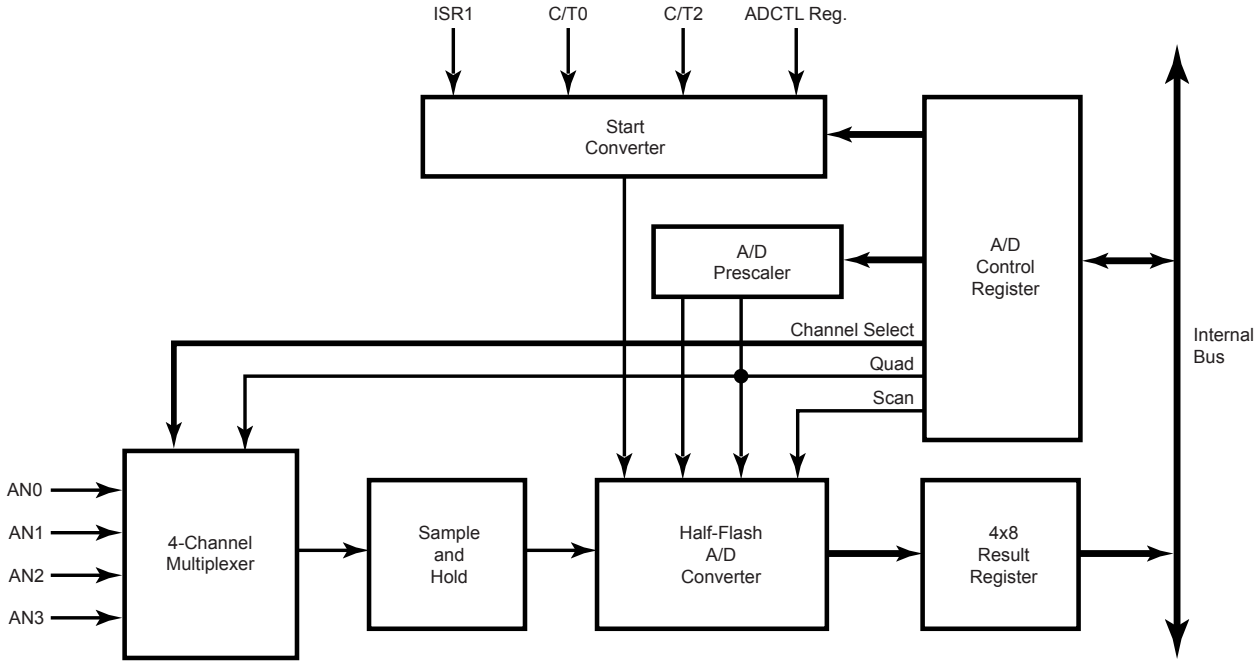


Figure 28. ADC Architecture

GENERAL-PURPOSE COUNTER/TIMER (C/T2) (Continued)

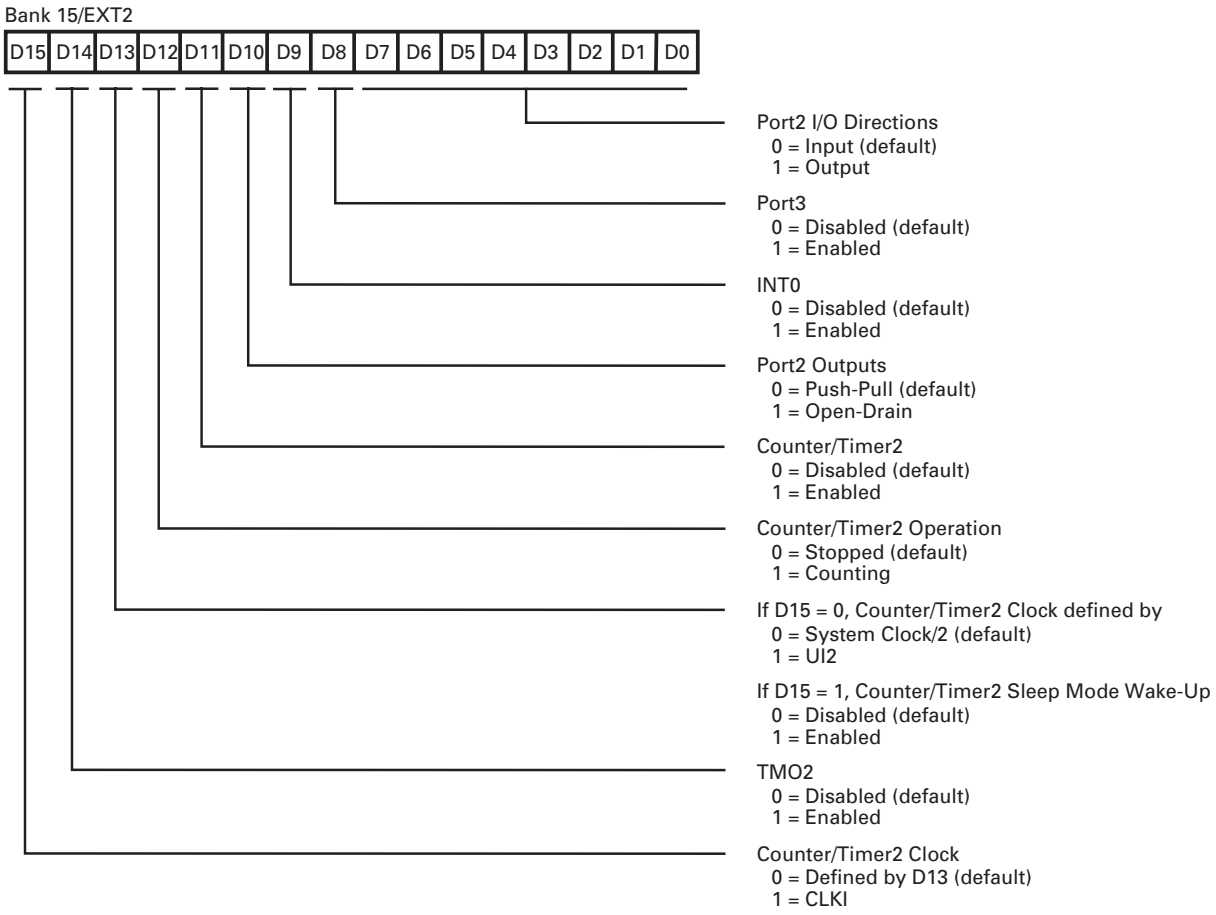


Figure 38. Counter/Timer2 Control Register

SERIAL PERIPHERAL INTERFACE (Continued)

Slave Mode Operation

SS must be asserted to enable a data transfer. Incoming data on the SDI pin is shifted into the SPI Shift Register one data bit per SCLK cycle. When a byte of data is received, the SPI Shift Register contents are automatically copied into RxBUF. The Receive Byte Available flag is set, and if enabled, an SPI interrupt is generated. The next byte of data may be received at this time. The current byte in RxBUF must be read before the next byte's reception is complete, or the Receive Byte Overrun flag will set, and the data in RxBUF will be overwritten. The Receive Byte Available flag is reset when RxBUF is read.

Unless the SPI output, SDO, is disabled, for every bit that is transferred into the slave through the SDI pin, a bit is transferred out through the SDO pin on the opposite clock edge. During slave operation, SCLK is an input.

Note: Slave Mode is not available on the 44-pin package.

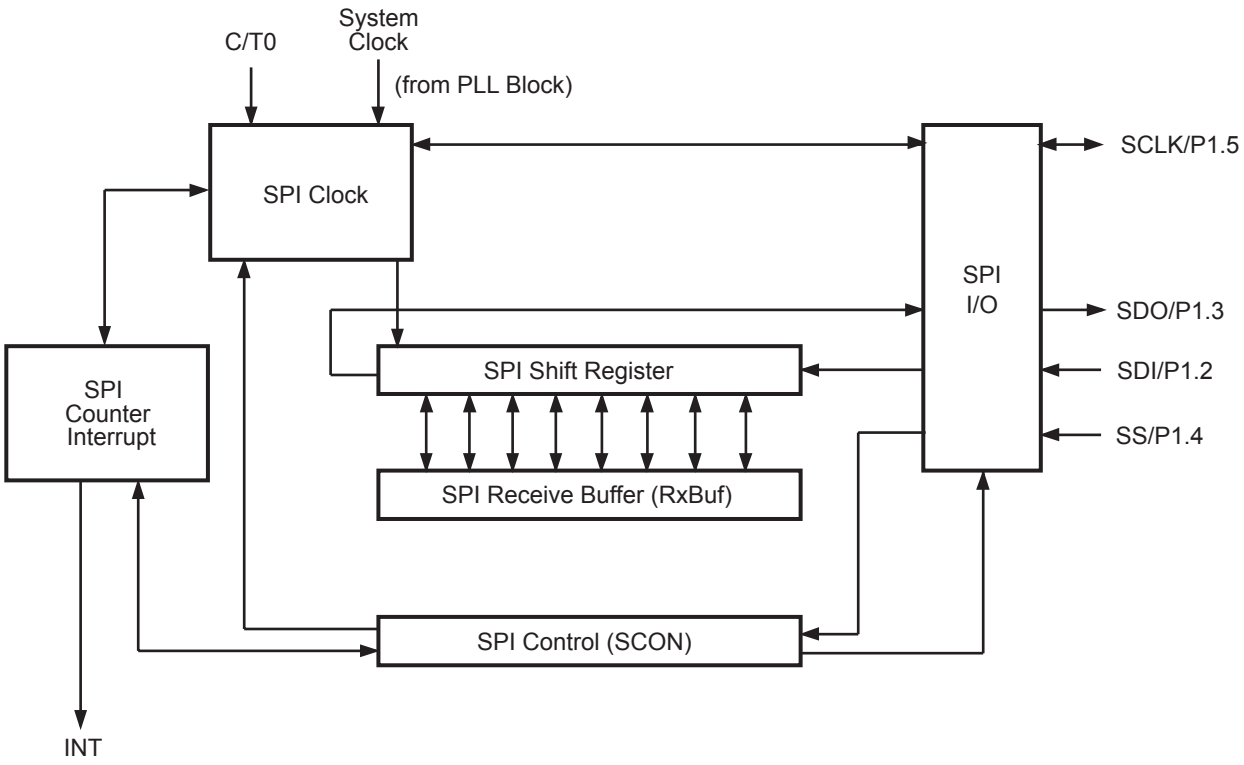


Figure 41. SPI Block Diagram

CONDITION CODES

The following Instruction Description defines the condition codes supported by the DSP assembler. If the instruction description refers to the <cc> (condition code) symbol in one of its addressing modes, the instruction only executes if the condition is true.

Code	Description
C	Carry
EQ	Equal (same as Z)
F	False
IE	Interrupts Enabled
MI	Minus
NC	No Carry
NE	Not Equal (same as NZ)
NIE	Not Interrupts Enabled
NOV	Not Overflow
NU0	Not User Zero
NU1	Not User One
NZ	Not zero
OV	Overflow
PL	Plus (Positive)
U0	User Zero
U1	User One
UGE	Unsigned Greater Than or Equal (Same as NC)
ULT	Unsigned Less Than (Same as C)
Z	Zero

INSTRUCTION DESCRIPTIONS (Continued)

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
LD	Load destination with source	LD<dest>,<src>	A,<hwregs>	1	1	LD A,X
			A,<dregs>	1	1	LD A,D0:0
			A,<pregs>	1	1	LD A,P0:1
			A,<regind>	1	1	LD A,@P1:1
			A,<memind>	1	3	LD A,@D0:0
			A,<direct>	1	1	LD A,124
			<direct>,A	1	1	LD 124,A
			<dregs>,<hwregs>	1	1	LD D0:0,EXT7
			<pregs>,<simm>	1	1	LD P1:1,#%FA
			<pregs>,<hwregs>	1	1	LD P1:1,EXT1
			<regind>,<limm>	1	1	LD@P1:1,#1234
			<regind>,<hwregs>	1	1	LD @P1:1+,X
			<hwregs>,<pregs>	1	1	LD Y,P0:0
			<hwregs>,<dregs>	1	1	LD SR,D0:0
			<hwregs>,<limm>	2	2	LD PC,#%1234
			<hwregs>,<accind>	1	3	LD X,@A
			<hwregs>,<memind>	1	3	LD Y,@D0:0
			<hwregs>,<regind>	1	1	LD A,@P0:0–LOOP
			<hwregs>,<hwregs>	1	1	LD X,EXT6

Notes:
When <dest> is <hwregs>, <dest> cannot be P.
When <dest> is <hwregs> and <src> is <hwregs>, <dest> cannot be EXTn if <src> is EXTn, <dest> cannot be X if <src> is X, <dest> cannot be SR if <src> is SR.
When <src> is <accind> <dest> cannot be A.

MLD	Multiply	MLD <src1>,<src2> [,<bank switch>]	<hwregs>,<regind>	1	1	MLD A,@P0:0+LOOP
			<hwregs>,<regind>, <bank switch>	1	1	MLD A,@P1:0,OFF
			<regind>,<regind>	1	1	MLD @P1:1,@P2:0
			<regind>,<regind>, <bank switch>	1	1	MLD @P0:1,@P1:0,ON

Notes:
If src1 is <regind> it must be a bank 1 register. Src2's <regind must be a bank 0 register.
<hwregs> for src1 cannot be X.
For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, the <bank switch> defaults to ON.

MPYA	Multiply and add	MPYA <src1>,<src2> [,<bank switch>]	<hwregs>,<regind>	1	1	MPYA A,@P0:0
			<hwregs>,<regind>, <bank switch>	1	1	MPYA A,@P1:0,OFF
			<regind>,<regind>	1	1	MPYA @P1:1,@P2:0
			<regind>,<regind>, <bank switch>	1	1	MPYA@P0:1,@P1:0,ON

Notes:
If src1 is <regind> it must be a bank 1 register. Src2's <regind> must be a bank 0 register.
<hwregs> for src1 cannot be X.
For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, the <bank switch> defaults to ON.

MPYS	Multiply and subtract	MPYS <src1>,<src2> [,<bank switch>]	<hwregs>,<regind>	1	1	MPYS A,@P0:0
			<hwregs>,<regind>, <bank switch>	1	1	MPYS A,@P1:0,OFF
			<regind>,<regind>	1	1	MPYS @P1:1,@P2:0
			<regind>,<regind>, <bank switch>	1	1	MPYS @P0:1,@P1:0,ON

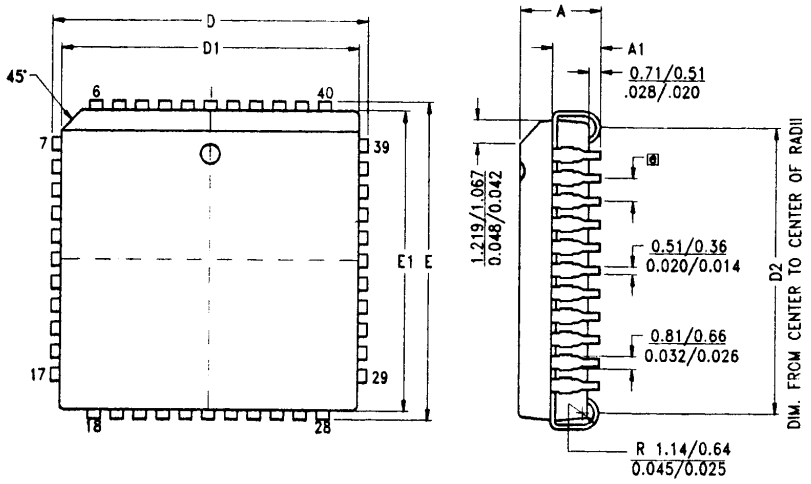
Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
Notes:						
If src1 is <regind> it must be a bank 1 register. Src2's <regind> must be a bank 0 register.						
<hwregs> for src1 cannot be X.						
For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, <regind> the <bank switch> defaults to ON.						
NEG	Negate	NEG <cc>,A	<cc>, A	1	1	NEG MI,A
			A	1	1	NEG A
NOP	No operation	NOP	None	1	1	NOP
OR	Bitwise OR	OR <dest>,<src>	A,<pregs>	1	1	OR A,P0:1
			A,<dregs>	1	1	OR A, D0:1
			A,<limm>	2	2	OR A,#%2C21
			A,<memind>	1	3	OR A,@@P2:1+
			A,<direct>	1	1	OR A, %2C
			A,<regind>	1	1	OR A,@P1:0–LOOP
			A,<hwregs>	1	1	OR A,EXT6
			A,<simm>	1	1	OR A,#%12
POP	Pop value from stack	POP <dest>	<pregs>	1	1	POP P0:0
			<dregs>	1	1	POP D0:1
			<regind>	1	1	POP @P0:0
			<hwregs>	1	1	POP A
PUSH	Push value onto stack	PUSH <src>	<pregs>	1	1	PUSH P0:0
			<dregs>	1	1	PUSH D0:1
			<regind>	1	1	PUSH @P0:0
			<hwregs>	1	1	PUSH BUS
			<limm>	2	2	PUSH #12345
			<accind>	1	3	PUSH @A
			<memind>	1	3	PUSH @@P0:0
RET	Return from subroutine	RET	None	1	2	RET
RL	Rotate Left	RL <cc>,A	<cc>,A	1	1	RL NZ,A
			A	1	1	RL A
RR	Rotate Right	RR <cc>,A	<cc>,A	1	1	RR C,A
			A	1	1	RR A
SCF	Set C flag	SCF	None	1	1	SCF
SIEF	Set IE flag	SIEF	None	1	1	SIEF
SLL	Shift left logical	SLL	[<cc>,]A	1	1	SLL NZ,A
			A	1	1	SLL A
SOPF	Set OP flag	SOPF	None	1	1	SOPF
SRA	Shift right arithmetic	SRA<cc>,A	<cc>,A	1	1	SRA NZ,A
			A	1	1	SRA A
SUB	Subtract	SUB<dest>,<src>	A,<pregs>	1	1	SUB A,P1:1
			A,<dregs>	1	1	SUB A,D0:1
			A,<limm>	2	2	SUB A,#%2C2C
			A,<memind>	1	3	SUB A,@D0:1
			A,<direct>	1	1	SUB A,%15
			A,<regind>	1	1	SUB A,@P2:0–LOOP
			A,<hwregs>	1	1	SUB A,STACK
			A,<simm>	1	1	SUB A, #%12

INSTRUCTION DESCRIPTIONS (Continued)

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
XOR	Bitwise exclusive OR	XOR <dest>,<src>	A,<pregs>	1	1	XOR A,P2:0
			A,<dregs>	1	1	XOR A,D0:1
			A,<limm>	2	2	XOR A,#13933
			A,<memind>	1	3	XOR A,@@P2:1+
			A,<direct>	1	1	XOR A,%2F
			A,<regind>	1	1	XOR A,@P2:0
			A,<hwregs>	1	1	XOR A,BUS
			A,<simm>	1	1	XOR A, #%12

Bank Switch Operand. The third (optional) operand of the MLD, MPYA and MPYS instructions represents whether the bank switch is set to ON or OFF. To illustrate, the keywords ON and OFF are used to state the direction of the switch. These keywords are referenced in the instruction descriptions through the <bank switch> symbol. The most notable capability is that a source operand can be multiplied by itself (squared).

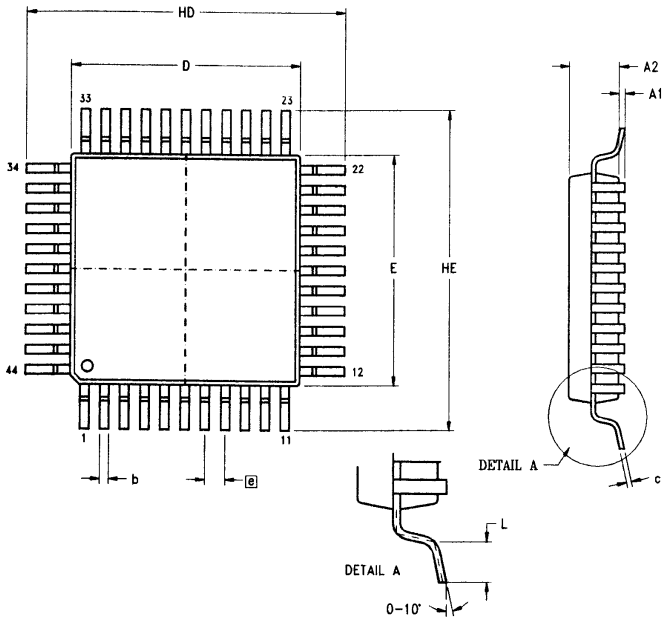
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 TYP		0.050 TYP	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM / INCH

Figure 44. 44-Pin PLCC Package Diagram

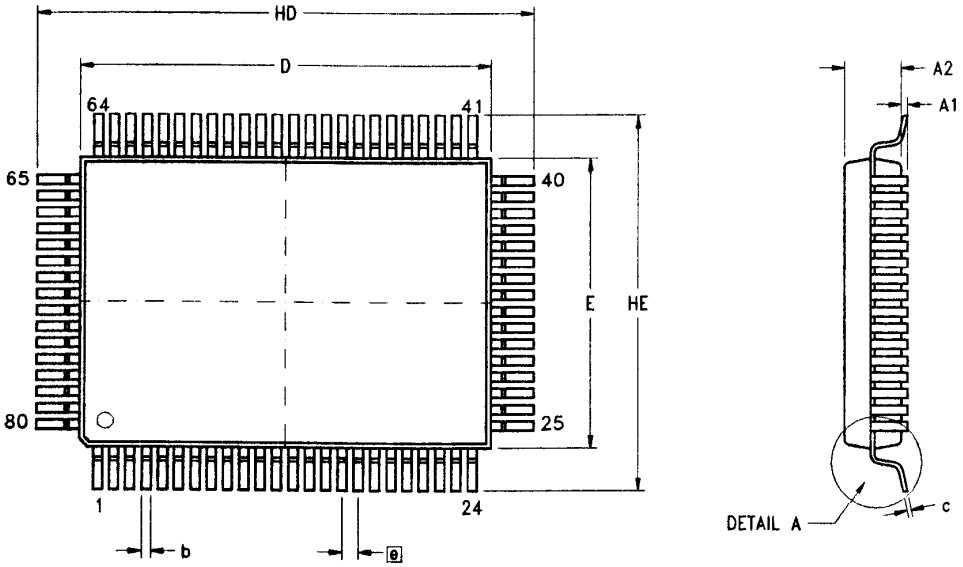


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 TYP		.0315 TYP	
L	0.60	1.20	.024	.047

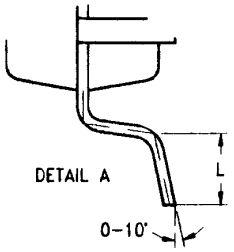
NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 / .004"

Figure 45. 44-Pin PQFP Package Diagram

PACKAGE INFORMATION (Continued)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.10	0.30	.004	.012
A2	2.60	2.80	.102	.110
b	0.30	0.45	.012	.018
c	0.13	0.20	.005	.008
HD	23.70	24.15	.933	.951
D	19.90	20.10	.783	.791
HE	17.70	18.15	.697	.715
E	13.90	14.10	.547	.555
e	0.80 TYP		.0315 TYP	
L	0.70	1.10	.028	.043



NOTES:
1. CONTROLLING DIMENSIONS: MILLIMETER
2. MAX COPLANARITY: .10 / .004

Figure 48. 80-Pin PQFP Package Diagram