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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	SPI, 3-Wire Serial
Clock Rate	20MHz
Non-Volatile Memory	OTP (16kB)
On-Chip RAM	1kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8927320vsg

GENERAL DESCRIPTION (Continued)

OTP version of the Z89223/323, is ideal for prototypes and early production builds.

Throughout this specification, references to the Z893x3 device apply equally to the Z89223/273/323/373, unless otherwise specified.

Notes: All signals with an overline are active Low. For example, in RD/$\overline{WR}$, RD is active High and $\overline{WR}$ is active Low. For I/O ports, P1.3 denotes Port1 bit 3. Pins called NC are "No Connection"—they do not connect any power, grounds, or signals.

Power connections follow conventional descriptions:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

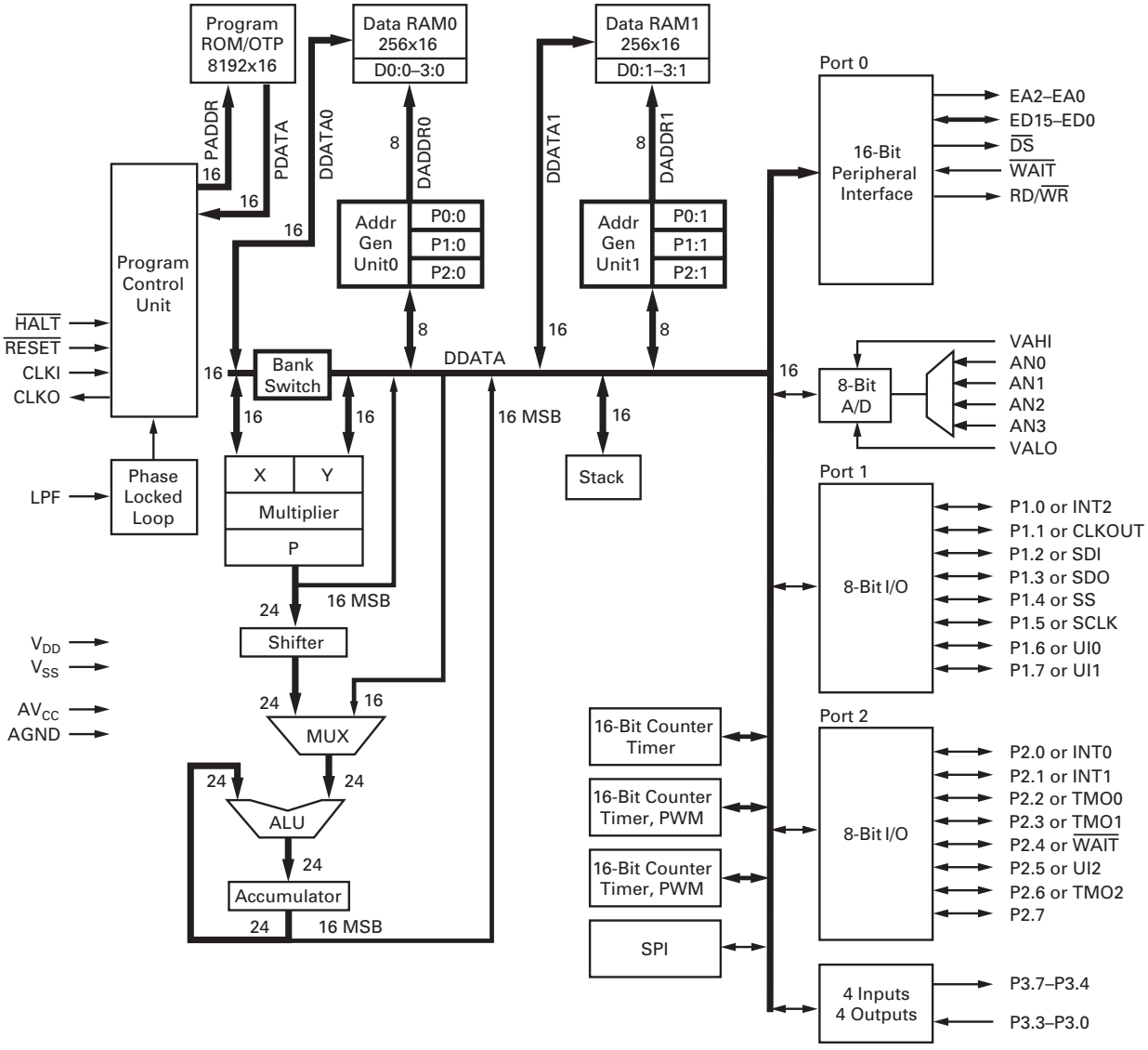


Figure 1. Z892X3/3x3 Functional Block Diagram

TMO1/UO1. Counter/Timer Output or User Output 1 (output). Counter/Timer 0 and Counter/Timer 1 can be programmed to provide output on this pin. When User Outputs are enabled, and the Counter/Timer is disabled, this pin provides the complement of Status Register bit 6.

TMO2. Counter/Timer 2 Output (output). This pin is the output of Counter/Timer 2

P0.15–P0.0. Port0 (input/output). This is a 16-bit user I/O port. Bits can be configured as input or output or globally as open-drain output. When enabled, Port0 uses the 16 data lines of the ED bus. The function of these pins can be dynamically changed by writing to the Port0 configuration registers. The High byte can also be configured to Port1 as described in the I/O Port section.

P1.7–P1.0. Port1 (input/output). These pins are Port1 inputs or outputs when not configured for use as special purpose peripheral interface. The following eight pin functions preempt use of these pins when enabled. INT2, CLKOUT, SDI, SDO, SS, SCLK, UI0, UI1.

Note: These pins are not bonded out on the 44-pin packages.

P2.7–P2.0. Port2 (input/output). These pins are Port2 inputs or outputs when not configured as peripheral interfaces. The following seven pin functions preempt use of P2.6–P2.0 when enabled. INT0, INT1, TMO0/UO0, TMO1/UO1, $\overline{\text{WAIT}}$, UI2, TMO2. P2.7 does not include a dual function.

Note: P2.7–P2.5 are not bonded out on the 44-pin packages.

The following port pins are available only on the 80-pin package:

P3.7–P3.4. Port3 (output). These pins are Port3 outputs.

P3.3–P3.0. Port3 (input). These pins are Port3 inputs.

Table 1. 44-Pin PLCC Z89223/273 Pin Description

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	P2.0/INT0	Port 2.0/Interrupt 0	Input/Output	23	AN2	A/D Input 2	Input
2	ED12/P0.12	External Data Bus/Port0	Input/Output	24	AN3	A/D Input 3	Input
3	ED13/P0.13	External Data Bus/Port0	Input/Output	25	P2.1/INT1	Port 2.1/Interrupt 1	Input/Output
4	ED14/P0.14	External Data Bus/Port0	Input/Output	26	AV_{CC}	Analog Power	
5	V_{SS}	Ground		27	V_{DD}	Power Supply	
6	ED15/P0.15	External Data Bus/Port0	Input/Output	28	RD/$\overline{WR}$	R/W External Bus	Output
7	ED3/P0.3	External Data Bus/Port0	Input/Output	29	EA0	Ext Address 0	Output
8	ED4/P0.4	External Data Bus/Port0	Input/Output	30	EA1	Ext Address 1	Output
9	V_{SS}	Ground		31	EA2	Ext Address 2	Output
10	ED5/P0.5	External Data Bus/Port0	Input/Output	32	P2.3/TMO1	Port 2.3/Timer Output 1	Input/Output
11	ED6/P0.6	External Data Bus/Port0	Input/Output	33	$\overline{DS}$	Ext Data Strobe	Output
12	ED7/P0.7	External Data Bus/Port0	Input/Output	34	P2.4/$\overline{WAIT}$	Port 2.4/Wait for ED	Input/Output
13	ED8/P0.8	External Data Bus/Port0	Input/Output	35	CLKI	Clock/Crystal In	Input
14	ED9/P0.9	External Data Bus/Port0	Input/Output	36	CLKO	Clock/Crystal Out	Output
15	V_{SS}	Ground		37	P2.2/TMO0	Port 2.2/Timer Output 0	Input/Output
16	ED10/P0.10	External Data Bus/Port0	Input/Output	38	LPF	PLL Low Pass Filter	Input
17	ED11/P0.11	External Data Bus/Port0	Input/Output	39	$\overline{RESET}$	Reset	Input
18	VAHI	Analog High Ref. Voltage	Input	40	V_{DD}	Power	
19	VALO	Analog Low Ref. Voltage	Input	41	ED0/P0.0	External Data Bus/Port0	Input/Output
20	AGND	Analog Ground		42	ED1/P0.1	External Data Bus/Port0	Input/Output
21	AN0	A/D Input 0	Input	43	ED2/P0.2	External Data Bus/Port0	Input/Output
22	AN1	A/D Input 1	Input	44	V_{SS}	Ground	

PIN CONFIGURATIONS (Continued)

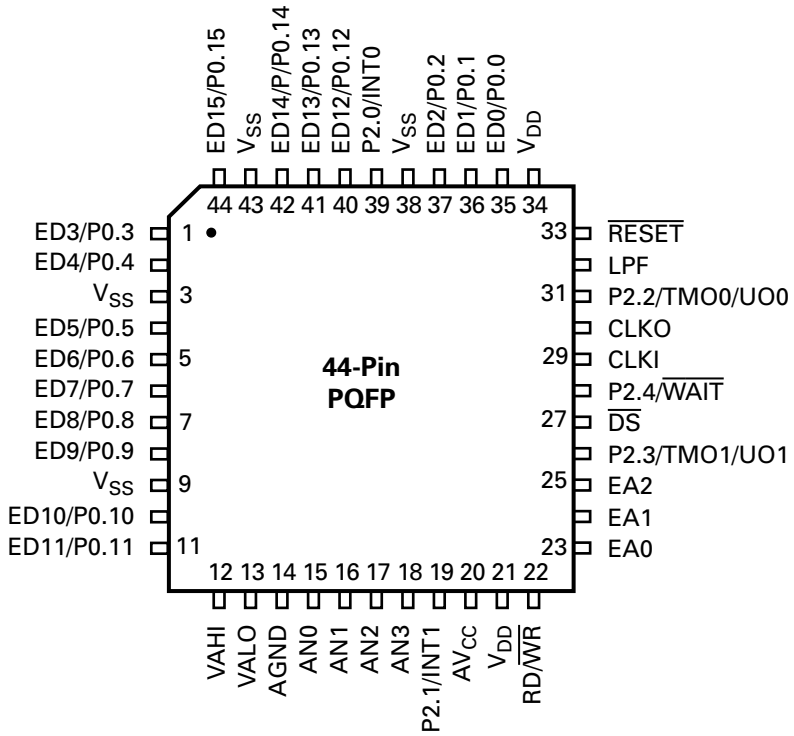


Figure 4. 44-Pin PQFP Z89223/273 Pin Configuration

PIN CONFIGURATIONS (Continued)

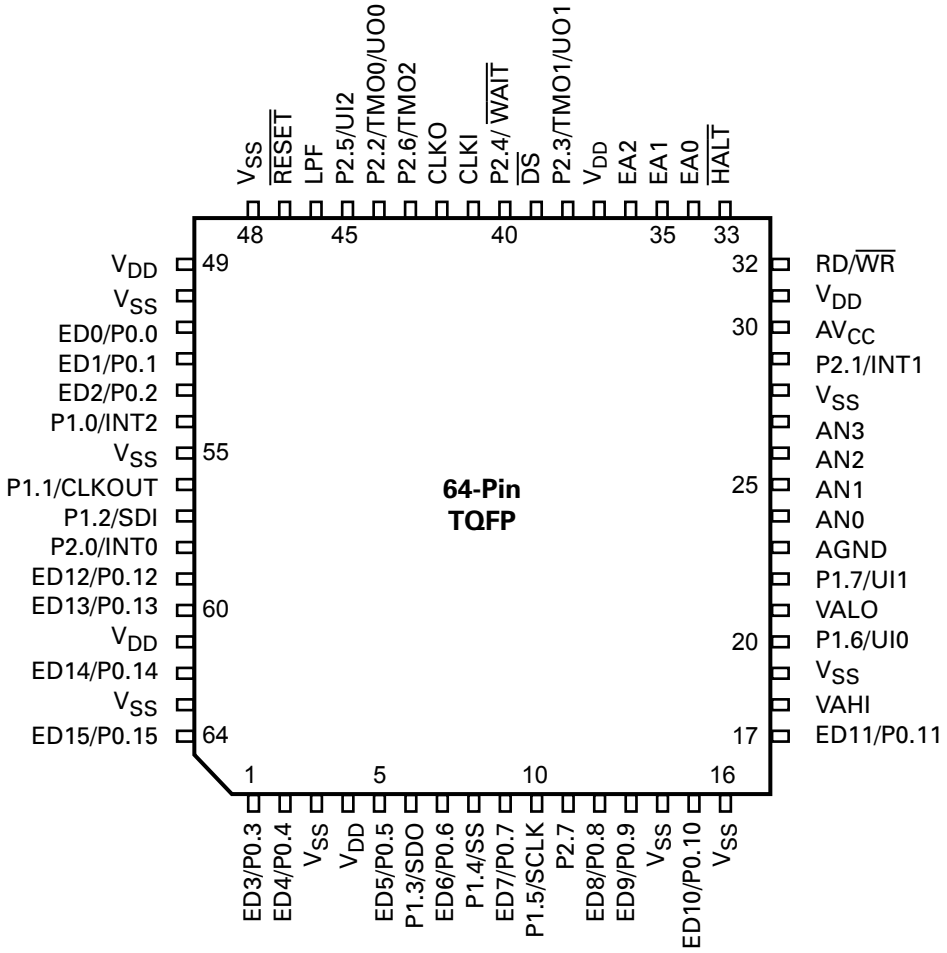


Figure 5. 64-Pin TQFP Z89323/373 Pin Configuration

Table 4. 68-Pin PLCC Z89323/373 Pin Description

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	P1.2/SDI	Port 1.2/Serial Input	Input/Output	35	AN0	A/D Input 0	Input
2	P2.0/INT0	Port 2.0/Interrupt 0	Input/Output	36	AN1	A/D Input 1	Input
3	ED12/P0.12	External Data Bus/Port0	Input/Output	37	AN2	A/D Input 2	Input
4	ED13/P0.13	External Data Bus/Port0	Input/Output	38	AN3	A/D Input 3	Input
5	V_{DD}	Power Supply		39	V_{SS}	Ground	
6	ED14/P0.14	External Data Bus/Port0	Input/Output	40	P2.1/INT1	Port 2.1/Interrupt 1	Input/Output
7	V_{SS}	Ground		41	AVCC	Analog Power	
8	ED15/P0.15	External Data Bus/Port0	Input/Output	42	V_{DD}	Power Supply	
9	NC	No Connection		43	RD/$\overline{WR}$	R/W External Bus	Output
10	NC	No Connection		44	$\overline{HALT}$	Halt Execution	Input
11	ED3/P0.3	External Data Bus/Port0	Input/Output	45	EA0	Ext Address 0	Output
12	ED4/P0.4	External Data Bus/Port0	Input/Output	46	EA1	Ext Address 1	Output
13	V_{SS}	Ground		47	EA2	Ext Address 2	Output
14	V_{DD}	Power Supply		48	NC	No Connection	
15	ED5/P0.5	External Data Bus/Port0	Input/Output	49	V_{DD}	Power Supply	
16	P1.3/SDO	Port 1.3/Serial Output	Input/Output	50	P2.3/TMO1	Port2.3/Timer Output 1	Input/Output
17	ED6/P0.6	External Data Bus/Port0	Input/Output	51	$\overline{DS}$	Ext Data Strobe	Output
18	P1.4/SS	Port 1.4/Slave Select	Input/Output	52	P2.4/$\overline{WAIT}$	Port 2.4/Wait for ED	Input/Output
19	ED7/P0.7	External Data Bus/Port0	Input/Output	53	CLKI	Clock/Crystal In	Input
20	P1.5/SCLK	Port 1.5/Serial Clock	Input/Output	54	CLKO	Clock/Crystal Out	Output
21	P2.7	Port 2.7	Input/Output	55	P2.6/TMO2	Port 2.6/Timer Output 2	Input/Output
22	ED8/P0.8	External Data Bus/Port0	Input/Output	56	P2.2/TMO0	Port 2.2/Timer Output 0	Input/Output
23	ED9/P0.9	External Data Bus/Port0	Input/Output	57	P2.5/UI2	Port 2.5/User Input 2	Input/Output
24	V_{SS}	Ground		58	LPF	PLL Low Pass Filter	Input
25	ED10/P0.10	External Data Bus/Port0	Input/Output	59	$\overline{RESET}$	Reset	Input
26	V_{SS}	Ground		60	V_{SS}	Ground	
27	ED11/P0.11	External Data Bus/Port0	Input/Output	61	V_{DD}	Power Supply	
28	V_{DD}	Power Supply		62	V_{SS}	Ground	
29	VAHI	Analog High Ref. Voltage	Input	63	ED0/P0.0	External Data Bus/Port0	Input/Output
30	V_{SS}	Ground		64	ED1/P0.1	External Data Bus/Port0	Input/Output
31	P1.6/UI0	Port 1.6/User Input 0	Input/Output	65	ED2/P0.2	External Data Bus/Port0	Input/Output
32	VALO	Analog Low Ref. Voltage	Input	66	P1.0/INT2	Port 1.0/Interrupt 2	Input/Output
33	P1.7/UI1	Port 1.7/User Input 1	Input/Output	67	V_{SS}	Ground	
34	AGND	Analog Ground		68	P1.1/CLKOUT	Port 1.1/Clock Output	Input/Output

AC ELECTRICAL CHARACTERISTICS

Table 8. V_{DD}= 5V ±10%, T_A = 0°C to +70°C for "S" Temperature Range T_A = –40°C to +85°C for "E" temperature range, unless otherwise noted

Symbol	Parameter	Min [ns]	Max [ns]
Clock			
TCY	CLKI Cycle Time for user-supplied clock	50	31250
CPWH	CLKI Pulse Width High	21	
CPWL	CLKI Pulse Width Low	21	
Tr	CLKI Rise Time for 20-MHz user-supplied clock		2
Tf	CLKI Fall Time for 20-MHz user-supplied clock		2
External Peripheral Bus			
EASET	EA Setup Time to $\overline{DS}$ Fall	10	
EAHOLD	EA Hold Time from $\overline{DS}$ Rise	4	
RWSET	Read/Write Setup Time to $\overline{DS}$ Fall	10	
RWHOLD	Read/Write Hold Time from $\overline{DS}$ Rise	0	
RDSET	Data Read Setup Time to $\overline{DS}$ Rise	15	
RDHOLD	Data Read Hold Time from $\overline{DS}$ Rise	0	
WRVALID	Data Write Valid Time from $\overline{DS}$ Fall		5
WRHOLD	Data Write Hold Time from $\overline{DS}$ Rise	2	
Reset			
RRISE	Reset Rise Time		20 TCY
RWIDTH	Reset Low Pulse Width	2 TCY	
Interrupt			
IWIDTH	Interrupt Pulse Width	1TCY	
Halt			
HWIDTH	Halt Low Pulse Width	3 TCY	
Wait State			
WLAT	Wait Latency Time from $\overline{DS}$ Fall		7
WDEA	Wait Deassert Setup Time to CLKOUT Rise	TBD	
SPI			
SDI–SCLK	Serial Data In to Serial Clock Setup Time	10	
SCLK–SDO	Serial Clock to Serial Data Out Valid	15	
SS–SCLK	Slave Select to Serial Clock Setup Time	1/2 SCLK Period	
SS–SDO	Slave Select to Serial Data Out Valid	15	
SCLK–SDI	Serial Clock to Serial Data In Hold Time	10	

TIMING DIAGRAMS

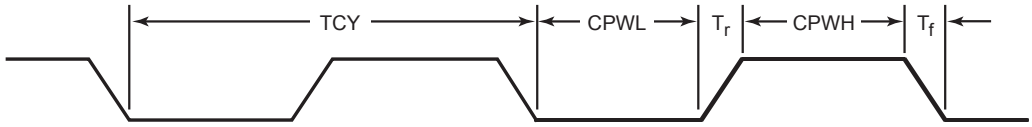


Figure 10. Clock Timing

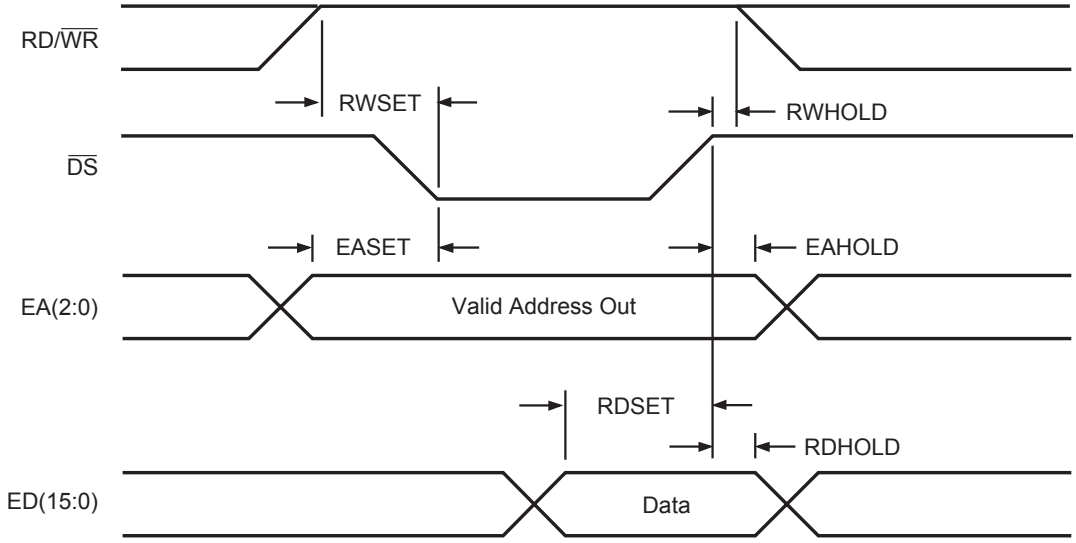


Figure 11. Read Timing

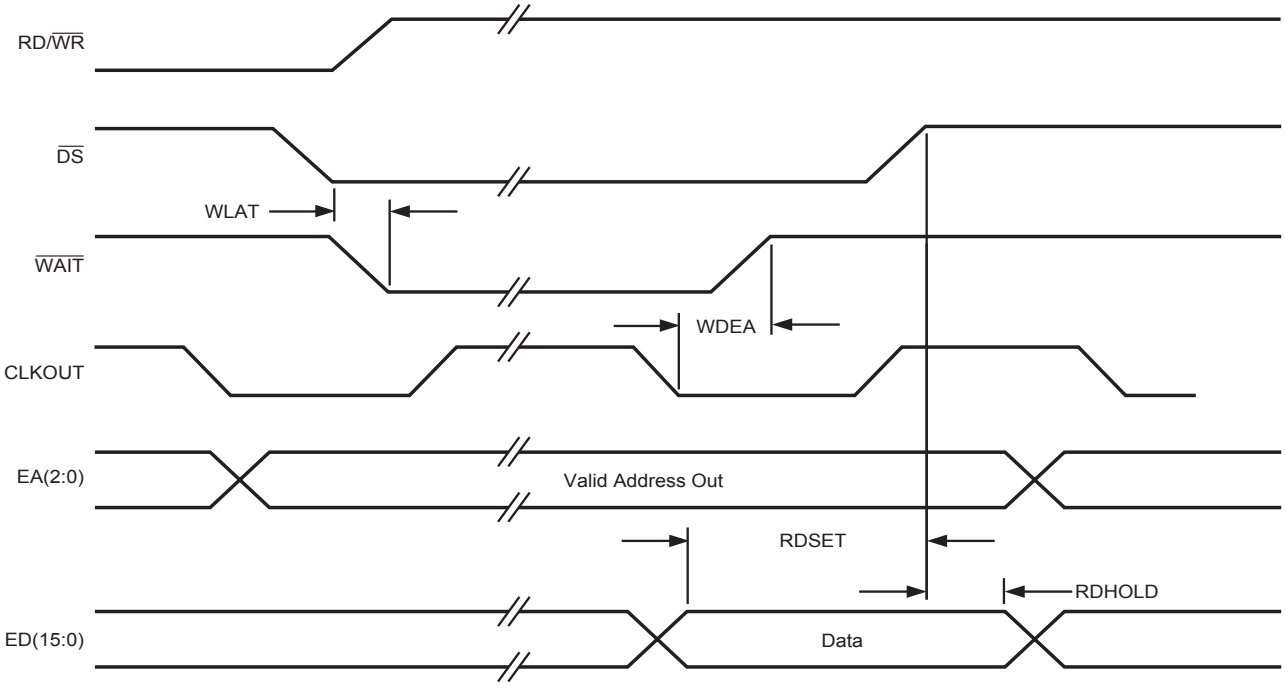
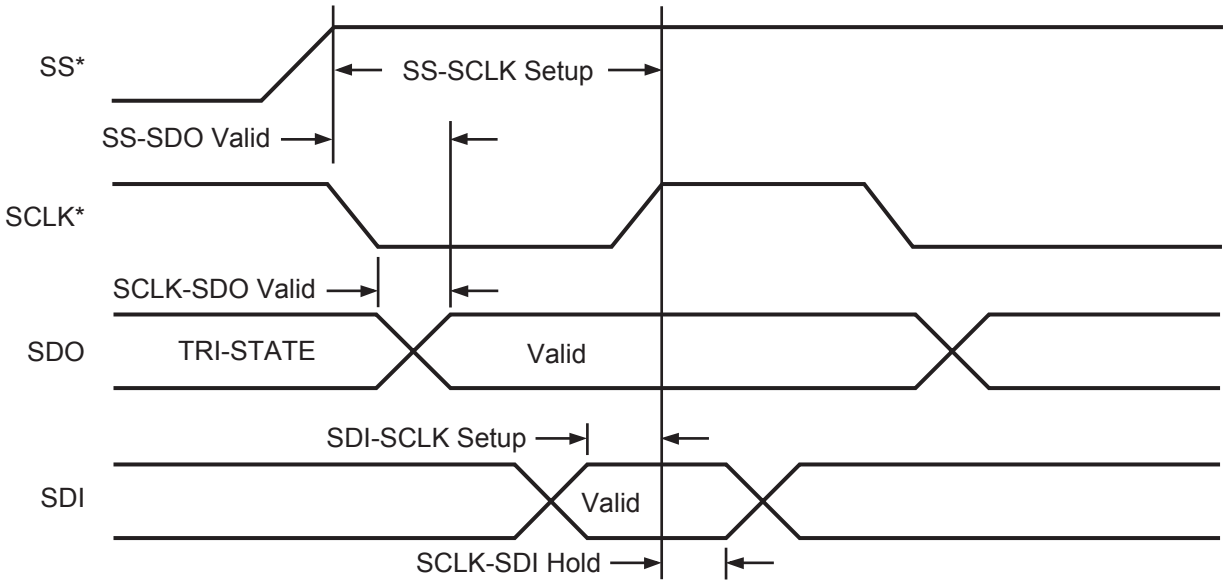


Figure 12. Read Timing Using $\overline{WAIT}$ Pin



*Notes: The polarity of SCLK and SS are programmable by the user. SS is used in Slave Mode only. This figure illustrates data transmission on the falling edge of SCLK, data reception on the rising edge of SCLK, with SS active Low (default).

Figure 15. SPI Timing (Master and Slave Modes)

REGISTERS

Both external and internal registers are accessed in one machine cycle. The external registers are used to access the on-chip peripherals when they are enabled.

The internal registers of the Z893X3 are defined below:

Register	Register Definition
X	Multiplier X Input, 16-bits
Y	Multiplier Y Input, 16-bits
P	Multiplier Output, 24-bits
A	Accumulator, 24-bits
Pn:b	Six Data RAM Pointers, 8-bits each
PC	Program Counter, 16-bits
SR	Status Register, 16-bits
EXT0	depends on Bank Select #, 16-bits
EXT1	depends on Bank Select #, 16-bits
EXT2	depends on Bank Select #, 16-bits
EXT3	depends on Bank Select #, 16-bits
EXT4	depends on Bank Select #, 16-bits
EXT5	depends on Bank Select #, 16-bits
EXT6	depends on Bank Select #, 16-bits
EXT7	Interrupt Status/Bank Select, 16-bits

X and **Y** are two 16-bit input registers for the multiplier. These registers can be utilized as temporary registers when the multiplier is not being used.

P holds the result of multiplications and is read-only.

A is a 24-bit Accumulator. The output of the ALU is sent to this register. When 16-bit data is transferred into this register, it is placed into the 16 MSBs and the least significant eight bits are set to zero. Only the upper 16 bits are transferred to the destination register when the Accumulator is selected as a source register in transfer instructions.

Pn:b are the pointer registers for accessing data RAM where n = 0, 1, or 2, and b = 0 or 1. They can be directly read or written. They point to locations in data RAM.

PC is the Program Counter. Any instruction which may modify this register requires two clock cycles.

SR is the status register. It contains the ALU status and processor control bits. The status register can always be read in its entirety. S15–S10 are set/reset by hardware and can only be read by software. S9–S0 control hardware operations and can be written by software.

Table 11. Status Register Bit Functions

SR Bit	Function	Read/Write
S15 (N)	ALU Negative	RO
S14 (OV)	ALU Overflow	RO
S13 (Z)	ALU Zero	RO
S12 (C)	Carry	RO
S11 (UI1)	User Input 1	RO
S10 (UI0)	User Input 0	RO
S9 (SH3)	MPY Output Arithmetically Shifted Right by Three Bits	R/W
S8 (OP)	Overflow Protection	R/W
S7 (IE)	Interrupt Enable	R/W
S6 ($\overline{UO1}$)	User Output 1	R/W
S5 ($\overline{UO0}$)	User Output 0	R/W
S4–S3	"Short Form Direct" bits	R/W
S2–S0 (RPL)	RAM Pointer Loop Size	R/W

Note: RO = read only, RW = read/write. The status register can always be read in its entirety.

S15–S12 are set/reset by the ALU after an operation.

S11–S10 are set/reset by the user input pins.

If **S9** is set and a multiply/shift option is used, the shifter shifts the result three bits right. This feature allows the data to be scaled and prevents overflows.

If **S8** is set, the hardware clamps at maximum positive or negative values instead of overflowing.

S7 enables interrupts.

S6–S5 are User Outputs. The complement of the value in the Status Register appears on bits 2 and 3 of Port2 if the User Outputs are enabled by writing a 1 to Bit 15 of Bank 15–EXT3, and Counter/Timer 0 and 1 are disabled.

S4–S3 are the two MSBs in the "short form direct" mode of addressing.

S2–S0 define the RAM pointer loop size as indicated in Table 12.

BANK/EXT REGISTER ASSIGNMENTS (Continued)

Interrupt Status/Bank Select Register—EXT7

Following is a description of EXT7. It contains both a Bank Select Field and Interrupt Status Bits.

Bank Select Field. The four LSBs of EXT7 denote which bank is selected as the current working bank.

Interrupt Status Bits. These bits can be read to identify which interrupts are pending. A "1" denotes interrupt pending, and a "0" denotes no interrupt. This ability to identify interrupts is particularly useful in polled interrupt operation or when servicing ISR2, which may come from several sources.

Note: Write "1" to a particular status bit to clear that bit. Before exiting an interrupt service routine, the relevant interrupt bit(s) should be cleared. To clear a bit efficiently:

- Load the value of EXT7 into a register or memory location
- Then load that value back into EXT7

Performing these steps clear all of the interrupts that were pending, but leave the Register Bank Select unchanged.

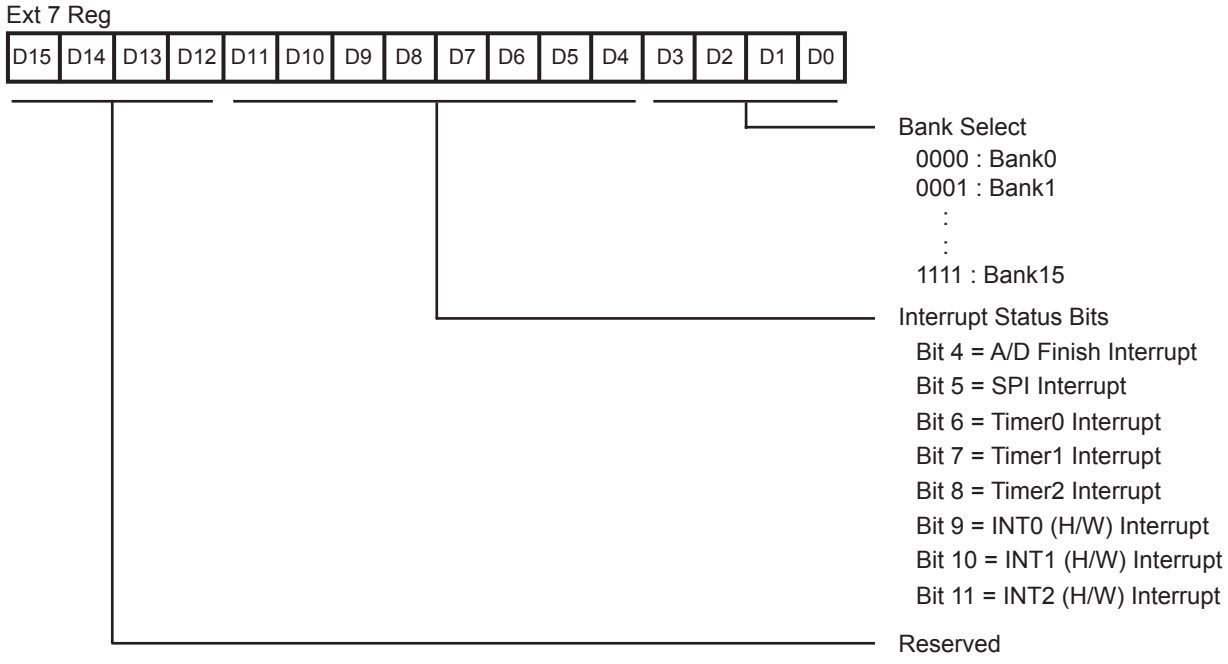


Figure 20. EXT7 Register

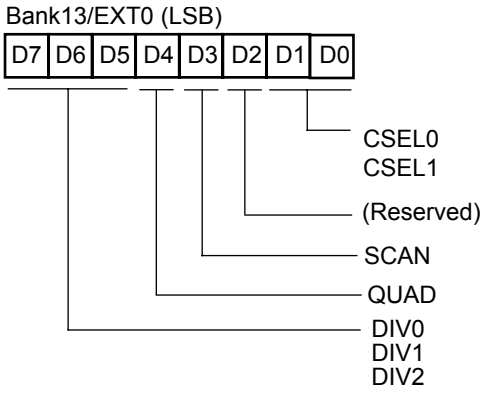


Figure 29. ADCTL Register (LSB)

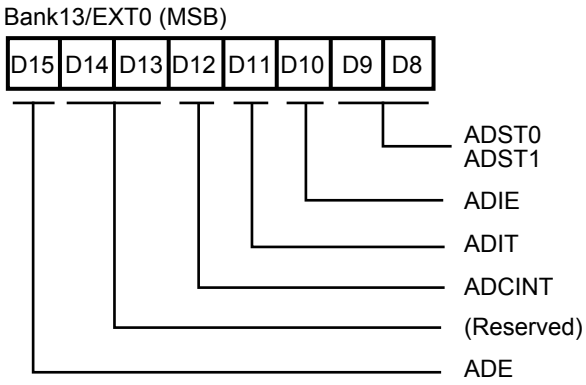


Figure 30. ADCTL Register (MSB)

Table 18. A/D Prescaler Values (Bits 7, 6, 5)

DIV2	DIV1	DIV0	A/D Prescaler (Crystal divided by)
0	0	0	8
0	0	1	16
0	1	0	24
0	1	1	32
1	0	0	40
1	0	1	48
1	1	0	56
1	1	1	64

Table 19. Operating Modes (Bits 4, 3)

QUAD	SCAN	Option
0	0	Convert selected channel 4 times, then stop
0	1	Convert selected channel, then stop.
1	0	Convert 4 channels, then stop.
1	1	Convert 4 channels continuously.

Table 20. Channel Select (Bits 1, 0)

CSEL1	CSEL0	Channel
0	0	AN0
0	1	AN1
1	0	AN2
1	1	AN3

ADE (Bit 15). A "0" disables any A/D conversions or accessing any A/D registers, except writing to the ADE bit. A "1" enables all A/D accesses.

Reserved (Bits 14, 13). Reserved for future use.

ADCINT (Bit 12). The A/D interrupt bit is read-only. The ADCINT will reset every time this register is written.

ADIT (Bit 11). Selects when to set the A/D interrupt if interrupts are enabled (ADIE=1). A value of "0" sets the interrupt after the first A/D conversion is complete. A value of "1" sets the interrupt after the fourth A/D conversion is complete.

ADIE (Bit 10). A/D Interrupt Enable. A value of "0" disables the A/D Interrupt. A value of "1" enables the A/D Interrupt.

Table 21. START (Bits 9, 8)

ADST1	ADST0	Option
0	0	Conversion starts when this register is written.
0	1	Conversion starts on INT1 per Interrupt Allocation Register
1	0	Conversion starts on C/T2 time-out.
1	1	Conversion starts on C/T0 time-out.

There are four A/D result registers. See the EXT Register Assignments for their location in the different banks.

PERIPHERALS (Continued)

Counter/Timers (C/T0 and C/T1)

The Z893x3 features two 16-bit Counter/Timers (C/T) that can be independently configured to operate in various modes. Each is implemented as a 16-bit Load Register and a 16-bit down counter. Either C/T input can be selected from UI0 or UI1. Either C/T output can be directed to TMO0 or TMO1. The C/T clock is a scaled version of the system clock. Each C/T features an 8-bit prescaler. The clock rates of the two C/T are independent of each other. The C/Ts can be programmed to recognize clock events on the rising edge, the falling edge, or both rising and falling edges of the input signal. Outputs on TMO0 or TMO1 can be programmed to occur with either polarity.

If either C/T is enabled and an output pin TMO0 or TMO1 is selected, and at the same time User Outputs are enabled, the C/T takes precedence, and Status Register bits 5 or 6 do not affect the state of the selected pin.

C/T Modes of Operation:

MODE 0—Square Wave Output. The C/T is configured to generate a continuous square wave of 50% duty cycle. Writing a new value to the TMLR Register takes effect at the end of the current cycle, unless TMR is written.

MODE 1—Retriggerable One-Shot. The C/T is configured to generate a single pulse of programmable duration. The pulse may be either logic High or logic Low. Retriggering the one-shot before the end of the pulse causes it to retrigger for a new duration.

MODE 2—8-Bit PWM. The C/T is configured to generate a pulse-width modulated waveform. The duty cycle ranges from 0–100% (0/256 to 255/256; 8-bits) of a cycle in steps of 1/256 of a cycle. The asserted state of the waveform may be either logic High or logic Low. Writing a new pulse-width value to the TMLR Register takes effect at the end of current cycle, unless TMR is written.

MODE 3—16-Bit PWM. The C/T is configured to generate a pulse-width modulated waveform. The duty cycle ranges from 0–100% (0/65,536 to 65,535/65,536; 16-bits) of a cycle in steps of 1/65,536 of a cycle. The asserted state of the waveform may be either logic High or logic Low. Writing a new pulse-width value to the TMLR Register takes effect at the end of current cycle, unless TMR is written.

MODE 4—Finite Pulse String Generator. The C/T is configured to generate 1 to 65,535 pulses. The output pulses are actually from the Timer Clock Prescaler divided by 2 (TMCLK). They are gated to the output until the Timer Down-Counter underflows.

MODE 5—Externally Clocked One-Shot. The C/T is configured to generate an output pulse. The pulse may be either logic High or logic Low. It is deasserted when a programmable number of input events (up to 65,535) occur on the input pin, UI0 or UI1.

MODE 6—Software Watch-Dog Timer. The C/T is configured to generate a Hardware Reset on time-out, unless retriggered by software.

MODE 7—Hardware Watch-Dog Timer. The C/T is configured to generate a Hardware Reset on time-out unless retriggered by an event on the input pin, UI0 or UI1.

MODE 8—Pulse Stopwatch. The C/T is configured to measure the time during which its input is asserted.

MODE 9—Edge-to-Edge Stopwatch. The C/T is configured to measure the period from one rising (falling) edge to the next rising (falling) edge on the input.

MODE 10—Edge Counter. The C/T is configured to count a number of input edges (up to 65,535). Input edges may be selected as rising or falling or both.

MODE 11—Gated Edge Counter. The C/T is configured to count the number of input edges (up to 65,535) in a time window set by the second timer. Edges are counted until the second timer underflows. Input edges may be selected as rising, falling, or both.

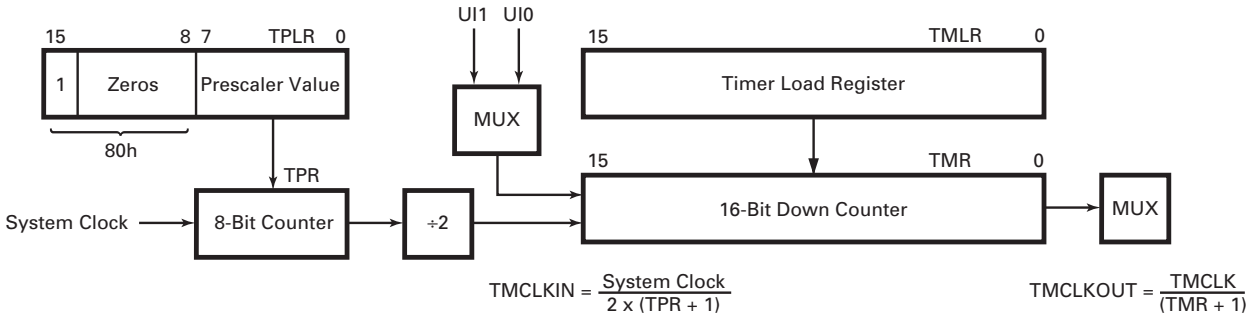


Figure 31. Counter/Timer 0 and 1 Block Diagram

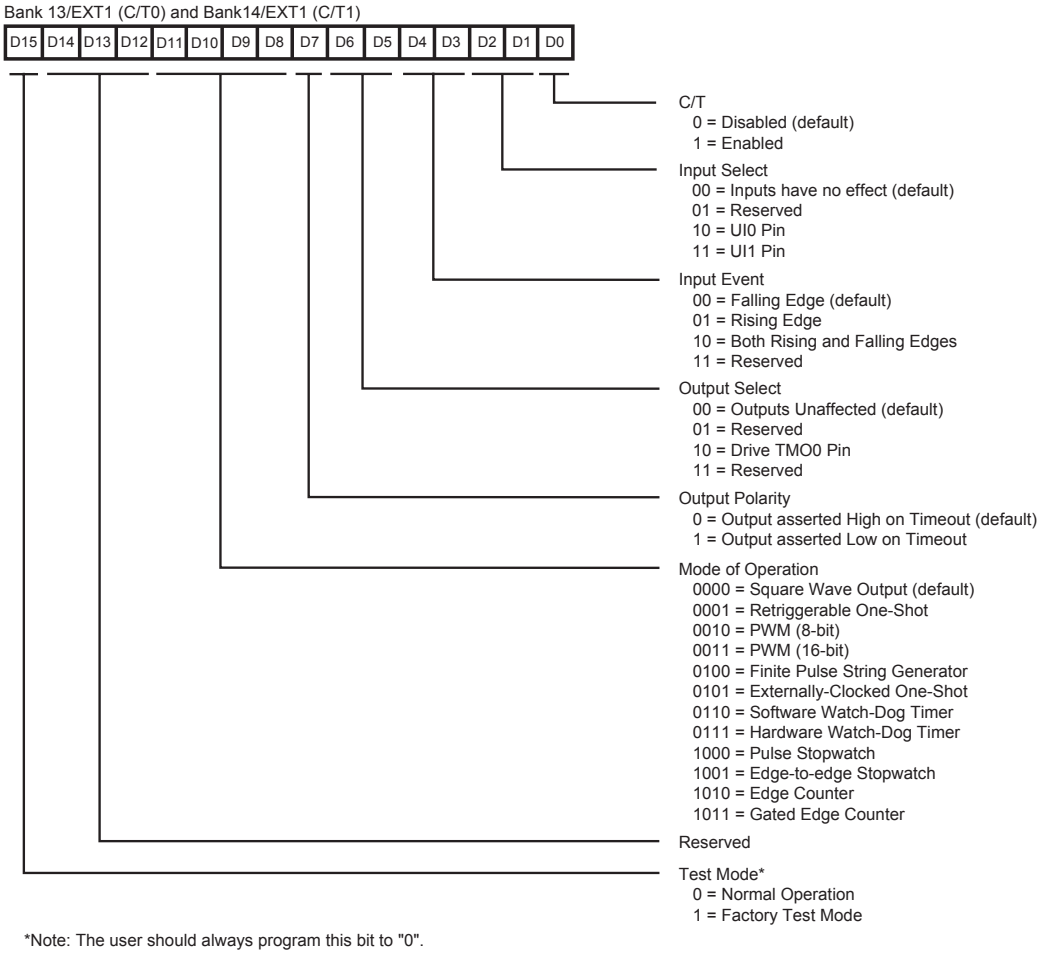


Figure 32. C/T0 and C/T1 Control Register

C/T Registers

Each C/T contains a set of five 16-bit Registers. Bank13 is used to access the registers for C/T0 and Bank14 is for the C/T1 registers. All accesses to C/T Registers occur with zero wait states.

Counter/Timer Control Register (Bank13,14/EXT1). The C/T Control register enables/disables the C/T, selects input and output options, and the mode of operation.

TMLR—Load Register (Bank13,14/EXT2). The 16-bit TMLR register holds the value that is loaded into TMR when TMR underflows.

TMR—Counter Register (Bank13,14/EXT3). TMR is a 16-bit down counter that holds the current C/T value. It can be read like any other ordinary register. However, writing to TMR is different than writing to an ordinary register. A write to TMR causes the contents of TMLR to be written into TMR, causing the C/T to be retriggered.

TPLR—Prescaler Load Register (Bank13,14/EXT4). The 16-bit TPLR register holds the prescaler load value in its lower 8 bits. Bit 15 must be written with a “1”, and bits 14–8 must be written with “0’s”.

Note: If the C/T interrupt is being used, this register must be re-written at the end of the interrupt service routine in order to enable the next interrupt. The number of clock cycles from the beginning of the interrupt service routine to the write must exceed the prescaler load value.

PERIPHERALS (Continued)

TPR—Prescaler Register (Bank13,14/EXT5). TPR is an 8-bit down counter that holds the current Prescaler Count Value. It can be read like any other ordinary register. However, writing to TPR is different than writing to an ordinary register. A write to TPR causes the lower 8-bit contents of TPLR to be written into TPR, causing the Prescaler to be retriggered.

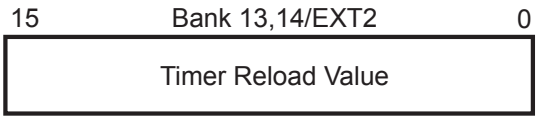


Figure 33. TMLR—Load Register

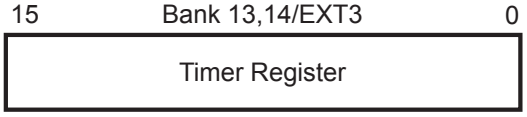


Figure 34. TMR—Counter Register

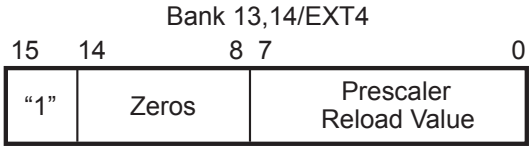


Figure 35. TPLR—Prescaler Load Register

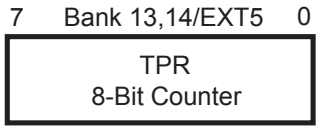


Figure 36. TPR—Prescaler Register

Prescaler Operation

The Prescaler section comprises TPLR and TPR, followed by a divide-by-two flip-flop. This operation generates a 50 percent duty cycle output, TMCLKIN. TPR's input clock is the system clock. The maximum prescaler output frequency is 1/2 the system clock frequency.

After TPR is loaded, it decrements at the system clock frequency and generates an output to the divide-by-two flip-flop. When the count reaches 0, the TPR counter is reloaded from the lower 8 bits of TPLR Register.

Two other events cause a reloading of the TPR counter:

1. Writing to TPR
2. Reloading TMR, which happens when TMR underflows, or when TMR is written.

Note: For C/T Modes 8–11, the external input signal on UI0 or UI1 is synchronized with TMCLKIN before being applied to TMR. The external input signal frequency must be no higher than 1/2 of the TMCLKIN frequency.

GENERAL-PURPOSE COUNTER/TIMER (C/T2) (Continued)

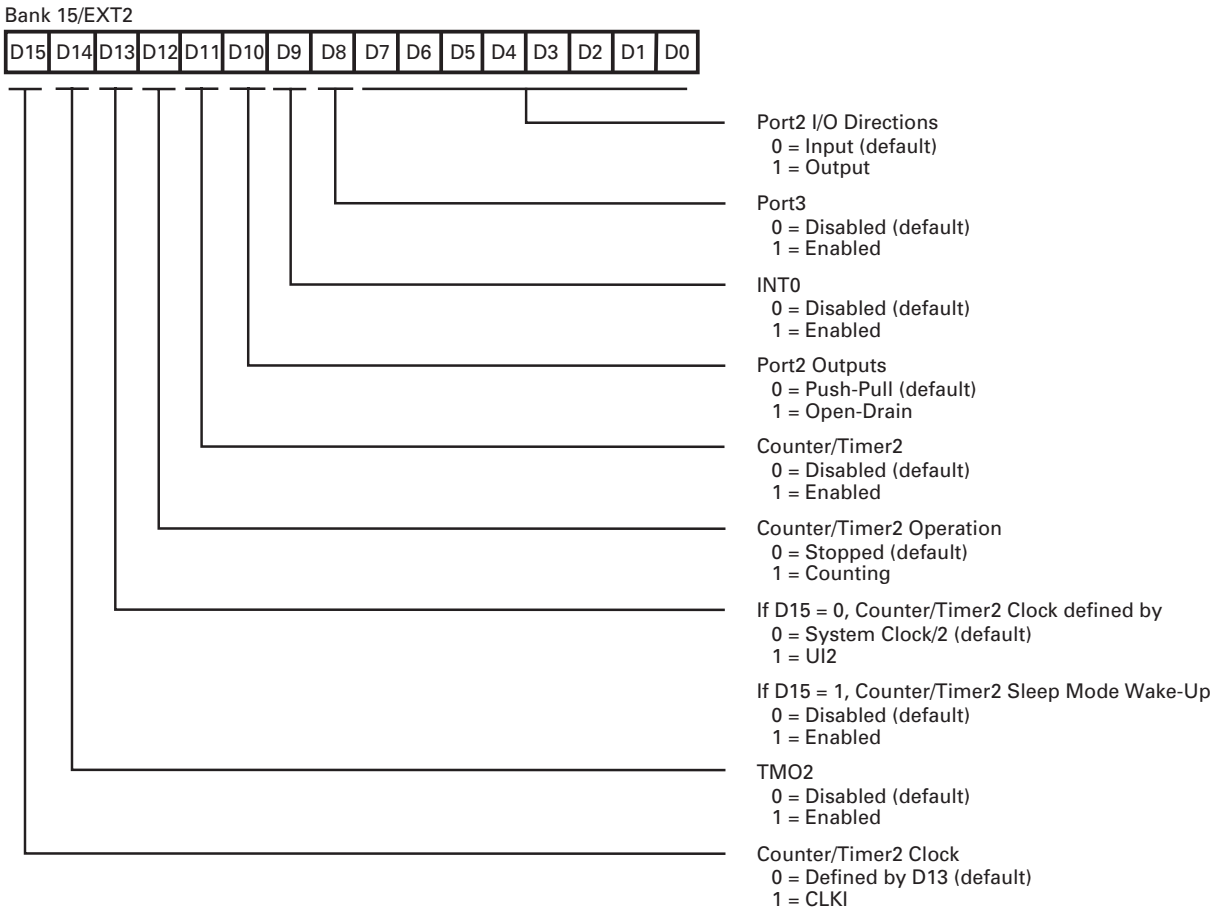


Figure 38. Counter/Timer2 Control Register

SERIAL PERIPHERAL INTERFACE

The Z893x3 incorporates a Serial Peripheral Interface (SPI) for communication with other microcontrollers and peripherals. The SPI can be operated either as the system Master, or as a system Slave. The SPI consists of three registers: the SPI Control Register (Bank15/EXT4), the SPI Receive/Buffer Register (RxBUF), and the SPI Shift Register.

SPI Data Access

Receive operations are double buffered. Bank0/EXT3 accesses both RxBUF for read (receive) operations, and the SPI shift register for write (transmit) operations.

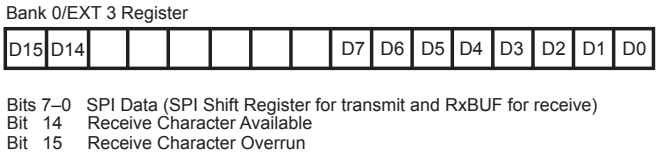


Figure 39. SPI Data Access

SPI Control Register

This register is the Low byte of Bank15/EXT4. It is a read/write register that controls Master/Slave selection, SS polarity, clock source and phase selection, and indicates byte available and data overrun conditions. The control register is multifunction depending on Master/Slave mode selection.

In Master mode, Bit 6 defines the SPI clock source. A “1” selects SCLK = C/T0 output, and a “0” selects SCLK = System Clock divided down by 2, 4, 8, or 16, as determined by bits 1 and 2.

In Slave Mode, bit 1 is the Receive Byte Overrun flag. This flag can be cleared by writing a “0” to this bit. Bit 2 is the SDO output enable.A “0” tristates SDO, a “1” enables data output on SDO. Bit 4 signals that a receive byte is available in the RxBUF Register. If the associated interrupt enable bit is enabled, an interrupt is generated.

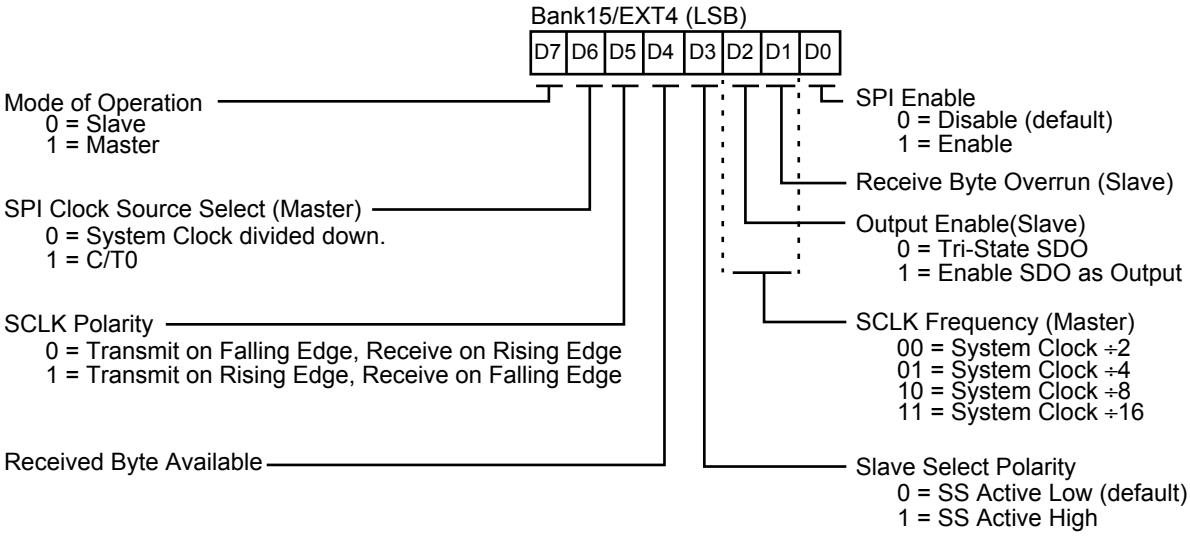


Figure 40. SPI Control Register

Master Mode Operation

The DSP must first activate the target slave’s select pin through an I/O port. Loading data into the SPI Shift Register initiates the transfer. Data is transferred out the SDO pin to the slave one data bit per SCLK cycle. The MSB is shifted out first. At the conclusion of the transfer, the Receive Byte Available flag is set, and if enabled, an SPI interrupt is generated. The Receive Byte Available flag is reset when RxBUF is read.

SYSTEM CLOCK GENERATOR

The System Clock can be generated from an external clock signal, or from the internal crystal oscillator. For the latter case, a 32-kHz crystal is used in conjunction with the internal crystal oscillator. The system clock generator includes a Phase-Locked Loop (PLL) circuit to derive a high-frequency System Clock from the low-frequency crystal oscillator. The benefits of using a low-frequency crystal are lower system cost, lower power consumption and lower EMI.

The Z893x3 supports several low-power clock modes to optimize power consumption. Total power consumption depends on System Clock frequency, and which oscillators and peripherals are enabled.

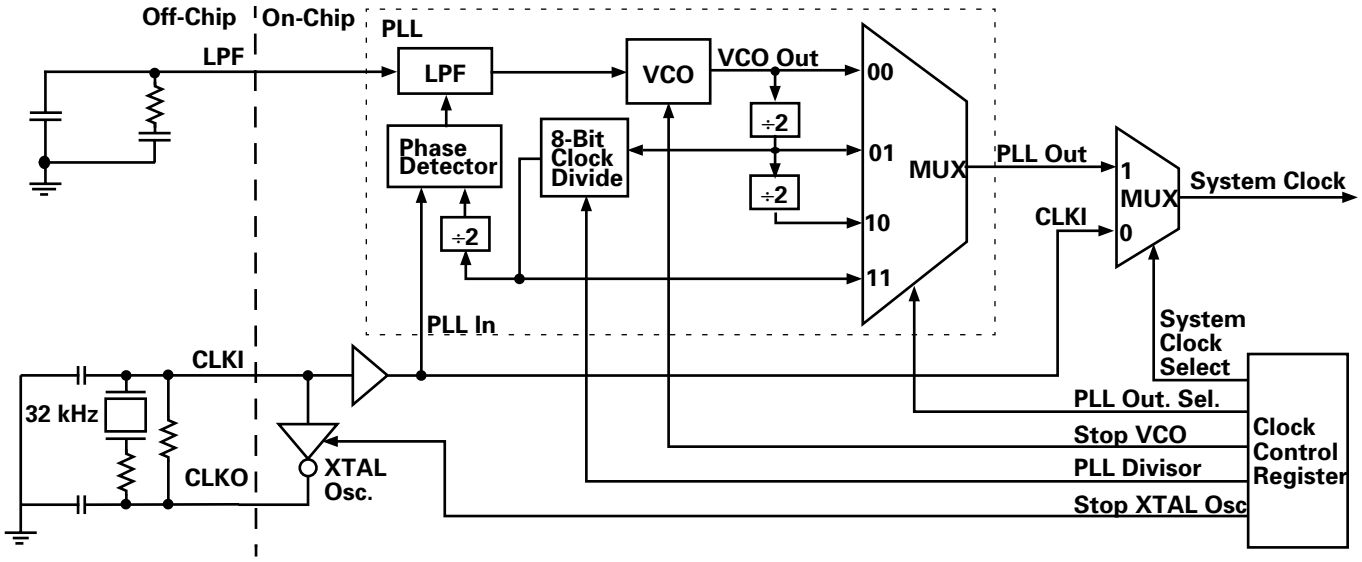


Figure 42. System Clock Generator

Modes of Operation

The various modes of clock operation are selected by writing to the appropriate bits and fields of the Clock Control Register, Bank15/EXT5. The mode of operation can be switched dynamically during program execution.

Power-up and Reset (Default)

At power-up, and following a reset or Sleep Mode Recovery, System Clock Select = 0, therefore system clock = CLKI. The XTAL Oscillator is running, so CLKI may be provided by a crystal, as depicted, or by an external clock (not shown). The VCO is running to minimize the time required to switch the system clock to PLL Out.

External Clock Direct

In this mode, an external clock on CLKI provides the System Clock. CLKO is not connected. System Clock Select = 0. The PLL is not used. The XTAL oscillator and VCO are both stopped to reduce power consumption.

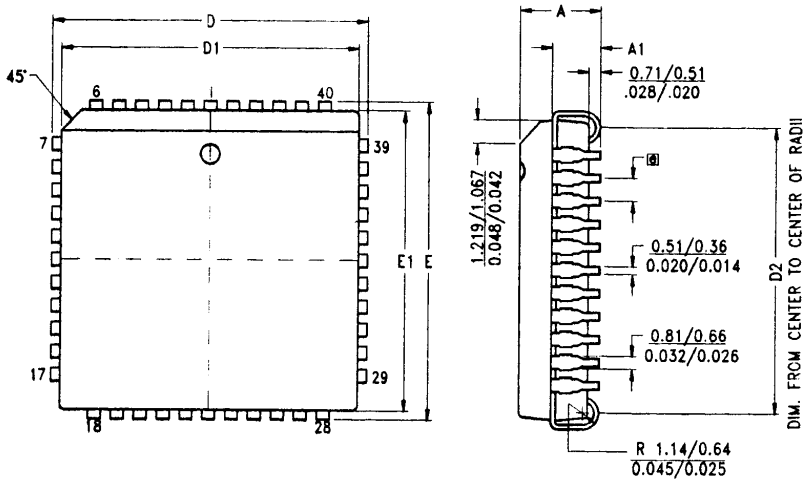
Crystal Oscillator DIrect

In this mode of operation, the XTAL Oscillator is running, and an external crystal provides a 32-kHz (typical) clock at CLKI. System Clock Select = 0, so the System Clock is the frequency at CLKI (32 kHz). This mode requires less power than running at a high-frequency clock rate. The VCO may be stopped to conserve even more power, or left running for rapid switching (wake up) to a high-frequency PLL generated clock. Whenever the PLL circuit is enabled, Stop VCO = 0, and a software delay of 10 ms must be observed before switching System Clock from CLKI to PLL Out. As a result, the PLL has time to stabilize.

PLL Clock

An external 32-kHz crystal, together with the on-chip XTAL oscillator, provides the PLL input. The VCO generates the System Clock. A low-pass filter must be connected to LPF as depicted. The XTAL oscillator and VCO are both running, and System Clock = PLL Out (System Clock Select = 1). The frequency generated by the PLL is deter-

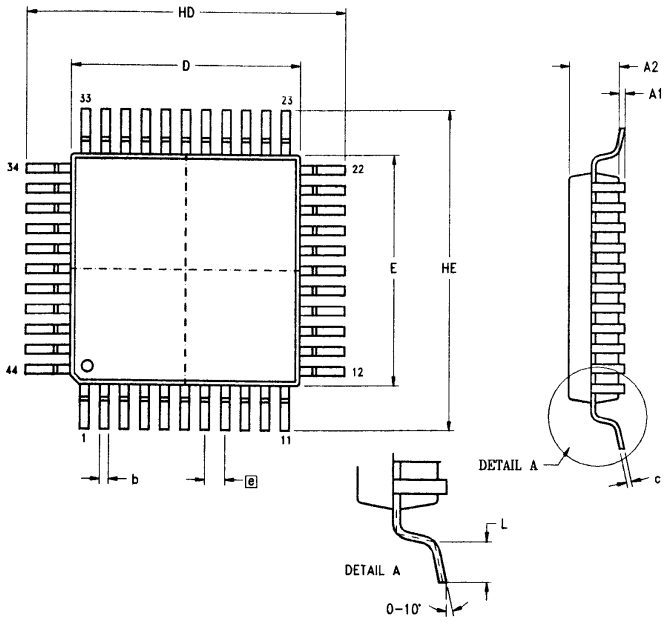
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 TYP		0.050 TYP	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM / INCH

Figure 44. 44-Pin PLCC Package Diagram

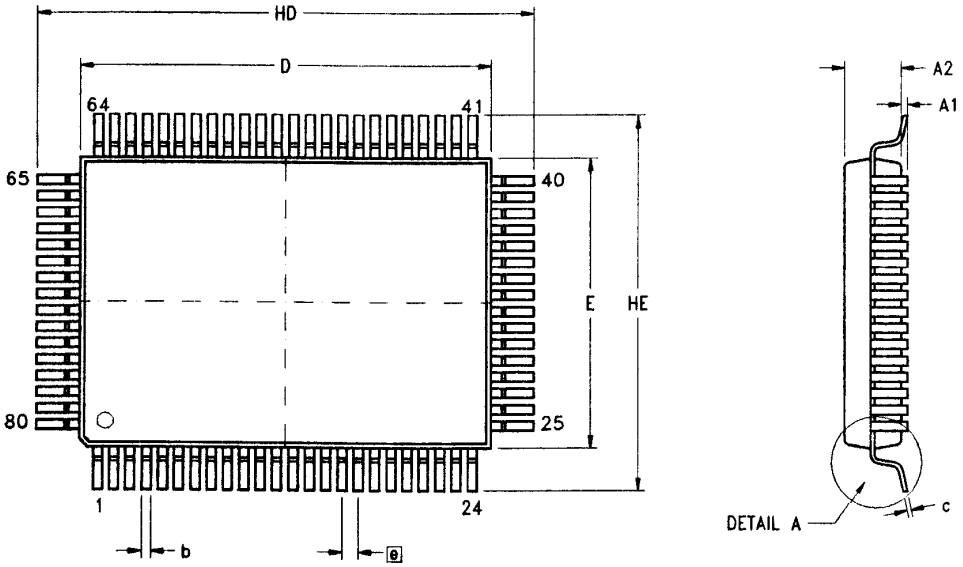


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 TYP		.0315 TYP	
L	0.60	1.20	.024	.047

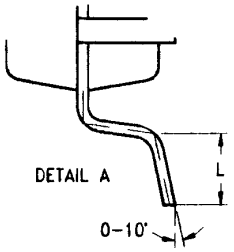
NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 / .004"

Figure 45. 44-Pin PQFP Package Diagram

PACKAGE INFORMATION (Continued)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.10	0.30	.004	.012
A2	2.60	2.80	.102	.110
b	0.30	0.45	.012	.018
c	0.13	0.20	.005	.008
HD	23.70	24.15	.933	.951
D	19.90	20.10	.783	.791
HE	17.70	18.15	.697	.715
E	13.90	14.10	.547	.555
e	0.80 TYP		.0315 TYP	
L	0.70	1.10	.028	.043



NOTES:
1. CONTROLLING DIMENSIONS: MILLIMETER
2. MAX COPLANARITY: .10 / .004

Figure 48. 80-Pin PQFP Package Diagram