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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	SPI, 3-Wire Serial
Clock Rate	20MHz
Non-Volatile Memory	OTP (16kB)
On-Chip RAM	1kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-TQFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8937320asc00tr

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GENERAL DESCRIPTION (Continued)

OTP version of the Z89223/323, is ideal for prototypes and early production builds.

Throughout this specification, references to the Z893x3 device apply equally to the Z89223/273/323/373, unless otherwise specified.

Notes: All signals with an overline are active Low. For example, in RD/WR, RD is active High and WR is active Low. For I/O ports, P1.3 denotes Port1 bit 3. Pins called NC are "No Connection"—they do not connect any power, grounds, or signals.

Power connections follow conventional descriptions:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

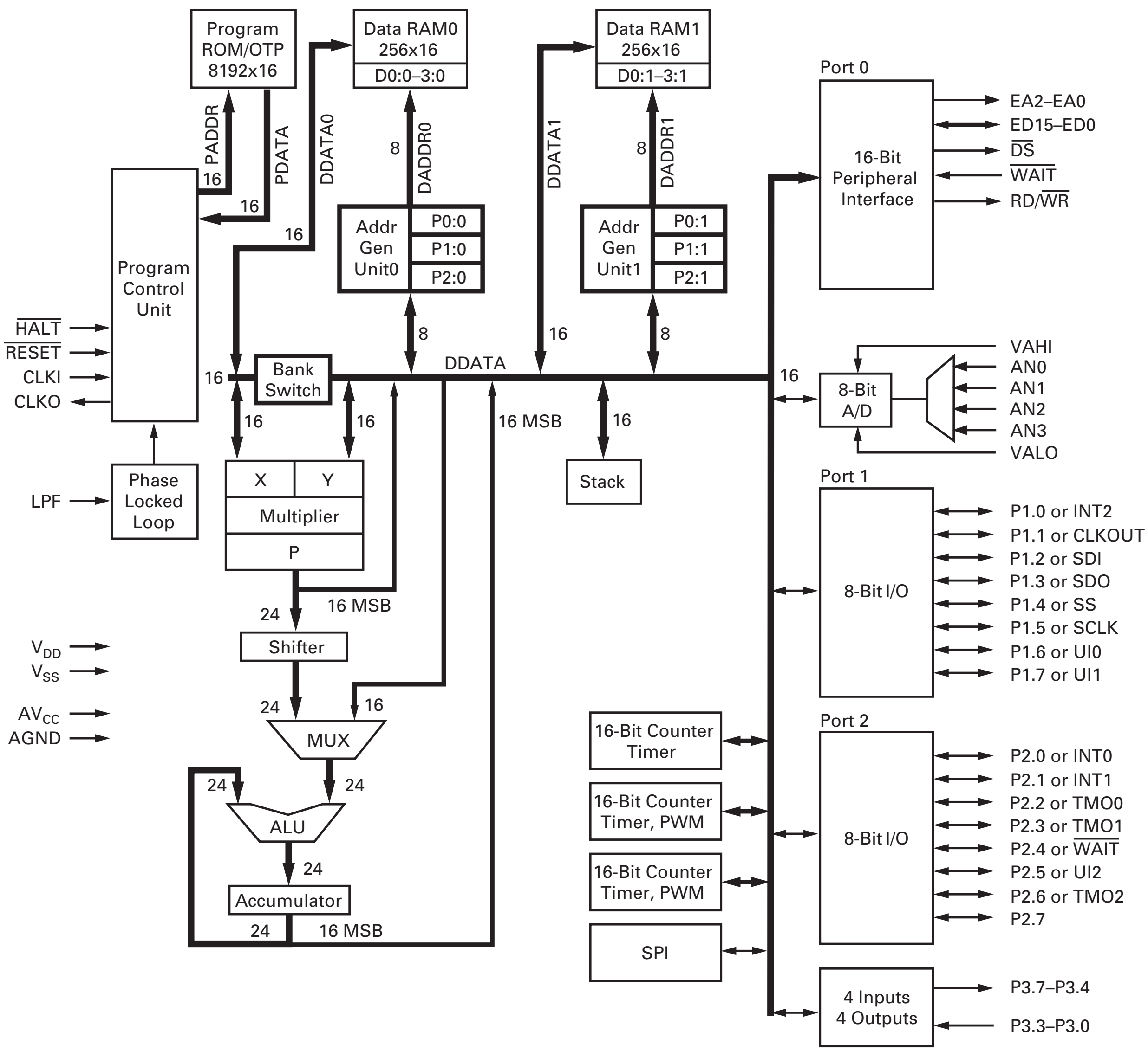

Figure 1. Z892X3/3x3 Functional Block Diagram

PIN FUNCTIONS

EA2–EA0. External Address Bus (output, latched). These pins provide the External Register Address. This address bus is driven during both internal and external accesses. One of up to seven user-defined external registers is selected by the processor for reads or writes. EXT7 is always reserved for use by the processor.

ED15–ED0. External Data Bus (input/output). These pins are the data bus for the user-defined external registers, and are shared by Port0. These pins are normally tristated, except when these registers are specified as destination registers in a write instruction to an external peripheral, or when Port0 is enabled for output. This bus uses the control signals RD/$\overline{\text{WR}}$, $\overline{\text{DS}}$, and $\overline{\text{WAIT}}$, and address pins EA2–EA0.

$\overline{\text{DS}}$. Data Strobe (output). This pin provides the data strobe signal for the ED Bus. $\overline{\text{DS}}$ is active for transfers to/from external peripherals only.

RD/$\overline{\text{WR}}$. Read/$\overline{\text{Write}}$ Select (output). This pin controls the data direction signal for the External Data Bus. Data is available from the processor on ED15–ED0 when this signal and $\overline{\text{DS}}$ are both Low.

$\overline{\text{WAIT}}$. Wait State (input). This pin is sampled at the rising edge of the clock with appropriate setup and hold times. A single wait-state can be generated internally by setting the appropriate bits in the wait state register. The user must drive this line if multiple wait states are required. This pin is shared with Port2.

CLKI. Clock (input). This pin is the clock circuit input. It can be driven by a signal or connected to a 32 KHz crystal.

CLKO. Clock (output). This pin is the clock circuit output. It is used for operation with a 32 KHz crystal and the PLL to generate the system clock.

$\overline{\text{HALT}}$. Halt State (input). This pin stops program execution. The processor continuously executes NOPs and the program counter remains constant while this pin is held Low. This pin offers an internal pull-up.

$\overline{\text{RESET}}$. Reset (input). This pin resets the processor. It pushes the contents of the Program Counter (PC) onto the stack and then fetches a new PC value from program memory address 0FFCH after the $\overline{\text{RESET}}$ signal is released. The Status register is set to all zeros. At power-up RAM and other registers are undefined, however, they are left unchanged with subsequent resets. $\overline{\text{RESET}}$ can be asserted asynchronously.

AN0–AN3. Analog Inputs (input). These are the analog input pins. The analog input signal should be between VALO and VAHI for accurate conversions.

VAHI. Analog High Reference Voltage (input). This pin provides the reference for the full scale voltage of the analog input signals.

VALO. Analog Low Reference Voltage (input). This pin provides the reference for the zero voltage of the analog input signals.

AV_{CC}–AGND. Filtered Analog Power and Ground must be provided on separate pins to reduce digital noise in the analog circuits.

Multifunction Pins. The Z89223/273/323/373 DSP family offers a user-configurable I/O structure, which means that most of the I/O pins offer dual functions. The function, direction (input or output), and for output, the characteristics (push-pull or open drain) are all under user-control, by programming the configuration registers appropriately as described in the I/O Ports section. The following share I/O Port pins:

INT0–INT2. External Interrupts (input, edge-triggered). These pins provide three of the eight interrupt sources to the Interrupt Controller. Each is programmable to be rising-edge or falling-edge triggered. The other five interrupt sources are from the on-chip peripherals.

CLKOUT. System Clock (output). This pin provides access to the internal processor clock.

SDI. Serial Data In (input). This pin is the SPI serial data input.

SDO. Serial Data Out (output). This pin is the SPI serial data output.

SS. Slave Select (input). This pin is used in SPI Slave Mode only. SS advises the SPI that it is the target of a serial transfer from an external Master.

SCLK. SPI Clock (output/input). This pin is an output in Master mode and an input in Slave mode.

UI0, UI1. User inputs (input). These general-purpose input pins are directly tested by the conditional branch instructions. They can also be read as bits in the status register. These are asynchronous input signals that require no special clock synchronization. Counter/Timer0 and Counter/Timer1 may use either of these pins as input.

UI2. User Input (input). This pin is the input to Counter/Timer 2.

TMO0/UO0. Counter/Timer Output or User Output 0 (output). Counter/Timer 0 and Counter/Timer 1 can be programmed to provide output on this pin. When User Outputs are enabled, and the Counter/Timer is disabled, this pin provides the complement of Status Register bit 5.

PIN CONFIGURATIONS

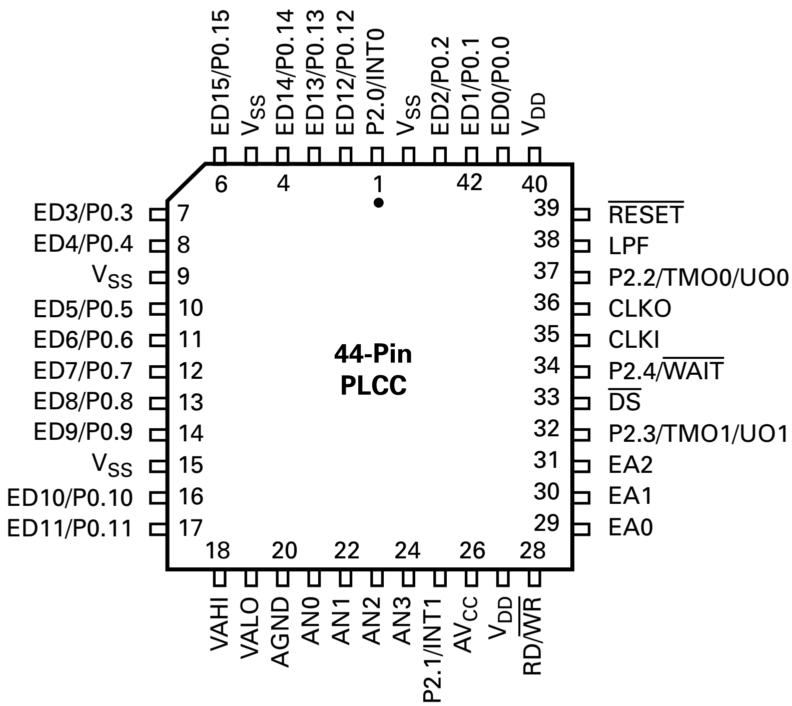

Figure 3. 44-Pin PLCC Z89223/273 Pin Configuration

Table 1. 44-Pin PLCC Z89223/273 Pin Description

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	P2.0/INT0	Port 2.0/Interrupt 0	Input/Output	23	AN2	A/D Input 2	Input
2	ED12/P0.12	External Data Bus/Port0	Input/Output	24	AN3	A/D Input 3	Input
3	ED13/P0.13	External Data Bus/Port0	Input/Output	25	P2.1/INT1	Port 2.1/Interrupt 1	Input/Output
4	ED14/P0.14	External Data Bus/Port0	Input/Output	26	AV_{CC}	Analog Power	
5	V_{SS}	Ground		27	V_{DD}	Power Supply	
6	ED15/P0.15	External Data Bus/Port0	Input/Output	28	RD/$\overline{\text{WR}}$	R/W External Bus	Output
7	ED3/P0.3	External Data Bus/Port0	Input/Output	29	EA0	Ext Address 0	Output
8	ED4/P0.4	External Data Bus/Port0	Input/Output	30	EA1	Ext Address 1	Output
9	V_{SS}	Ground		31	EA2	Ext Address 2	Output
10	ED5/P0.5	External Data Bus/Port0	Input/Output	32	P2.3/TMO1	Port 2.3/Timer Output 1	Input/Output
11	ED6/P0.6	External Data Bus/Port0	Input/Output	33	$\overline{\text{DS}}$	Ext Data Strobe	Output
12	ED7/P0.7	External Data Bus/Port0	Input/Output	34	P2.4/$\overline{\text{WAIT}}$	Port 2.4/Wait for ED	Input/Output
13	ED8/P0.8	External Data Bus/Port0	Input/Output	35	CLKI	Clock/Crystal In	Input
14	ED9/P0.9	External Data Bus/Port0	Input/Output	36	CLKO	Clock/Crystal Out	Output
15	V_{SS}	Ground		37	P2.2/TMO0	Port 2.2/Timer Output 0	Input/Output
16	ED10/P0.10	External Data Bus/Port0	Input/Output	38	LPF	PLL Low Pass Filter	Input
17	ED11/P0.11	External Data Bus/Port0	Input/Output	39	$\overline{\text{RESET}}$	Reset	Input
18	VAHI	Analog High Ref. Voltage	Input	40	V_{DD}	Power	
19	VALO	Analog Low Ref. Voltage	Input	41	ED0/P0.0	External Data Bus/Port0	Input/Output
20	AGND	Analog Ground		42	ED1/P0.1	External Data Bus/Port0	Input/Output
21	AN0	A/D Input 0	Input	43	ED2/P0.2	External Data Bus/Port0	Input/Output
22	AN1	A/D Input 1	Input	44	V_{SS}	Ground	

Table 2. 44-Pin PQFP Z89223/273 Pin Description

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	ED3/P0.3	External Data Bus/Port0	Input/Output	23	EA0	Ext Address 0	Output
2	ED4/P0.4	External Data Bus/Port0	Input/Output	24	EA1	Ext Address 1	Output
3	V_{SS}	Ground		25	EA2	Ext Address 2	Output
4	ED5/P0.5	External Data Bus/Port0	Input/Output	26	P2.3/TMO1	Port 2.3/Timer Output 1	Input/Output
5	ED6/P0.6	External Data Bus/Port0	Input/Output	27	$\overline{DS}$	Ext Data Strobe	Output
6	ED7/P0.7	External Data Bus/Port0	Input/Output	28	P2.4/$\overline{WAIT}$	Port 2.4/Wait for ED	Input/Output
7	ED8/P0.8	External Data Bus/Port0	Input/Output	29	CLKI	Clock/Crystal In	Input
8	ED9/P0.9	External Data Bus/Port0	Input/Output	30	CLKO	Clock/Crystal Out	Output
9	V_{SS}	Ground		31	P2.2/TMO0	Port 2.2/Timer Output 0	Input/Output
10	ED10/P0.10	External Data Bus/Port0	Input/Output	32	LPF	PLL Low Pass Filter	Input
11	ED11/P0.11	External Data Bus/Port0	Input/Output	33	$\overline{RESET}$	Reset	Input
12	VAHI	Analog High Ref. Voltage	Input	34	V_{DD}	Power Supply	
13	VALO	Analog Low Ref. Voltage	Input	35	ED0/P0.0	External Data Bus/Port0	Input/Output
14	AGND	Analog Ground		36	ED1/P0.1	External Data Bus/Port0	Input/Output
15	AN0	A/D Input 0	Input	37	ED2/P0.2	External Data Bus/Port0	Input/Output
16	AN1	A/D Input 1	Input	38	V_{SS}	Ground	
17	AN2	A/D Input 2	Input	39	P2.0/INT0	Port 2.0/Interrupt 0	Input/Output
18	AN3	A/D Input 3	Input	40	ED12/P0.12	External Data Bus/Port0	Input/Output
19	P2.1/INT1	Port 2.1/Interrupt 1	Input/Output	41	ED13/P0.13	External Data Bus/Port0	Input/Output
20	AV_{CC}	Analog Power		42	ED14/P0.14	External Data Bus/Port0	Input/Output
21	V_{DD}	Power		43	V_{SS}	Ground	
22	RD/$\overline{WR}$	R/W Exteral Output Bus		44	ED15/P0.15	External Data Bus/Port0	Input/Output

Table 3. 64-Pin TQFP Z89223/273 Pin Description

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	ED3/P0.3	External Data Bus/Port0	Input/Output	33	$\overline{\text{HALT}}$	Halt Execution	Input
2	ED4/P0.4	External Data Bus/Port0	Input/Output	34	EA0	Ext Address 0	Output
3	V_{SS}	Ground		35	EA1	Ext Address 1	Output
4	V_{DD}	Power Supply		36	EA2	Ext Address 2	Output
5	ED5/P0.5	External Data Bus/Port0	Input/Output	37	V_{DD}	Power Supply	
6	P1.3/SDO	Port 1.3/Serial Output	Input/Output	38	P2.3/TMO1	Port2.3/Timer Output 1	Input/Output
7	ED6/P0.6	External Data Bus/Port0	Input/Output	39	$\overline{\text{DS}}$	Ext Data Strobe	Output
8	P1.4/SS	Port 1.4/Slave Select	Input/Output	40	P2.4/$\overline{\text{WAIT}}$	Port 2.4/Wait for ED	Input/Output
9	ED7/P0.7	External Data Bus/Port0	Input/Output	41	CLKI	Clock/Crystal In	Input
10	P1.5/SCLK	Port 1.5/Serial Clock	Input/Output	42	CLKO	Clock/Crystal Out	Output
11	P2.7	Port 2.7	Input/Output	43	P2.6/TMO2	Port 2.6/Timer Output 2	Input/Output
12	ED8/P0.8	External Data Bus/Port0	Input/Output	44	P2.2/TMO0	Port 2.2/Timer Output 0	Input/Output
13	ED9/P0.9	External Data Bus/Port0	Input/Output	45	P2.5/UI2	Port 2.5/User Input 2	Input/Output
14	V_{SS}	Ground		46	LPF	PLL Low Pass Filter	Input
15	ED10/P0.10	External Data Bus/Port0	Input/Output	47	$\overline{\text{RESET}}$	Reset	Input
16	V_{SS}	Ground		48	V_{SS}	Ground	
17	ED11/P0.11	External Data Bus/Port0	Input/Output	49	V_{DD}	Power Supply	
18	VAHI	Analog High Ref. Voltage	Input	50	V_{SS}	Ground	
19	V_{SS}	Ground		51	ED0/P0.0	External Data Bus/Port0	Input/Output
20	P1.6/UI0	Port 1.6/User Input 0	Input/Output	52	ED1/P0.1	External Data Bus/Port0	Input/Output
21	VALO	Analog Low Ref. Voltage	Input	53	ED2/P0.2	External Data Bus/Port0	Input/Output
22	P1.7/UI1	Port 1.7/User Input 1	Input/Output	54	P1.0/INT2	Port 1.0/Interrupt 2	Input/Output
23	AGND	Analog Ground		55	V_{SS}	Ground	
24	AN0	A/D Input 0	Input	56	P1.1/CLKOUT	Port 1.1/Clock Output	Input/Output
25	AN1	A/D Input 1	Input	57	P1.2/SDI	Port 1.2/Serial Input	Input/Output
26	AN2	A/D Input 2	Input	58	P2.0/INT0	Port 2.0/Interrupt 0	Input/Output
27	AN3	A/D Input 3	Input	59	ED12/P0.12	External Data Bus/Port0	Input/Output
28	V_{SS}	Ground		60	ED13/P0.13	External Data Bus/Port0	Input/Output
29	P2.1/INT1	Port 2.1/Interrupt 1	Input/Output	61	V_{DD}	Power Supply	
30	AVCC	Analog Power		62	ED14/P0.14	External Data Bus/Port0	Input/Output
31	V_{DD}	Power Supply		63	V_{SS}	Ground	
32	RD/$\overline{\text{WR}}$	R/W External Bus	Output	64	ED15/P0.15	External Data Bus/Port0	Input/Output

PIN CONFIGURATIONS (Continued)

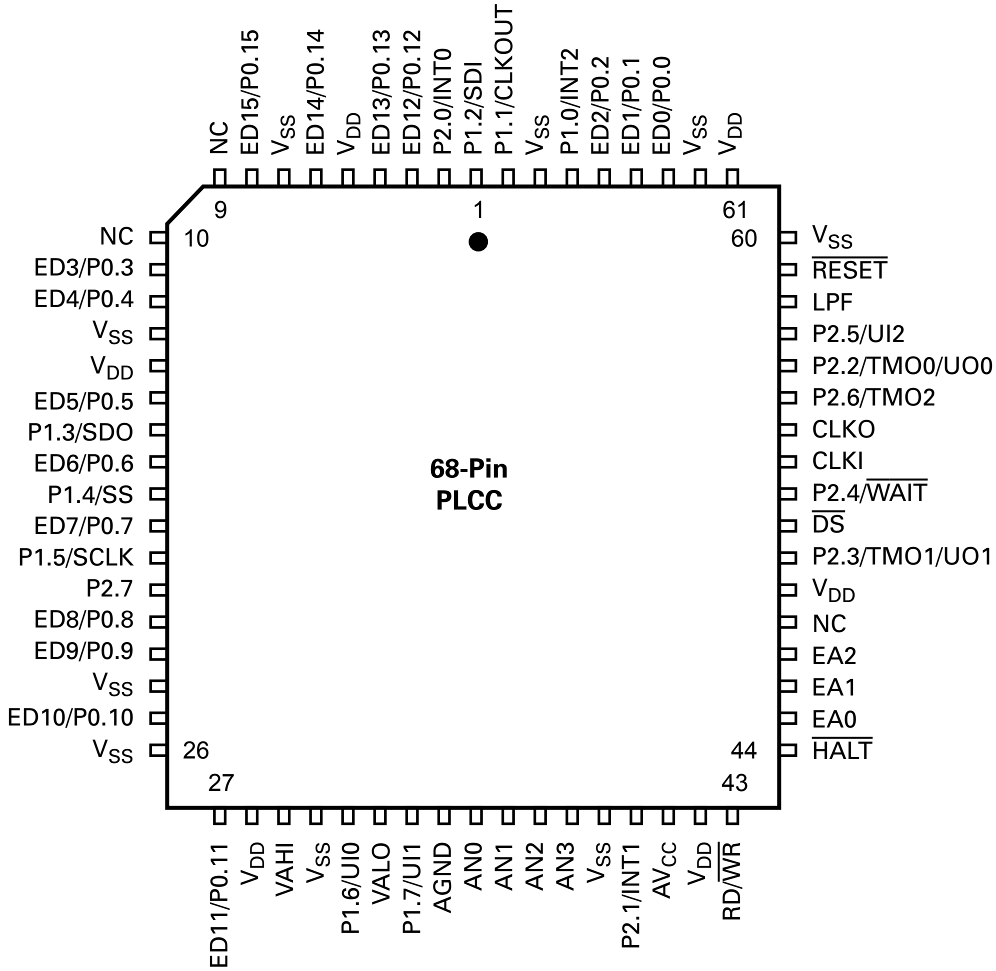

Figure 6. 68-Pin PLCC Z89323/373 Pin Configuration

DC ELECTRICAL CHARACTERISTICS

Table 6. ROM Version: V_{DD} = 5V ±10%, T_A = 0°C to +70°C for "S" temperature range T_A = –40°C to +85°C for "E" temperature range, unless otherwise noted; IDD measured with peripherals disabled

Symbol	Parameter	Condition	Min	Typical	Max
I_{DD-PLL}	Supply Current using PLL	V_{DD} = 5.0V, 20 MHz		60mA	66mA
I_{DD-ECD}	Supply Current using External Clock Direct	V_{DD} = 5.0V, 20 MHz		55 mA	61mA
I_{DD-XOD}	Supply Current using XTAL Oscillator Direct	V_{DD} = 5.0V, 32-kHz XTAL		250µA	275µA
$I_{DD-DEEP}$	Supply Current during Deep Sleep	V_{DD} = 5.0V, 32kHz XTAL		175µA	193µA
V_{IH}	Input High Level		2.7V		
V_{IL}	Input Low Level				0.8V
I_L	Input Leakage		-10µA		10µA
V_{OH}	Output High Voltage	I_{OH} = –100 µA	V_{DD}–0.2V		
		I_{OH} = –160 µA	2.4V		
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA			0.4V
		I_{OL} = 2.0 mA			0.5V
I_{FL}	Output Floating Leakage Current		-10µA		10µA

Table 7. OTP Version: V_{DD} = 5V ±10%, T_A = 0°C to +70°C for "S" temperature range T_A = –40°C to +85°C for "E" temperature range, unless otherwise noted; IDD measured with peripherals disabled

Symbol	Parameter	Condition	Min	Typical	Max
I_{DD-PLL}	Supply Current using PLL	V_{DD} = 5.0V, 20 MHz		78mA	86mA
I_{DD-ECD}	Supply Current using External Clock Direct	V_{DD} = 5.0V, 20 MHz		75mA	83mA
I_{DD-XOD}	Supply Current using XTAL Oscillator Direct	V_{DD} = 5.0V, 32-kHz XTAL		17mA	19mA
$I_{DD-DEEP}$	Supply Current during Deep Sleep	V_{DD} = 5.0V, 32kHz XTAL		17mA	19mA
V_{IH}	Input High Level		2.7V		
V_{IL}	Input Low Level				0.8V
I_L	Input Leakage		-10µA		10µA
V_{OH}	Output High Voltage	I_{OH} = –100 µA	V_{DD}–0.2V		
		I_{OH} = –160 µA	2.4V		
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA			0.4V
		I_{OL} = 2.0 mA			0.5V
I_{FL}	Output Floating Leakage Current		-10µA		10µA

AC ELECTRICAL CHARACTERISTICS

Table 8. V_{DD}= 5V ±10%, T_A = 0°C to +70°C for “S” Temperature Range T_A = –40°C to +85°C for “E” temperature range, unless otherwise noted

Symbol	Parameter	Min [ns]	Max [ns]
Clock			
TCY	CLKI Cycle Time for user-supplied clock	50	31250
CPWH	CLKI Pulse Width High	21	
CPWL	CLKI Pulse Width Low	21	
Tr	CLKI Rise Time for 20-MHz user-supplied clock		2
Tf	CLKI Fall Time for 20-MHz user-supplied clock		2
External Peripheral Bus			
EASET	EA Setup Time to $\overline{DS}$ Fall	10	
EAHOLD	EA Hold Time from $\overline{DS}$ Rise	4	
RWSET	Read/Write Setup Time to $\overline{DS}$ Fall	10	
RWHOLD	Read/Write Hold Time from $\overline{DS}$ Rise	0	
RDSET	Data Read Setup Time to $\overline{DS}$ Rise	15	
RDHOLD	Data Read Hold Time from $\overline{DS}$ Rise	0	
WRVALID	Data Write Valid Time from $\overline{DS}$ Fall		5
WRHOLD	Data Write Hold Time from $\overline{DS}$ Rise	2	
Reset			
RRISE	Reset Rise Time		20 TCY
RWIDTH	Reset Low Pulse Width	2 TCY	
Interrupt			
IWIDTH	Interrupt Pulse Width	1TCY	
Halt			
HWIDTH	Halt Low Pulse Width	3 TCY	
Wait State			
WLAT	Wait Latency Time from $\overline{DS}$ Fall		7
WDEA	Wait Deassert Setup Time to CLKOUT Rise	TBD	
SPI			
SDI–SCLK	Serial Data In to Serial Clock Setup Time	10	
SCLK–SDO	Serial Clock to Serial Data Out Valid	15	
SS–SCLK	Slave Select to Serial Clock Setup Time	1/2 SCLK Period	
SS–SDO	Slave Select to Serial Data Out Valid	15	
SCLK–SDI	Serial Clock to Serial Data In Hold Time	10	

TIMING DIAGRAMS (Continued)

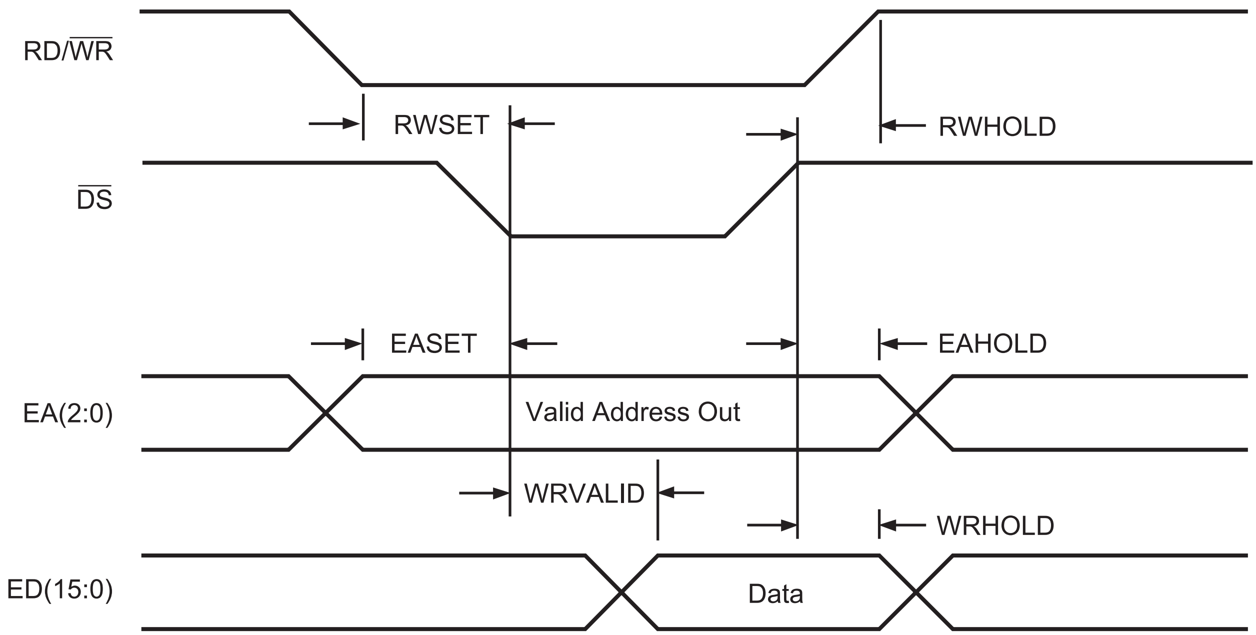

Figure 13. Write Timing

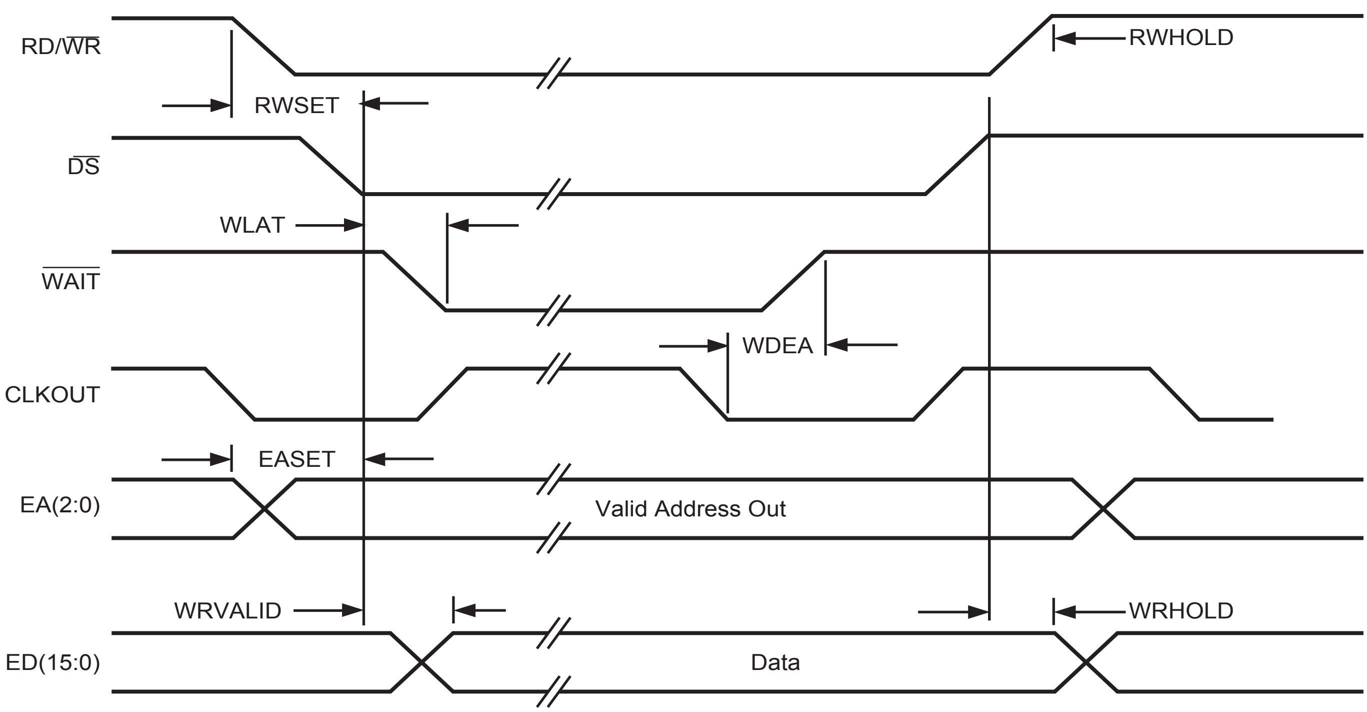

Figure 14. Write Timing Using WAIT Pin

FUNCTIONAL DESCRIPTION

Instruction Timing. Most instructions are executed in one machine cycle. A multiplication or multiply/accumulate instruction requires a single cycle. Long immediate instructions, and Jump or Call instructions, are executed in two machine cycles. Specific instruction cycle times are described in the Instruction Description section.

Multiply/Accumulate. The multiplier can perform a 16-bit x 16-bit multiply, or multiply/accumulate, in one machine cycle using the Accumulator and/or both the X and Y inputs. The multiplier produces a 32-bit result, however, only the 24 most significant bits are saved for the next instruction or accumulation. For operations on very small numbers where the least significant bits are important, the data should first be scaled to avoid truncation errors.

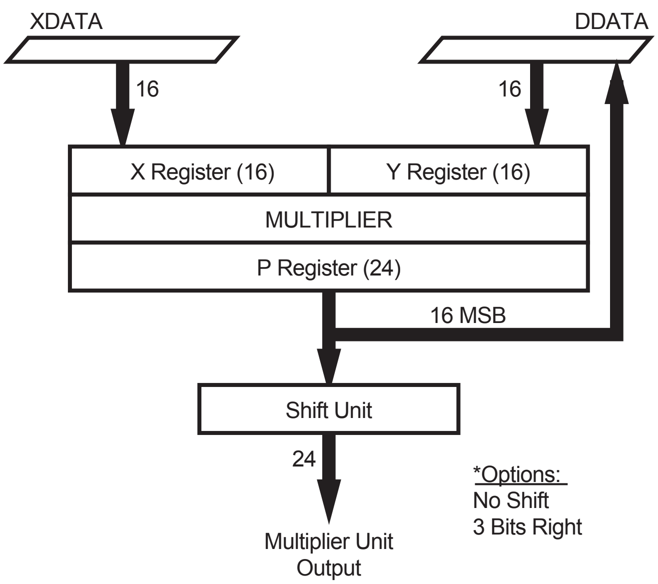

Figure 16. Multiplier Block Diagram

All inputs to the multiplier should be fractional two's-complement, 16-bit binary numbers, which places them in the range [–1 to 0.9999695]. The result is in 24 bits, so the range is [–1 to 0.9999999].

If 8000H is loaded into both the X and Y registers, the multiplication produces an incorrect result. Positive one cannot be represented in fractional notation, and the multiplier actually yields the result 8000H x 8000H = 8000H (–1 x –1 = –1). The user should avoid this case to prevent erroneous results.

A shifter between the P Register and the Multiplier Unit Output can shift the data by three bits right or no shift.

Data Bus Bank Switch. There is a switch that connects the X Bus to the DDATA Bus that allows both the X and Y registers to be loaded with the same operand for a one cycle squaring operation. The switch is also used to read the X register.

ALU. The ALU features two input ports. One is connected to the output of the 24-bit Accumulator. The other input selects either the Multiplier Unit Output or the 16-bit DDATA bus (left-justified with zeros in the eight LSBs). The ALU performs arithmetic, logic, and shift operations.

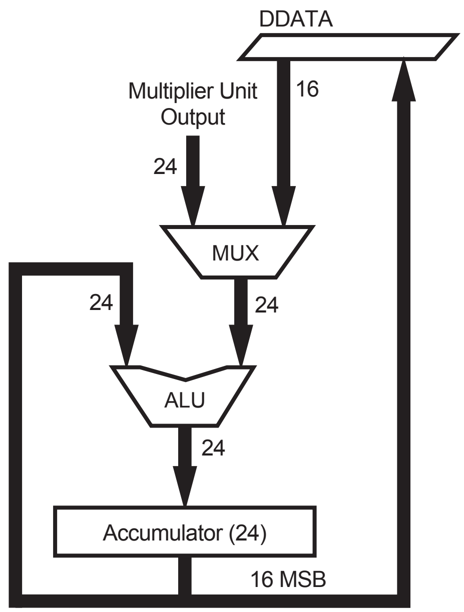

Figure 17. ALU Block Diagram

Hardware Stack. A six-level hardware stack is connected to the DDATA bus to hold subroutine return addresses or data. The CALL instruction pushes PC+2 onto the stack, and the RET instruction pops the contents of the stack to the PC.

User Inputs and Outputs. The Z893x3 features three User Inputs, UI0, UI1, and UI2. Pins UI0 and UI1 are connected directly to status register bits S10 and S11, and can be read, or used as a condition code in any conditional instruction. Pins UI0, UI1 and UI2 may also be used to clock the Counter/Timers. There are two user output bits, UO0 and UO1, which share pins with the timer outputs TMO0 and TMO1 on Port2. When the User Outputs are enabled, they are the complements of bits S5 and S6 of the Status Register.

I/O PORTS

I/O pin allocation of ports for the different package types is designed to provide configuration flexibility. Each port line of Ports 0, 1, and 2 can be independently selected as an input or an output. Each port's output lines can be globally selected as push-pull or as open-drain outputs

Table 15. I/O Port Bit Allocations

Device Pins	44-Pin PLCC, 44-Pin PQFP	64-Pin TQFP, 68-Pin PLCC	80-Pin PQFP
P0 MSB	ED15–ED8, or P0.15–P0.8, or P1.7–P1.0	ED15–ED8, or P0.15–P0.8	ED15–ED8, or P0.15–P0.8
P0 LSB	ED7–ED0, or P0.7–P0.0	ED7–ED0, or P0.7–P0.0	ED7–ED0, or P0.7–P0.0
P1		P1.7–P1.0	P1.7–P1.0
P2	P2.4–P2.0	P2.7–P2.0	P2.7–P2.0
P3			P3.7–P3.0

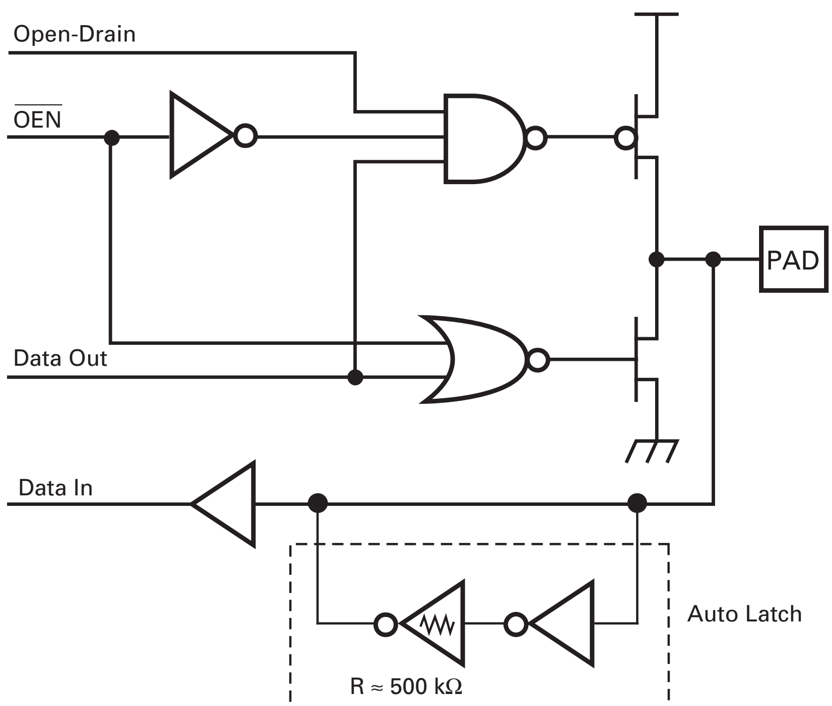

Figure 24. Port 0, 1 and 2 Configuration

Port1—8-Bit Programmable I/O

Bank15/EXT1 is the Port1 control register. The MSB is the Port1 direction control. Port1 data is accessed as the LSB of EXT5 in Banks 0, 1, or 5. The Port1 pins can also be mapped to internal functions. When INT2, CLKOUT, UI0 and UI1, or the SPI are enabled, they use Port1 pins. The 44-pin packages do not feature Port1 pins, however, Port1 and its internal functions can be mapped to the MSB of the ED Bus/Port0 pins. See bits 2–0 of Bank15/EXT1.

Table 16. Port1 Bit Function Allocation

Port Pin	IF	Condition	Then	Else
P1.0/INT2	Bank15/EXT1 Bit 3 = 1	Enable INT2	INT2	P1.0
P1.1/CLKOUT	Bank15/EXT1 Bit 5 = 1	Enable CLKOUT	CLKOUT	P1.1
P1.2/SDI	Bank15/EXT4 Bit 0 = 1	Enable SPI	SDI	P1.2
P1.3/SDO	Bank15/EXT4 Bit 0 = 1	Enable SPI	SDO	P1.3
P1.4/SS	Bank15/EXT4 Bit 0 = 1	Enable SPI	SS	P1.4
P1.5/SCLK	Bank15/EXT4 Bit 0 = 1	Enable SPI	SCLK	P1.5
P1.6/UI0	Bank13/EXT1 Bits [2,1] = 10, or Bank14/EXT1 Bits [2,1] = 10	Enable UI0	UI0	P1.6
P1.7/UI1	Bank13/EXT1 Bits [2,1] = 11, or Bank14/EXT1 Bits [2,1] = 11	Enable UI1	UI1	P1.7

PERIPHERALS (Continued)

Counter/Timers (C/T0 and C/T1)

The Z893x3 features two 16-bit Counter/Timers (C/T) that can be independently configured to operate in various modes. Each is implemented as a 16-bit Load Register and a 16-bit down counter. Either C/T input can be selected from UI0 or UI1. Either C/T output can be directed to TMO0 or TMO1. The C/T clock is a scaled version of the system clock. Each C/T features an 8-bit prescaler. The clock rates of the two C/T are independent of each other. The C/Ts can be programmed to recognize clock events on the rising edge, the falling edge, or both rising and falling edges of the input signal. Outputs on TMO0 or TMO1 can be programmed to occur with either polarity.

If either C/T is enabled and an output pin TMO0 or TMO1 is selected, and at the same time User Outputs are enabled, the C/T takes precedence, and Status Register bits 5 or 6 do not affect the state of the selected pin.

C/T Modes of Operation:

MODE 0—Square Wave Output. The C/T is configured to generate a continuous square wave of 50% duty cycle. Writing a new value to the TMLR Register takes effect at the end of the current cycle, unless TMR is written.

MODE 1—Retriggerable One-Shot. The C/T is configured to generate a single pulse of programmable duration. The pulse may be either logic High or logic Low. Retriggering the one-shot before the end of the pulse causes it to retrigger for a new duration.

MODE 2—8-Bit PWM. The C/T is configured to generate a pulse-width modulated waveform. The duty cycle ranges from 0–100% (0/256 to 255/256; 8-bits) of a cycle in steps of 1/256 of a cycle. The asserted state of the waveform may be either logic High or logic Low. Writing a new pulse-width value to the TMLR Register takes effect at the end of current cycle, unless TMR is written.

MODE 3—16-Bit PWM. The C/T is configured to generate a pulse-width modulated waveform. The duty cycle ranges from 0–100% (0/65,536 to 65,535/65,536; 16-bits) of a cycle in steps of 1/65,536 of a cycle. The asserted state of the waveform may be either logic High or logic Low. Writing a new pulse-width value to the TMLR Register takes effect at the end of current cycle, unless TMR is written.

MODE 4—Finite Pulse String Generator. The C/T is configured to generate 1 to 65,535 pulses. The output pulses are actually from the Timer Clock Prescaler divided by 2 (TMCLK). They are gated to the output until the Timer Down-Counter underflows.

MODE 5—Externally Clocked One-Shot. The C/T is configured to generate an output pulse. The pulse may be either logic High or logic Low. It is deasserted when a programmable number of input events (up to 65,535) occur on the input pin, UI0 or UI1.

MODE 6—Software Watch-Dog Timer. The C/T is configured to generate a Hardware Reset on time-out, unless retriggered by software.

MODE 7—Hardware Watch-Dog Timer. The C/T is configured to generate a Hardware Reset on time-out unless retriggered by an event on the input pin, UI0 or UI1.

MODE 8—Pulse Stopwatch. The C/T is configured to measure the time during which its input is asserted.

MODE 9—Edge-to-Edge Stopwatch. The C/T is configured to measure the period from one rising (falling) edge to the next rising (falling) edge on the input.

MODE 10—Edge Counter. The C/T is configured to count a number of input edges (up to 65,535). Input edges may be selected as rising or falling or both.

MODE 11—Gated Edge Counter. The C/T is configured to count the number of input edges (up to 65,535) in a time window set by the second timer. Edges are counted until the second timer underflows. Input edges may be selected as rising, falling, or both.

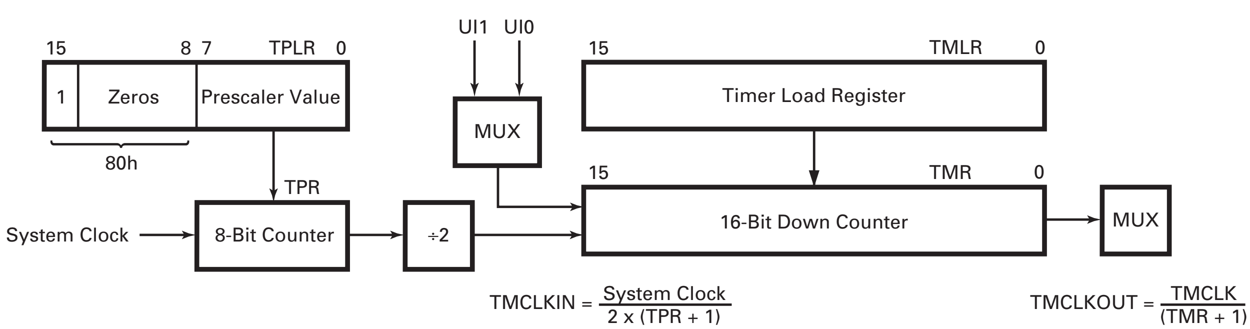

Figure 31. Counter/Timer 0 and 1 Block Diagram

GENERAL-PURPOSE COUNTER/TIMER (C/T2) (Continued)

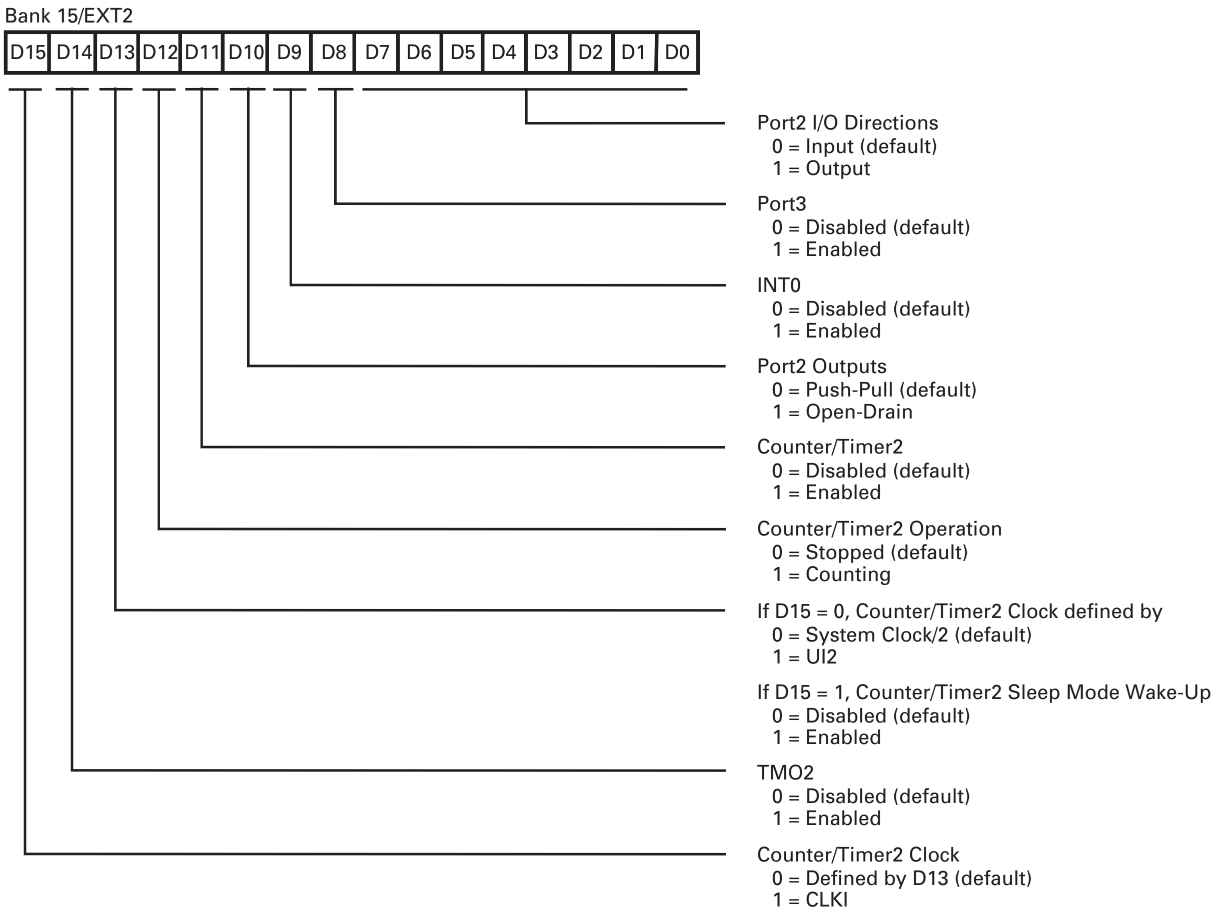

Figure 38. Counter/Timer2 Control Register

SERIAL PERIPHERAL INTERFACE

The Z893x3 incorporates a Serial Peripheral Interface (SPI) for communication with other microcontrollers and peripherals. The SPI can be operated either as the system Master, or as a system Slave. The SPI consists of three registers: the SPI Control Register (Bank15/EXT4), the SPI Receive/Buffer Register (RxBUF), and the SPI Shift Register.

SPI Data Access

Receive operations are double buffered. Bank0/EXT3 accesses both RxBUF for read (receive) operations, and the SPI shift register for write (transmit) operations.

Bank 0/EXT 3 Register

D15	D14							D7	D6	D5	D4	D3	D2	D1	D0

Bits 7–0 SPI Data (SPI Shift Register for transmit and RxBUF for receive)
Bit 14 Receive Character Available
Bit 15 Receive Character Overrun

Figure 39. SPI Data Access

SPI Control Register

This register is the Low byte of Bank15/EXT4. It is a read/write register that controls Master/Slave selection, SS polarity, clock source and phase selection, and indicates byte available and data overrun conditions. The control register is multifunction depending on Master/Slave mode selection.

In Master mode, Bit 6 defines the SPI clock source. A “1” selects SCLK = C/T0 output, and a “0” selects SCLK = System Clock divided down by 2, 4, 8, or 16, as determined by bits 1 and 2.

In Slave Mode, bit 1 is the Receive Byte Overrun flag. This flag can be cleared by writing a “0” to this bit. Bit 2 is the SDO output enable.A “0” tristates SDO, a “1” enables data output on SDO. Bit 4 signals that a receive byte is available in the RxBUF Register. If the associated interrupt enable bit is enabled, an interrupt is generated.

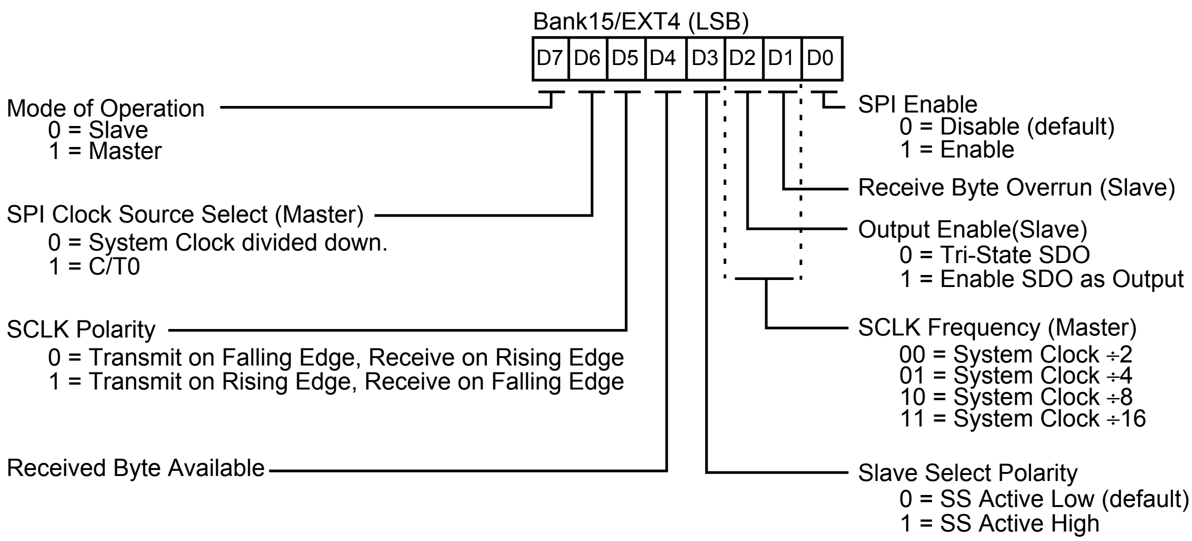

Figure 40. SPI Control Register

Master Mode Operation

The DSP must first activate the target slave’s select pin through an I/O port. Loading data into the SPI Shift Register initiates the transfer. Data is transferred out the SDO pin to the slave one data bit per SCLK cycle. The MSB is shifted out first. At the conclusion of the transfer, the Receive Byte Available flag is set, and if enabled, an SPI interrupt is generated. The Receive Byte Available flag is reset when RxBUF is read.

CONDITION CODES

The following Instruction Description defines the condition codes supported by the DSP assembler. If the instruction description refers to the <cc> (condition code) symbol in one of its addressing modes, the instruction only executes if the condition is true.

Code	Description
C	Carry
EQ	Equal (same as Z)
F	False
IE	Interrupts Enabled
MI	Minus
NC	No Carry
NE	Not Equal (same as NZ)
NIE	Not Interrupts Enabled
NOV	Not Overflow
NU0	Not User Zero
NU1	Not User One
NZ	Not zero
OV	Overflow
PL	Plus (Positive)
U0	User Zero
U1	User One
UGE	Unsigned Greater Than or Equal (Same as NC)
ULT	Unsigned Less Than (Same as C)
Z	Zero

INSTRUCTION DESCRIPTIONS (Continued)

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
LD	Load	LD<dest>,<src>	A,<hwregs>	1	1	LD A,X
	destination		A,<dregs>	1	1	LD A,D0:0
	with source		A,<pregs>	1	1	LD A,P0:1
			A,<regind>	1	1	LD A,@P1:1
			A,<memind>	1	3	LD A,@D0:0
			A,<direct>	1	1	LD A,124
			<direct>,A	1	1	LD 124,A
			<dregs>,<hwregs>	1	1	LD D0:0,EXT7
			<pregs>,<simm>	1	1	LD P1:1,#%FA
			<pregs>,<hwregs>	1	1	LD P1:1,EXT1
			<regind>,<limm>	1	1	LD@P1:1,#1234
			<regind>,<hwregs>	1	1	LD @P1:1+,X
			<hwregs>,<pregs>	1	1	LD Y,P0:0
			<hwregs>,<dregs>	1	1	LD SR,D0:0
			<hwregs>,<limm>	2	2	LD PC,#%1234
			<hwregs>,<accind>	1	3	LD X,@A
			<hwregs>,<memind>	1	3	LD Y,@D0:0
			<hwregs>,<regind>	1	1	LD A,@P0:0–LOOP
			<hwregs>,<hwregs>	1	1	LD X,EXT6

Notes:
When <dest> is <hwregs>, <dest> cannot be P.
When <dest> is <hwregs> and <src> is <hwregs>, <dest> cannot be EXTn if <src> is EXTn, <dest> cannot be X if <src> is X, <dest> cannot be SR if <src> is SR.
When <src> is <accind> <dest> cannot be A.

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
MLD	Multiply	MLD <src1>,<src2>	<hwregs>,<regind>	1	1	MLD A,@P0:0+LOOP
		[,<bank switch>]	<hwregs>,<regind>,	1	1	MLD A,@P1:0,OFF
			<bank switch>	1	1	MLD @P1:1,@P2:0
			<regind>,<regind>	1	1	MLD @P0:1,@P1:0,ON
			<regind>,<regind>,			
			<bank switch>			

Notes:
If src1 is <regind> it must be a bank 1 register. Src2's <regind must be a bank 0 register.
<hwregs> for src1 cannot be X.
For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, the <bank switch> defaults to ON.

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
MPYA	Multiply and	MPYA <src1>,<src2>	<hwregs>,<regind>	1	1	MPYA A,@P0:0
	add	[,<bank switch>]	<hwregs>,<regind>,	1	1	MPYA A,@P1:0,OFF
			<bank switch>	1	1	MPYA @P1:1,@P2:0
			<regind>,<regind>	1	1	MPYA@P0:1,@P1:0,ON
			<regind>,<regind>,			
			<bank switch>			

Notes:
If src1 is <regind> it must be a bank 1 register. Src2's <regind> must be a bank 0 register.
<hwregs> for src1 cannot be X.
For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, the <bank switch> defaults to ON.

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
MPYS	Multiply and	MPYS <src1>,<src2>	<hwregs>,<regind>	1	1	MPYS A,@P0:0
	subtract	[,<bank switch>]	<hwregs>,<regind>,	1	1	MPYS A,@P1:0,OFF
			<bank switch>	1	1	MPYS @P1:1,@P2:0
			<regind>,<regind>	1	1	MPYS
			<regind>,<regind>,			@P0:1,@P1:0,ON
			<bank switch>			

ORDERING INFORMATION

Package Type	ROM	OTP
44-Pin PLCC	Z8922320VSC	Z8927320VSC
	Z8922320VEC	
44-Pin PQFP	Z8922320FSC	
	Z8922320FEC	
64-Pin TQFP	Z8932320ASC	Z8937320ASC
	Z8932320AEC	
68-Pin PLCC	Z8932320VSC	Z8937320VSC
	Z8932320VEC	
80-Pin PQFP	Z8932320FSC	Z8937320FSC
	Z8932320FEC	

For fast results, contact your local ZiLOG sales office for assistance in ordering the part required.

CODES

Package	V = PLCC
	A = TQFP
	F = PQFP
Temperature	S = 0°C to +70°C
	E = –40°C to 85°C
Speed	20 = 20 MHz
Environmental	C = Plastic Standard

Example:

Z 89323 20 V S C is a Z89323, 20 MHz, PLCC, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- V — Package
- 20 — Speed/Bond Out Option
- 89323 — Product Number
- Z — ZiLOG Prefix

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