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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	SPI, 3-Wire Serial
Clock Rate	20MHz
Non-Volatile Memory	OTP (16kB)
On-Chip RAM	1kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-TQFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8937320asg

External Bus and External Registers. The following is made to clarify naming conventions used in this specification. The external bus and external registers are external to the DSP core, and are used to access internal and external peripherals.

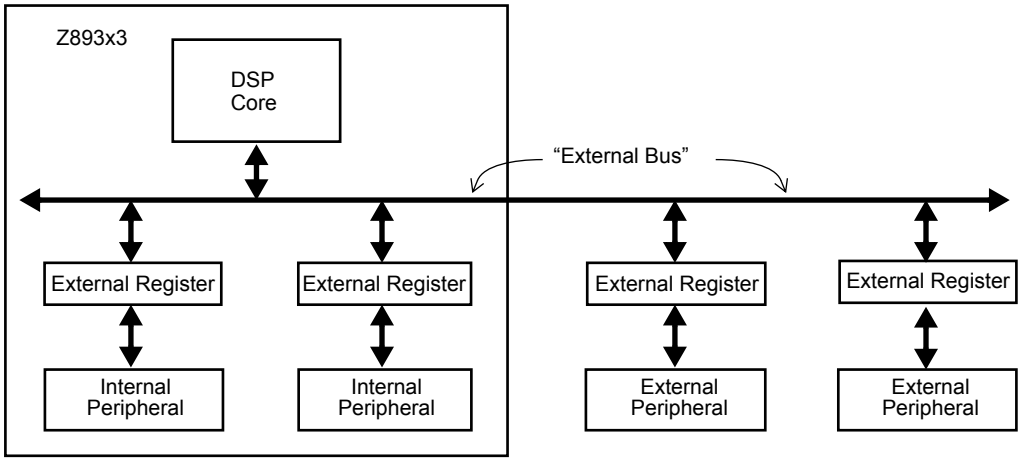

Figure 2. "External" Bus

TMO1/UO1. Counter/Timer Output or User Output 1 (output). Counter/Timer 0 and Counter/Timer 1 can be programmed to provide output on this pin. When User Outputs are enabled, and the Counter/Timer is disabled, this pin provides the complement of Status Register bit 6.

TMO2. Counter/Timer 2 Output (output). This pin is the output of Counter/Timer 2

P0.15–P0.0. Port0 (input/output). This is a 16-bit user I/O port. Bits can be configured as input or output or globally as open-drain output. When enabled, Port0 uses the 16 data lines of the ED bus. The function of these pins can be dynamically changed by writing to the Port0 configuration registers. The High byte can also be configured to Port1 as described in the I/O Port section.

P1.7–P1.0. Port1 (input/output). These pins are Port1 inputs or outputs when not configured for use as special purpose peripheral interface. The following eight pin functions preempt use of these pins when enabled. INT2, CLKOUT, SDI, SDO, SS, SCLK, UI0, UI1.

Note: These pins are not bonded out on the 44-pin packages.

P2.7–P2.0. Port2 (input/output). These pins are Port2 inputs or outputs when not configured as peripheral interfaces. The following seven pin functions preempt use of P2.6–P2.0 when enabled. INT0, INT1, TMO0/UO0, TMO1/UO1, $\overline{\text{WAIT}}$, UI2, TMO2. P2.7 does not include a dual function.

Note: P2.7–P2.5 are not bonded out on the 44-pin packages.

The following port pins are available only on the 80-pin package:

P3.7–P3.4. Port3 (output). These pins are Port3 outputs.

P3.3–P3.0. Port3 (input). These pins are Port3 inputs.

Table 1. 44-Pin PLCC Z89223/273 Pin Description

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	P2.0/INT0	Port 2.0/Interrupt 0	Input/Output	23	AN2	A/D Input 2	Input
2	ED12/P0.12	External Data Bus/Port0	Input/Output	24	AN3	A/D Input 3	Input
3	ED13/P0.13	External Data Bus/Port0	Input/Output	25	P2.1/INT1	Port 2.1/Interrupt 1	Input/Output
4	ED14/P0.14	External Data Bus/Port0	Input/Output	26	AV_{CC}	Analog Power	
5	V_{SS}	Ground		27	V_{DD}	Power Supply	
6	ED15/P0.15	External Data Bus/Port0	Input/Output	28	RD/$\overline{WR}$	R/W External Bus	Output
7	ED3/P0.3	External Data Bus/Port0	Input/Output	29	EA0	Ext Address 0	Output
8	ED4/P0.4	External Data Bus/Port0	Input/Output	30	EA1	Ext Address 1	Output
9	V_{SS}	Ground		31	EA2	Ext Address 2	Output
10	ED5/P0.5	External Data Bus/Port0	Input/Output	32	P2.3/TMO1	Port 2.3/Timer Output 1	Input/Output
11	ED6/P0.6	External Data Bus/Port0	Input/Output	33	$\overline{DS}$	Ext Data Strobe	Output
12	ED7/P0.7	External Data Bus/Port0	Input/Output	34	P2.4/$\overline{WAIT}$	Port 2.4/Wait for ED	Input/Output
13	ED8/P0.8	External Data Bus/Port0	Input/Output	35	CLKI	Clock/Crystal In	Input
14	ED9/P0.9	External Data Bus/Port0	Input/Output	36	CLKO	Clock/Crystal Out	Output
15	V_{SS}	Ground		37	P2.2/TMO0	Port 2.2/Timer Output 0	Input/Output
16	ED10/P0.10	External Data Bus/Port0	Input/Output	38	LPF	PLL Low Pass Filter	Input
17	ED11/P0.11	External Data Bus/Port0	Input/Output	39	$\overline{RESET}$	Reset	Input
18	VAHI	Analog High Ref. Voltage	Input	40	V_{DD}	Power	
19	VALO	Analog Low Ref. Voltage	Input	41	ED0/P0.0	External Data Bus/Port0	Input/Output
20	AGND	Analog Ground		42	ED1/P0.1	External Data Bus/Port0	Input/Output
21	AN0	A/D Input 0	Input	43	ED2/P0.2	External Data Bus/Port0	Input/Output
22	AN1	A/D Input 1	Input	44	V_{SS}	Ground	

PIN CONFIGURATIONS (Continued)

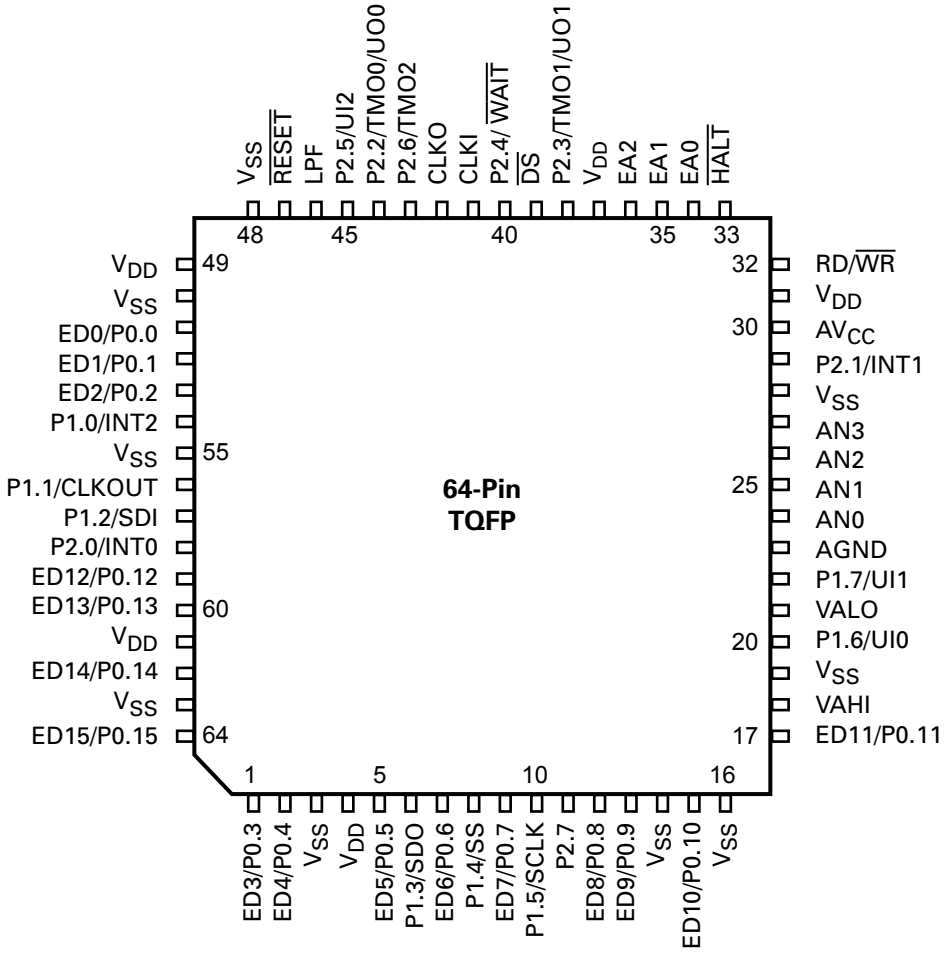

Figure 5. 64-Pin TQFP Z89323/373 Pin Configuration

PIN CONFIGURATIONS (Continued)

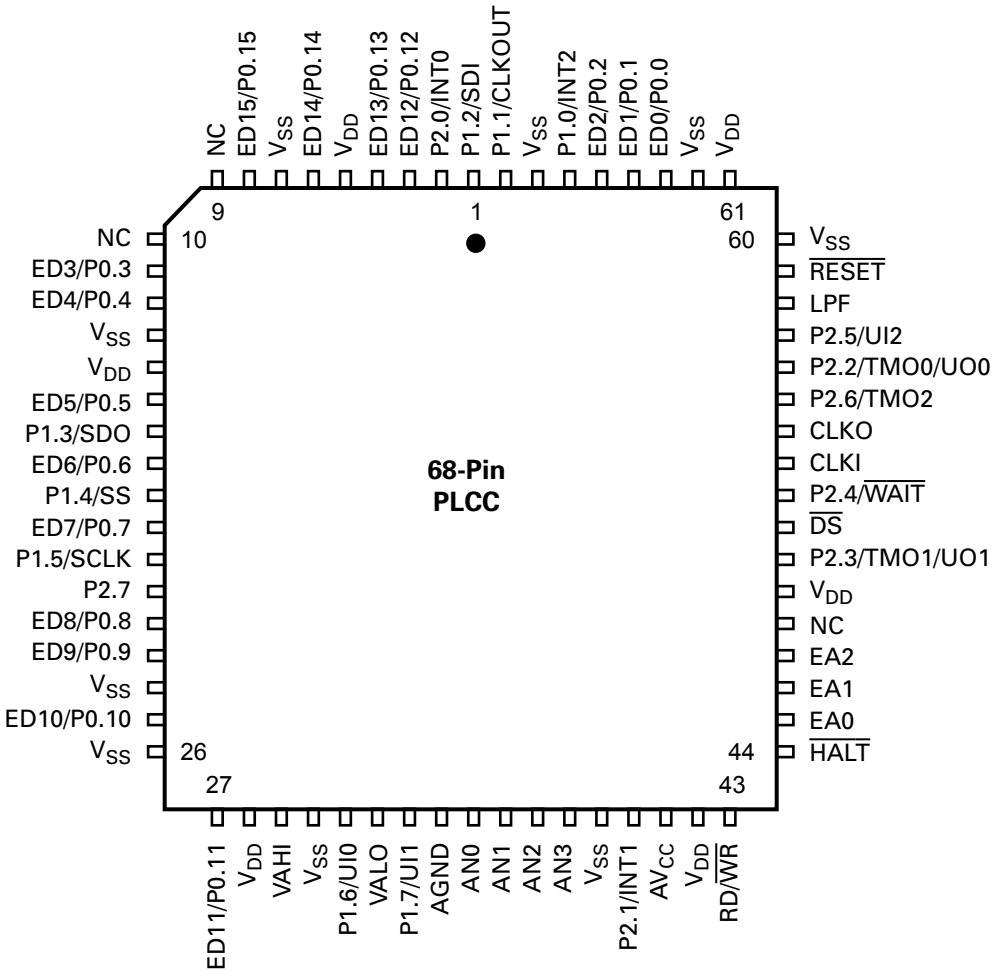

Figure 6. 68-Pin PLCC Z89323/373 Pin Configuration

Table 4. 68-Pin PLCC Z89323/373 Pin Description

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	P1.2/SDI	Port 1.2/Serial Input	Input/Output	35	AN0	A/D Input 0	Input
2	P2.0/INT0	Port 2.0/Interrupt 0	Input/Output	36	AN1	A/D Input 1	Input
3	ED12/P0.12	External Data Bus/Port0	Input/Output	37	AN2	A/D Input 2	Input
4	ED13/P0.13	External Data Bus/Port0	Input/Output	38	AN3	A/D Input 3	Input
5	V_{DD}	Power Supply		39	V_{SS}	Ground	
6	ED14/P0.14	External Data Bus/Port0	Input/Output	40	P2.1/INT1	Port 2.1/Interrupt 1	Input/Output
7	V_{SS}	Ground		41	AVCC	Analog Power	
8	ED15/P0.15	External Data Bus/Port0	Input/Output	42	V_{DD}	Power Supply	
9	NC	No Connection		43	RD/$\overline{WR}$	R/W External Bus	Output
10	NC	No Connection		44	$\overline{HALT}$	Halt Execution	Input
11	ED3/P0.3	External Data Bus/Port0	Input/Output	45	EA0	Ext Address 0	Output
12	ED4/P0.4	External Data Bus/Port0	Input/Output	46	EA1	Ext Address 1	Output
13	V_{SS}	Ground		47	EA2	Ext Address 2	Output
14	V_{DD}	Power Supply		48	NC	No Connection	
15	ED5/P0.5	External Data Bus/Port0	Input/Output	49	V_{DD}	Power Supply	
16	P1.3/SDO	Port 1.3/Serial Output	Input/Output	50	P2.3/TMO1	Port2.3/Timer Output 1	Input/Output
17	ED6/P0.6	External Data Bus/Port0	Input/Output	51	$\overline{DS}$	Ext Data Strobe	Output
18	P1.4/SS	Port 1.4/Slave Select	Input/Output	52	P2.4/$\overline{WAIT}$	Port 2.4/Wait for ED	Input/Output
19	ED7/P0.7	External Data Bus/Port0	Input/Output	53	CLKI	Clock/Crystal In	Input
20	P1.5/SCLK	Port 1.5/Serial Clock	Input/Output	54	CLKO	Clock/Crystal Out	Output
21	P2.7	Port 2.7	Input/Output	55	P2.6/TMO2	Port 2.6/Timer Output 2	Input/Output
22	ED8/P0.8	External Data Bus/Port0	Input/Output	56	P2.2/TMO0	Port 2.2/Timer Output 0	Input/Output
23	ED9/P0.9	External Data Bus/Port0	Input/Output	57	P2.5/UI2	Port 2.5/User Input 2	Input/Output
24	V_{SS}	Ground		58	LPF	PLL Low Pass Filter	Input
25	ED10/P0.10	External Data Bus/Port0	Input/Output	59	$\overline{RESET}$	Reset	Input
26	V_{SS}	Ground		60	V_{SS}	Ground	
27	ED11/P0.11	External Data Bus/Port0	Input/Output	61	V_{DD}	Power Supply	
28	V_{DD}	Power Supply		62	V_{SS}	Ground	
29	VAHI	Analog High Ref. Voltage	Input	63	ED0/P0.0	External Data Bus/Port0	Input/Output
30	V_{SS}	Ground		64	ED1/P0.1	External Data Bus/Port0	Input/Output
31	P1.6/UI0	Port 1.6/User Input 0	Input/Output	65	ED2/P0.2	External Data Bus/Port0	Input/Output
32	VALO	Analog Low Ref. Voltage	Input	66	P1.0/INT2	Port 1.0/Interrupt 2	Input/Output
33	P1.7/UI1	Port 1.7/User Input 1	Input/Output	67	V_{SS}	Ground	
34	AGND	Analog Ground		68	P1.1/CLKOUT	Port 1.1/Clock Output	Input/Output

PIN CONFIGURATIONS (Continued)

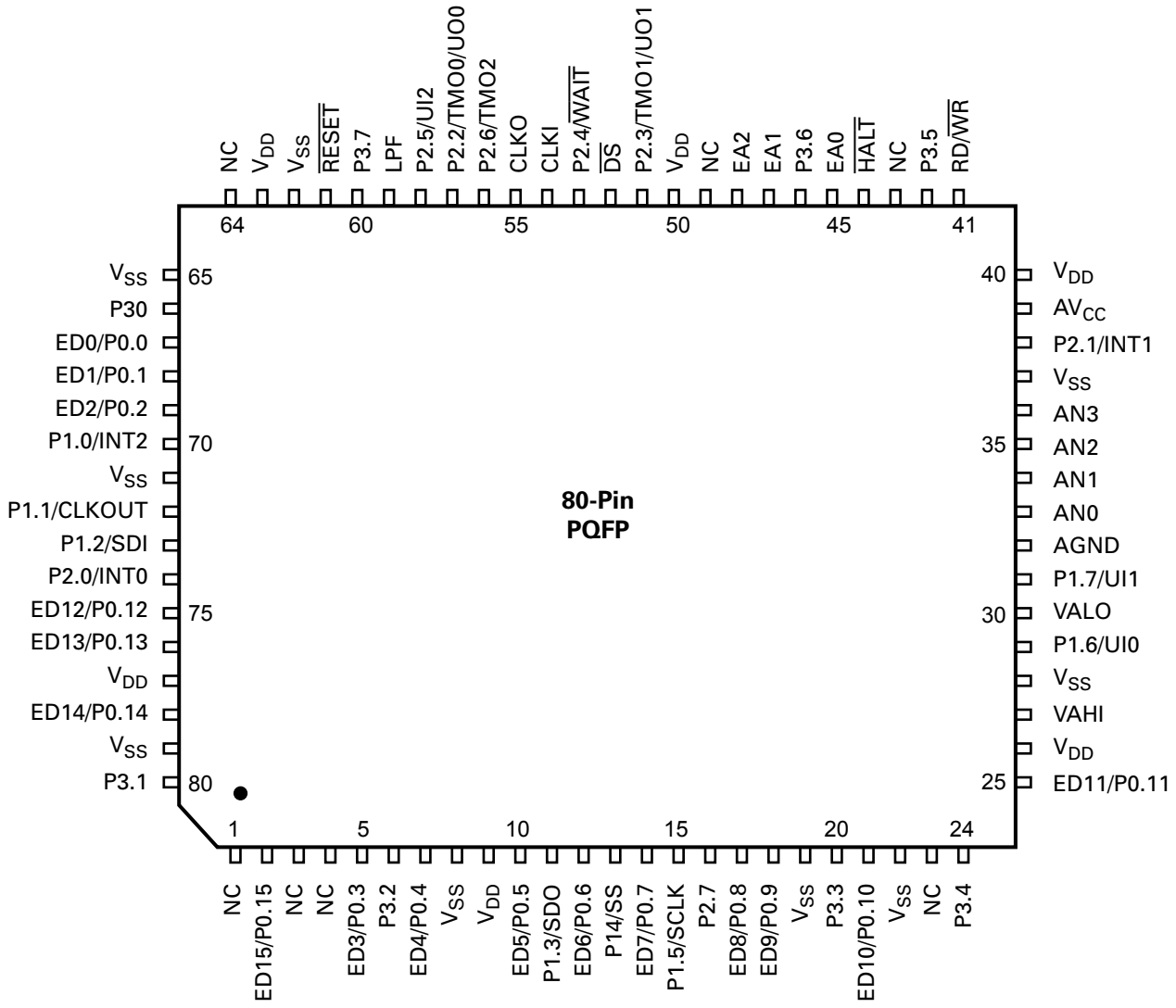

Figure 7. 80-Pin PQFP Z89323/373 Pin Configuration

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage	–0.3	7.0	V
T_{STG}	Storage Temperature	–65	150	°C
T_A	Ambient Operating Temperature			
	"S" device	0	70	°C
	"E" device	–40	85	°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin.

Positive current $I_{(+)}$ flows in to the referenced pin.

Negative current $I_{(-)}$ flows out of the referenced pin.

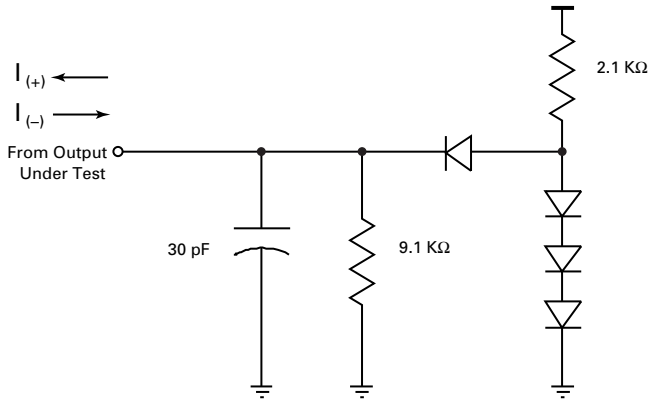

Figure 8. Test Load Diagram

AC ELECTRICAL CHARACTERISTICS

Table 8. V_{DD}= 5V ±10%, T_A = 0°C to +70°C for "S" Temperature Range T_A = –40°C to +85°C for "E" temperature range, unless otherwise noted

Symbol	Parameter	Min [ns]	Max [ns]
Clock			
TCY	CLKI Cycle Time for user-supplied clock	50	31250
CPWH	CLKI Pulse Width High	21	
CPWL	CLKI Pulse Width Low	21	
Tr	CLKI Rise Time for 20-MHz user-supplied clock		2
Tf	CLKI Fall Time for 20-MHz user-supplied clock		2
External Peripheral Bus			
EASET	EA Setup Time to $\overline{DS}$ Fall	10	
EAHOLD	EA Hold Time from $\overline{DS}$ Rise	4	
RWSET	Read/Write Setup Time to $\overline{DS}$ Fall	10	
RWHOLD	Read/Write Hold Time from $\overline{DS}$ Rise	0	
RDSET	Data Read Setup Time to $\overline{DS}$ Rise	15	
RDHOLD	Data Read Hold Time from $\overline{DS}$ Rise	0	
WRVALID	Data Write Valid Time from $\overline{DS}$ Fall		5
WRHOLD	Data Write Hold Time from $\overline{DS}$ Rise	2	
Reset			
RRISE	Reset Rise Time		20 TCY
RWIDTH	Reset Low Pulse Width	2 TCY	
Interrupt			
IWIDTH	Interrupt Pulse Width	1TCY	
Halt			
HWIDTH	Halt Low Pulse Width	3 TCY	
Wait State			
WLAT	Wait Latency Time from $\overline{DS}$ Fall		7
WDEA	Wait Deassert Setup Time to CLKOUT Rise	TBD	
SPI			
SDI–SCLK	Serial Data In to Serial Clock Setup Time	10	
SCLK–SDO	Serial Clock to Serial Data Out Valid	15	
SS–SCLK	Slave Select to Serial Clock Setup Time	1/2 SCLK Period	
SS–SDO	Slave Select to Serial Data Out Valid	15	
SCLK–SDI	Serial Clock to Serial Data In Hold Time	10	

TIMING DIAGRAMS

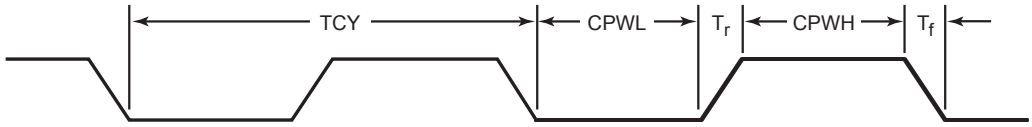

Figure 10. Clock Timing

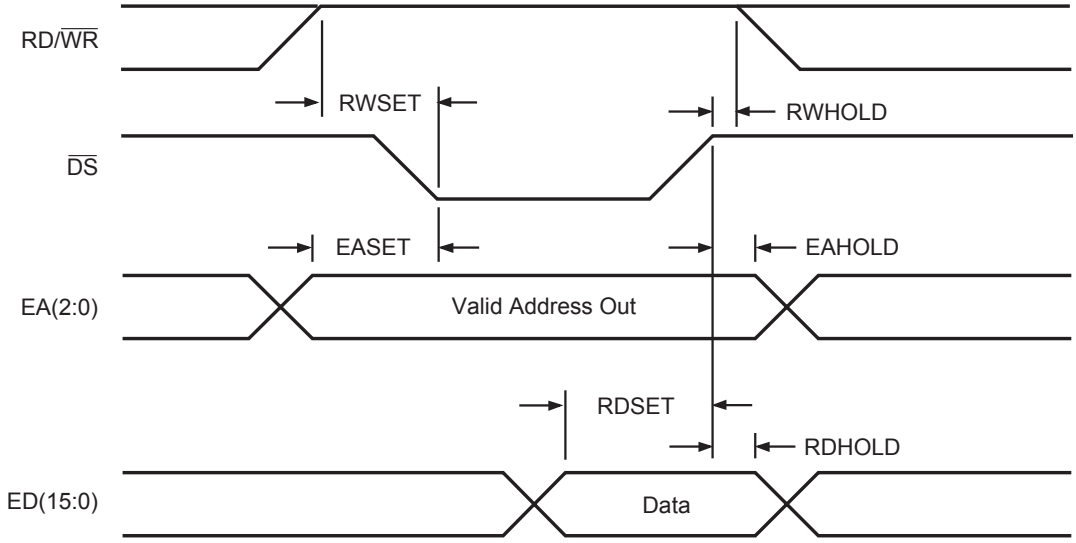

Figure 11. Read Timing

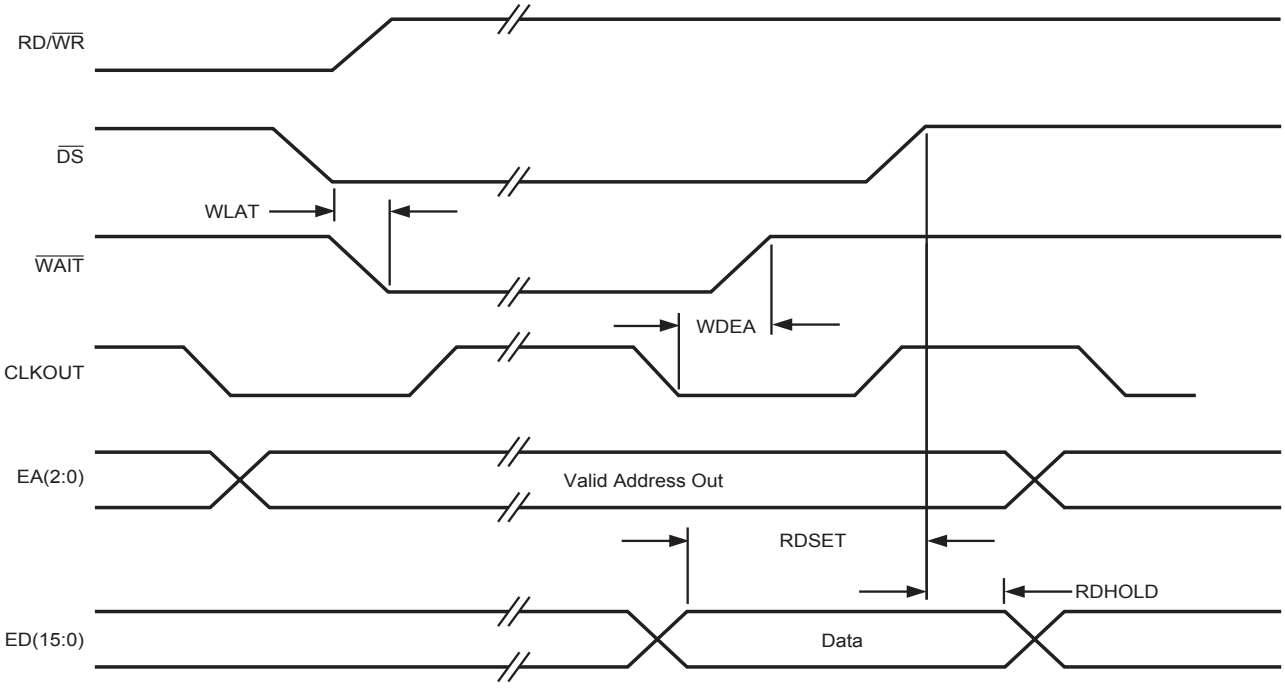

Figure 12. Read Timing Using $\overline{WAIT}$ Pin

FUNCTIONAL DESCRIPTION

Instruction Timing. Most instructions are executed in one machine cycle. A multiplication or multiply/accumulate instruction requires a single cycle. Long immediate instructions, and Jump or Call instructions, are executed in two machine cycles. Specific instruction cycle times are described in the Instruction Description section.

Multiply/Accumulate. The multiplier can perform a 16-bit x 16-bit multiply, or multiply/accumulate, in one machine cycle using the Accumulator and/or both the X and Y inputs. The multiplier produces a 32-bit result, however, only the 24 most significant bits are saved for the next instruction or accumulation. For operations on very small numbers where the least significant bits are important, the data should first be scaled to avoid truncation errors.

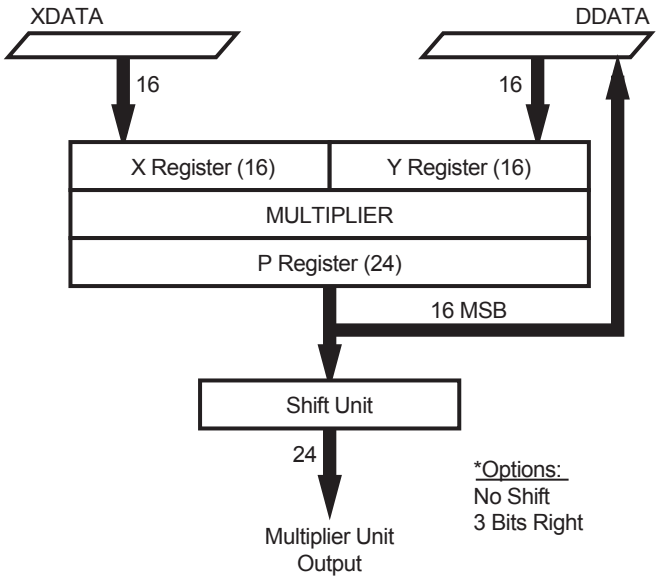

Figure 16. Multiplier Block Diagram

All inputs to the multiplier should be fractional two's-complement, 16-bit binary numbers, which places them in the range [–1 to 0.9999695]. The result is in 24 bits, so the range is [–1 to 0.9999999].

If 8000H is loaded into both the X and Y registers, the multiplication produces an incorrect result. Positive one cannot be represented in fractional notation, and the multiplier actually yields the result 8000H x 8000H = 8000H (–1 x –1 = –1). The user should avoid this case to prevent erroneous results.

A shifter between the P Register and the Multiplier Unit Output can shift the data by three bits right or no shift.

Data Bus Bank Switch. There is a switch that connects the X Bus to the DDATA Bus that allows both the X and Y registers to be loaded with the same operand for a one cycle squaring operation. The switch is also used to read the X register.

ALU. The ALU features two input ports. One is connected to the output of the 24-bit Accumulator. The other input selects either the Multiplier Unit Output or the 16-bit DDATA bus (left-justified with zeros in the eight LSBs). The ALU performs arithmetic, logic, and shift operations.

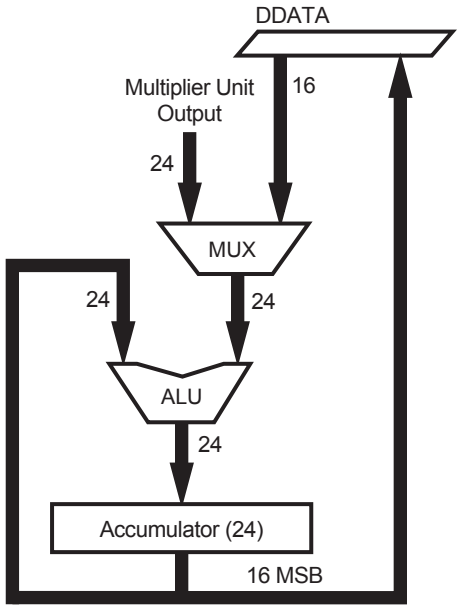

Figure 17. ALU Block Diagram

Hardware Stack. A six-level hardware stack is connected to the DDATA bus to hold subroutine return addresses or data. The CALL instruction pushes PC+2 onto the stack, and the RET instruction pops the contents of the stack to the PC.

User Inputs and Outputs. The Z893x3 features three User Inputs, UI0, UI1, and UI2. Pins UI0 and UI1 are connected directly to status register bits S10 and S11, and can be read, or used as a condition code in any conditional instruction. Pins UI0, UI1 and UI2 may also be used to clock the Counter/Timers. There are two user output bits, UO0 and UO1, which share pins with the timer outputs TMO0 and TMO1 on Port2. When the User Outputs are enabled, they are the complements of bits S5 and S6 of the Status Register.

I/O PORTS

I/O pin allocation of ports for the different package types is designed to provide configuration flexibility. Each port line of Ports 0, 1, and 2 can be independently selected as an input or an output. Each port's output lines can be globally selected as push-pull or as open-drain outputs

Table 15. I/O Port Bit Allocations

Device Pins	44-Pin PLCC, 44-Pin PQFP	64-Pin TQFP, 68-Pin PLCC	80-Pin PQFP
P0 MSB	ED15–ED8, or P0.15–P0.8, or P1.7–P1.0	ED15–ED8, or P0.15–P0.8	ED15–ED8, or P0.15–P0.8
P0 LSB	ED7–ED0, or P0.7–P0.0	ED7–ED0, or P0.7–P0.0	ED7–ED0, or P0.7–P0.0
P1		P1.7–P1.0	P1.7–P1.0
P2	P2.4–P2.0	P2.7–P2.0	P2.7–P2.0
P3			P3.7–P3.0

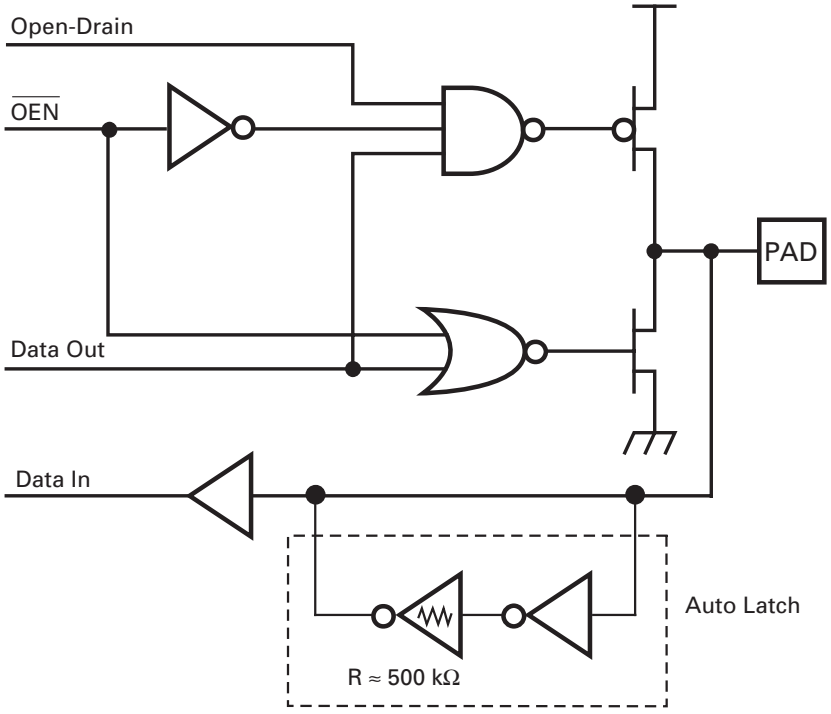

Figure 24. Port 0, 1 and 2 Configuration

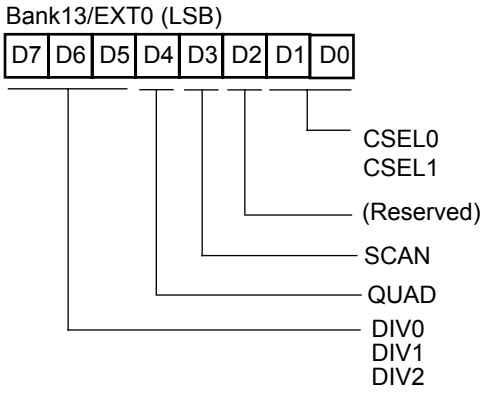

Figure 29. ADCTL Register (LSB)

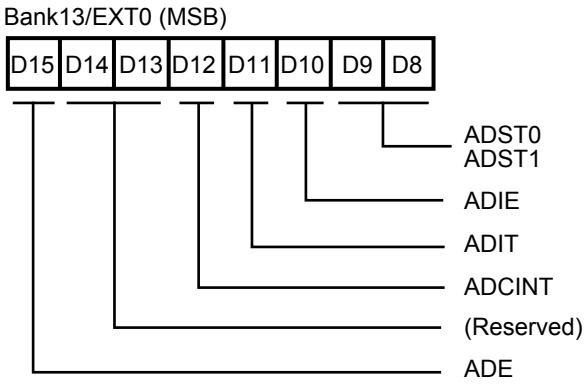

Figure 30. ADCTL Register (MSB)

Table 18. A/D Prescaler Values (Bits 7, 6, 5)

DIV2	DIV1	DIV0	A/D Prescaler (Crystal divided by)
0	0	0	8
0	0	1	16
0	1	0	24
0	1	1	32
1	0	0	40
1	0	1	48
1	1	0	56
1	1	1	64

Table 19. Operating Modes (Bits 4, 3)

QUAD	SCAN	Option
0	0	Convert selected channel 4 times, then stop
0	1	Convert selected channel, then stop.
1	0	Convert 4 channels, then stop.
1	1	Convert 4 channels continuously.

Table 20. Channel Select (Bits 1, 0)

CSEL1	CSEL0	Channel
0	0	AN0
0	1	AN1
1	0	AN2
1	1	AN3

ADE (Bit 15). A "0" disables any A/D conversions or accessing any A/D registers, except writing to the ADE bit. A "1" enables all A/D accesses.

Reserved (Bits 14, 13). Reserved for future use.

ADCINT (Bit 12). The A/D interrupt bit is read-only. The ADCINT will reset every time this register is written.

ADIT (Bit 11). Selects when to set the A/D interrupt if interrupts are enabled (ADIE=1). A value of "0" sets the interrupt after the first A/D conversion is complete. A value of "1" sets the interrupt after the fourth A/D conversion is complete.

ADIE (Bit 10). A/D Interrupt Enable. A value of "0" disables the A/D Interrupt. A value of "1" enables the A/D Interrupt.

Table 21. START (Bits 9, 8)

ADST1	ADST0	Option
0	0	Conversion starts when this register is written.
0	1	Conversion starts on INT1 per Interrupt Allocation Register
1	0	Conversion starts on C/T2 time-out.
1	1	Conversion starts on C/T0 time-out.

There are four A/D result registers. See the EXT Register Assignments for their location in the different banks.

PERIPHERALS (Continued)

Counter/Timers (C/T0 and C/T1)

The Z893x3 features two 16-bit Counter/Timers (C/T) that can be independently configured to operate in various modes. Each is implemented as a 16-bit Load Register and a 16-bit down counter. Either C/T input can be selected from UI0 or UI1. Either C/T output can be directed to TMO0 or TMO1. The C/T clock is a scaled version of the system clock. Each C/T features an 8-bit prescaler. The clock rates of the two C/T are independent of each other. The C/Ts can be programmed to recognize clock events on the rising edge, the falling edge, or both rising and falling edges of the input signal. Outputs on TMO0 or TMO1 can be programmed to occur with either polarity.

If either C/T is enabled and an output pin TMO0 or TMO1 is selected, and at the same time User Outputs are enabled, the C/T takes precedence, and Status Register bits 5 or 6 do not affect the state of the selected pin.

C/T Modes of Operation:

MODE 0—Square Wave Output. The C/T is configured to generate a continuous square wave of 50% duty cycle. Writing a new value to the TMLR Register takes effect at the end of the current cycle, unless TMR is written.

MODE 1—Retriggerable One-Shot. The C/T is configured to generate a single pulse of programmable duration. The pulse may be either logic High or logic Low. Retriggering the one-shot before the end of the pulse causes it to retrigger for a new duration.

MODE 2—8-Bit PWM. The C/T is configured to generate a pulse-width modulated waveform. The duty cycle ranges from 0–100% (0/256 to 255/256; 8-bits) of a cycle in steps of 1/256 of a cycle. The asserted state of the waveform may be either logic High or logic Low. Writing a new pulse-width value to the TMLR Register takes effect at the end of current cycle, unless TMR is written.

MODE 3—16-Bit PWM. The C/T is configured to generate a pulse-width modulated waveform. The duty cycle ranges from 0–100% (0/65,536 to 65,535/65,536; 16-bits) of a cycle in steps of 1/65,536 of a cycle. The asserted state of the waveform may be either logic High or logic Low. Writing a new pulse-width value to the TMLR Register takes effect at the end of current cycle, unless TMR is written.

MODE 4—Finite Pulse String Generator. The C/T is configured to generate 1 to 65,535 pulses. The output pulses are actually from the Timer Clock Prescaler divided by 2 (TMCLK). They are gated to the output until the Timer Down-Counter underflows.

MODE 5—Externally Clocked One-Shot. The C/T is configured to generate an output pulse. The pulse may be either logic High or logic Low. It is deasserted when a programmable number of input events (up to 65,535) occur on the input pin, UI0 or UI1.

MODE 6—Software Watch-Dog Timer. The C/T is configured to generate a Hardware Reset on time-out, unless retriggered by software.

MODE 7—Hardware Watch-Dog Timer. The C/T is configured to generate a Hardware Reset on time-out unless retriggered by an event on the input pin, UI0 or UI1.

MODE 8—Pulse Stopwatch. The C/T is configured to measure the time during which its input is asserted.

MODE 9—Edge-to-Edge Stopwatch. The C/T is configured to measure the period from one rising (falling) edge to the next rising (falling) edge on the input.

MODE 10—Edge Counter. The C/T is configured to count a number of input edges (up to 65,535). Input edges may be selected as rising or falling or both.

MODE 11—Gated Edge Counter. The C/T is configured to count the number of input edges (up to 65,535) in a time window set by the second timer. Edges are counted until the second timer underflows. Input edges may be selected as rising, falling, or both.

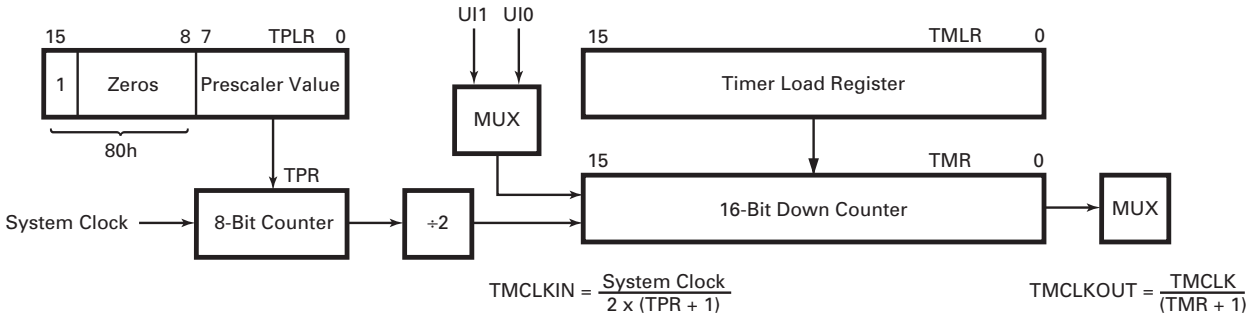

Figure 31. Counter/Timer 0 and 1 Block Diagram

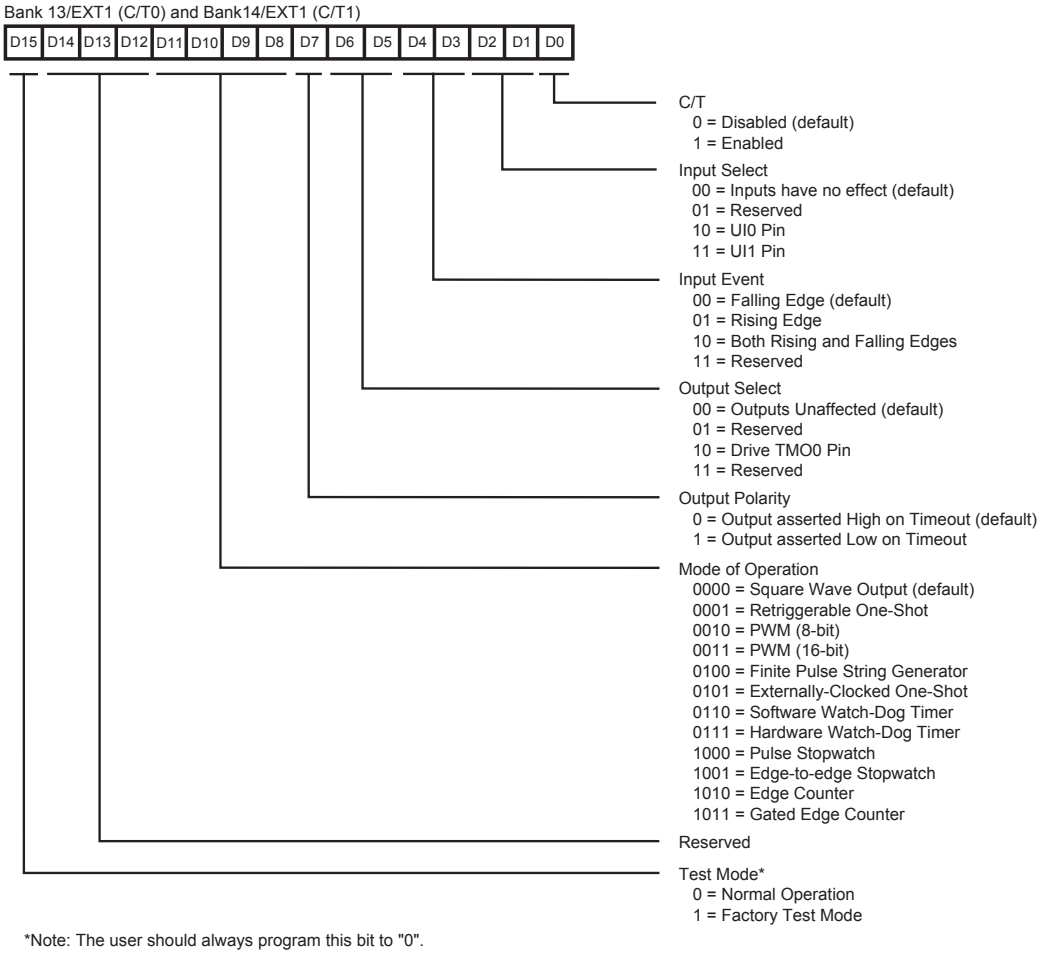

Figure 32. C/T0 and C/T1 Control Register

C/T Registers

Each C/T contains a set of five 16-bit Registers. Bank13 is used to access the registers for C/T0 and Bank14 is for the C/T1 registers. All accesses to C/T Registers occur with zero wait states.

Counter/Timer Control Register (Bank13,14/EXT1). The C/T Control register enables/disables the C/T, selects input and output options, and the mode of operation.

TMLR—Load Register (Bank13,14/EXT2). The 16-bit TMLR register holds the value that is loaded into TMR when TMR underflows.

TMR—Counter Register (Bank13,14/EXT3). TMR is a 16-bit down counter that holds the current C/T value. It can be read like any other ordinary register. However, writing to TMR is different than writing to an ordinary register. A write to TMR causes the contents of TMLR to be written into TMR, causing the C/T to be retriggered.

TPLR—Prescaler Load Register (Bank13,14/EXT4). The 16-bit TPLR register holds the prescaler load value in its lower 8 bits. Bit 15 must be written with a “1”, and bits 14–8 must be written with “0’s”.

Note: If the C/T interrupt is being used, this register must be re-written at the end of the interrupt service routine in order to enable the next interrupt. The number of clock cycles from the beginning of the interrupt service routine to the write must exceed the prescaler load value.

PERIPHERALS (Continued)

TPR—Prescaler Register (Bank13,14/EXT5). TPR is an 8-bit down counter that holds the current Prescaler Count Value. It can be read like any other ordinary register. However, writing to TPR is different than writing to an ordinary register. A write to TPR causes the lower 8-bit contents of TPLR to be written into TPR, causing the Prescaler to be retriggered.

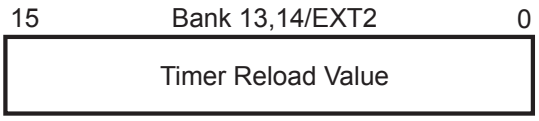

Figure 33. TMLR—Load Register

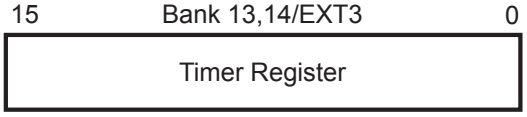

Figure 34. TMR—Counter Register

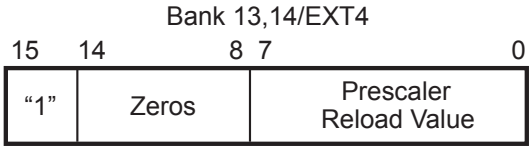

Figure 35. TPLR—Prescaler Load Register

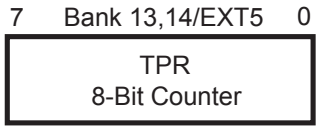

Figure 36. TPR—Prescaler Register

Prescaler Operation

The Prescaler section comprises TPLR and TPR, followed by a divide-by-two flip-flop. This operation generates a 50 percent duty cycle output, TMCLKIN. TPR's input clock is the system clock. The maximum prescaler output frequency is 1/2 the system clock frequency.

After TPR is loaded, it decrements at the system clock frequency and generates an output to the divide-by-two flip-flop. When the count reaches 0, the TPR counter is reloaded from the lower 8 bits of TPLR Register.

Two other events cause a reloading of the TPR counter:

1. Writing to TPR
2. Reloading TMR, which happens when TMR underflows, or when TMR is written.

Note: For C/T Modes 8–11, the external input signal on UI0 or UI1 is synchronized with TMCLKIN before being applied to TMR. The external input signal frequency must be no higher than 1/2 of the TMCLKIN frequency.

SYSTEM CLOCK GENERATOR

The System Clock can be generated from an external clock signal, or from the internal crystal oscillator. For the latter case, a 32-kHz crystal is used in conjunction with the internal crystal oscillator. The system clock generator includes a Phase-Locked Loop (PLL) circuit to derive a high-frequency System Clock from the low-frequency crystal oscillator. The benefits of using a low-frequency crystal are lower system cost, lower power consumption and lower EMI.

The Z893x3 supports several low-power clock modes to optimize power consumption. Total power consumption depends on System Clock frequency, and which oscillators and peripherals are enabled.

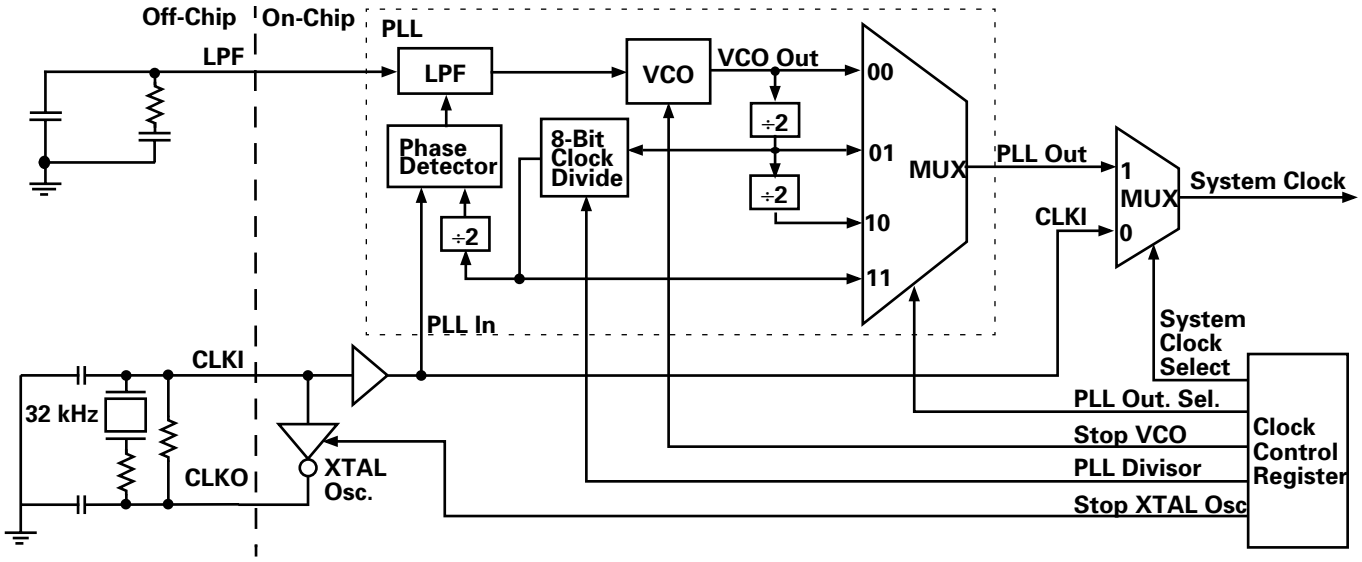

Figure 42. System Clock Generator

Modes of Operation

The various modes of clock operation are selected by writing to the appropriate bits and fields of the Clock Control Register, Bank15/EXT5. The mode of operation can be switched dynamically during program execution.

Power-up and Reset (Default)

At power-up, and following a reset or Sleep Mode Recovery, System Clock Select = 0, therefore system clock = CLKI. The XTAL Oscillator is running, so CLKI may be provided by a crystal, as depicted, or by an external clock (not shown). The VCO is running to minimize the time required to switch the system clock to PLL Out.

External Clock Direct

In this mode, an external clock on CLKI provides the System Clock. CLKO is not connected. System Clock Select = 0. The PLL is not used. The XTAL oscillator and VCO are both stopped to reduce power consumption.

Crystal Oscillator DIrect

In this mode of operation, the XTAL Oscillator is running, and an external crystal provides a 32-kHz (typical) clock at CLKI. System Clock Select = 0, so the System Clock is the frequency at CLKI (32 kHz). This mode requires less power than running at a high-frequency clock rate. The VCO may be stopped to conserve even more power, or left running for rapid switching (wake up) to a high-frequency PLL generated clock. Whenever the PLL circuit is enabled, Stop VCO = 0, and a software delay of 10 ms must be observed before switching System Clock from CLKI to PLL Out. As a result, the PLL has time to stabilize.

PLL Clock

An external 32-kHz crystal, together with the on-chip XTAL oscillator, provides the PLL input. The VCO generates the System Clock. A low-pass filter must be connected to LPF as depicted. The XTAL oscillator and VCO are both running, and System Clock = PLL Out (System Clock Select = 1). The frequency generated by the PLL is deter-

INSTRUCTION SET

The addressing modes are:

<pregs>, <hwregs>. These modes are used for loads to and from registers within the chip, such as loading to the accumulator, or loading from a pointer register. The names of the registers are specified in the operand field (destination first, then source).

<dregs>. This mode is used for access to the lower 16 addresses in each bank of RAM. The 4-bit address comes from 2 bits of the status register and 2 bits of the operand field of the data pointer. Data registers can be used to access data in RAM, but typically are used as pointers to access data from the program memory.

<accind>. Similar to the previous mode, the address for the program memory read is stored in the Accumulator. Hence, @A in the second operand field loads the number in memory specified by the address in A.

<direct>. The direct mode allows read or write to data RAM from the Accumulator by specifying the absolute address of the RAM in the operand of the instruction. A number between 0 and 255 indicates a location in RAM bank 0, and a number between 256 and 511 indicates a location in RAM bank 1.

<limm>. This address mode indicates a long immediate operand. A 16-bit word can be loaded directly from the operand into the specified register or memory location.

<simm>. This address mode indicates a short immediate operand. It is used to load 8-bit data into the specified RAM pointer.

<regind>. This mode is used for indirect access to the data RAM. The address of the RAM location is stored in the pointer. The "@" symbol indicates "indirect" and precedes the pointer. For example, @P1:1 refers to the location in RAM bank 1 specified by the value in the pointer.

<memind>. This mode is used for indirect access to the program memory. The address of the memory is located in a RAM location, which is specified by the value in a pointer. Therefore, @@P1:1 instructs the processor to read from a location in memory, which is specified by a value in RAM, and the location of the RAM is in turn specified by the value in the pointer.

Note: the data pointer can also be used for a memory access in this manner, but only one "@" precedes the pointer. In both cases, each time the addressing mode is used, the memory address stored in RAM is incremented by one to allow easy transfer of sequential data from program memory.

Table 24. Instruction Set Addressing Modes

Symbolic Name	Syntax	Description
<pregs>	Pn:b	Pointer Registers
<dregs> (points to RAM)	Dn:b	Data Registers
<hwregs>	X, Y, PC, SR, P, EDn, A, BUS	Hardware Registers
<accind> (points to Program Memory)	@A	Accumulator Memory Indirect
<direct>	<expression>	Direct Address Expression
<limm>	#<const exp>	Long (16-bit) Immediate Value
<simm>	#<const exp>	Short (8-bit) Immediate Value
<regind> (points to RAM)	@Pn:b	Pointer Register Indirect
	@Pn:b+	Pointer Register Indirect with Increment
	@Pn:b–LOOP	Pointer Register Indirect with Loop Decrement
	@Pn:b+LOOP	Pointer register Indirect with Loop Increment
<memind> (points to Program Memory)	@@Pn:b	Pointer Register Memory Indirect
	@Dn:b	Data Register Memory Indirect
	@@Pn:b–LOOP	Pointer Register Memory Indirect with Loop Decrement
	@@Pn:b+LOOP	Pointer Register Memory Indirect with Loop Increment
	@@Pn:b+	Pointer Register Memory Indirect with Increment

INSTRUCTION DESCRIPTIONS (Continued)

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
XOR	Bitwise exclusive OR	XOR <dest>,<src>	A,<pregs>	1	1	XOR A,P2:0
			A,<dregs>	1	1	XOR A,D0:1
			A,<limm>	2	2	XOR A,#13933
			A,<memind>	1	3	XOR A,@@P2:1+
			A,<direct>	1	1	XOR A,%2F
			A,<regind>	1	1	XOR A,@P2:0
			A,<hwregs>	1	1	XOR A,BUS
			A,<simm>	1	1	XOR A, #%12

Bank Switch Operand. The third (optional) operand of the MLD, MPYA and MPYS instructions represents whether the bank switch is set to ON or OFF. To illustrate, the keywords ON and OFF are used to state the direction of the switch. These keywords are referenced in the instruction descriptions through the <bank switch> symbol. The most notable capability is that a source operand can be multiplied by itself (squared).

ORDERING INFORMATION

Package Type	ROM	OTP
44-Pin PLCC	Z8922320VSC	Z8927320VSC
	Z8922320VEC	
44-Pin PQFP	Z8922320FSC	
	Z8922320FEC	
64-Pin TQFP	Z8932320ASC	Z8937320ASC
	Z8932320AEC	
68-Pin PLCC	Z8932320VSC	Z8937320VSC
	Z8932320VEC	
80-Pin PQFP	Z8932320FSC	Z8937320FSC
	Z8932320FEC	

For fast results, contact your local ZiLOG sales office for assistance in ordering the part required.

CODES

Package	V = PLCC
	A = TQFP
	F = PQFP
Temperature	S = 0°C to +70°C
	E = –40°C to 85°C
Speed	20 = 20 MHz
Environmental	C = Plastic Standard

Example:

Z 89323 20 V S C is a Z89323, 20 MHz, PLCC, 0°C to +70°C, Plastic Standard Flow