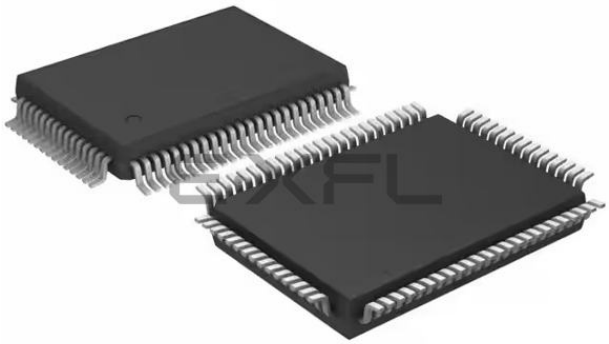

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	SPI, 3-Wire Serial
Clock Rate	20MHz
Non-Volatile Memory	OTP (16kB)
On-Chip RAM	1kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-PQFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8937320fsc00tr

Table 1. 44-Pin PLCC Z89223/273 Pin Description

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	P2.0/INT0	Port 2.0/Interrupt 0	Input/Output	23	AN2	A/D Input 2	Input
2	ED12/P0.12	External Data Bus/Port0	Input/Output	24	AN3	A/D Input 3	Input
3	ED13/P0.13	External Data Bus/Port0	Input/Output	25	P2.1/INT1	Port 2.1/Interrupt 1	Input/Output
4	ED14/P0.14	External Data Bus/Port0	Input/Output	26	AV_{CC}	Analog Power	
5	V_{SS}	Ground		27	V_{DD}	Power Supply	
6	ED15/P0.15	External Data Bus/Port0	Input/Output	28	RD/$\overline{WR}$	R/W External Bus	Output
7	ED3/P0.3	External Data Bus/Port0	Input/Output	29	EA0	Ext Address 0	Output
8	ED4/P0.4	External Data Bus/Port0	Input/Output	30	EA1	Ext Address 1	Output
9	V_{SS}	Ground		31	EA2	Ext Address 2	Output
10	ED5/P0.5	External Data Bus/Port0	Input/Output	32	P2.3/TMO1	Port 2.3/Timer Output 1	Input/Output
11	ED6/P0.6	External Data Bus/Port0	Input/Output	33	$\overline{DS}$	Ext Data Strobe	Output
12	ED7/P0.7	External Data Bus/Port0	Input/Output	34	P2.4/$\overline{WAIT}$	Port 2.4/Wait for ED	Input/Output
13	ED8/P0.8	External Data Bus/Port0	Input/Output	35	CLKI	Clock/Crystal In	Input
14	ED9/P0.9	External Data Bus/Port0	Input/Output	36	CLKO	Clock/Crystal Out	Output
15	V_{SS}	Ground		37	P2.2/TMO0	Port 2.2/Timer Output 0	Input/Output
16	ED10/P0.10	External Data Bus/Port0	Input/Output	38	LPF	PLL Low Pass Filter	Input
17	ED11/P0.11	External Data Bus/Port0	Input/Output	39	$\overline{RESET}$	Reset	Input
18	VAHI	Analog High Ref. Voltage	Input	40	V_{DD}	Power	
19	VALO	Analog Low Ref. Voltage	Input	41	ED0/P0.0	External Data Bus/Port0	Input/Output
20	AGND	Analog Ground		42	ED1/P0.1	External Data Bus/Port0	Input/Output
21	AN0	A/D Input 0	Input	43	ED2/P0.2	External Data Bus/Port0	Input/Output
22	AN1	A/D Input 1	Input	44	V_{SS}	Ground	

PIN CONFIGURATIONS (Continued)

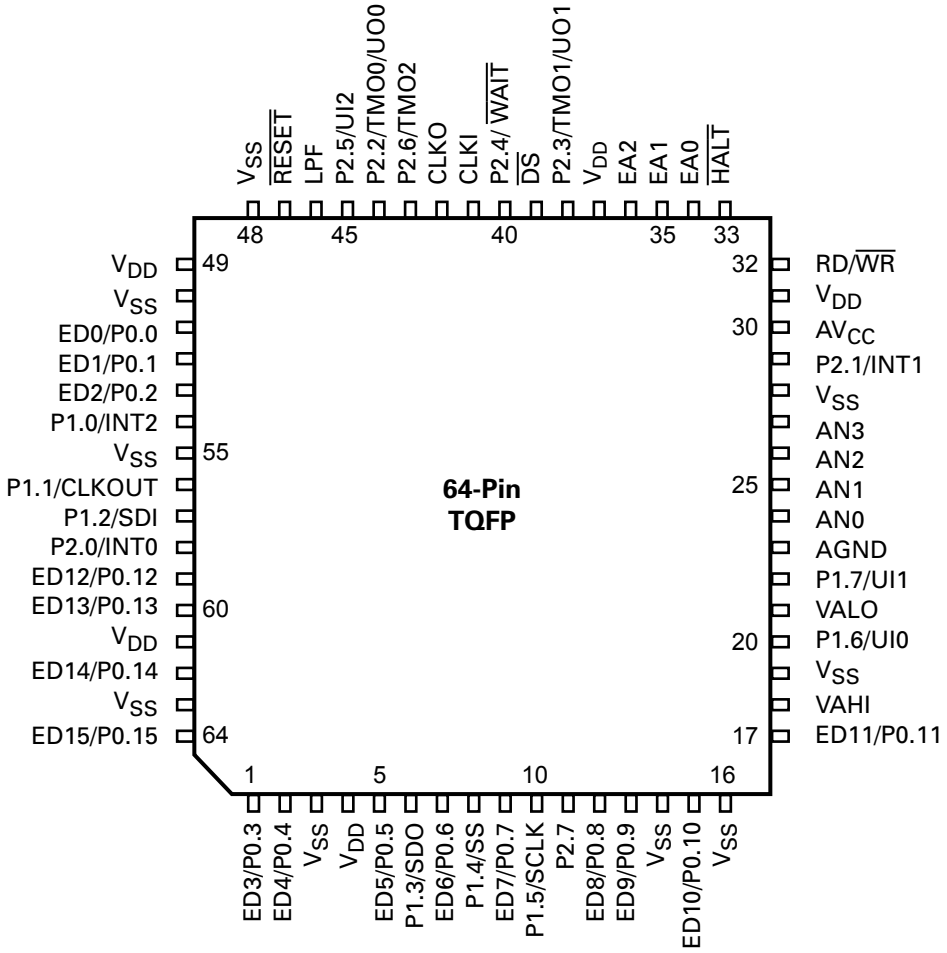


Figure 5. 64-Pin TQFP Z89323/373 Pin Configuration

Table 4. 68-Pin PLCC Z89323/373 Pin Description

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	P1.2/SDI	Port 1.2/Serial Input	Input/Output	35	AN0	A/D Input 0	Input
2	P2.0/INT0	Port 2.0/Interrupt 0	Input/Output	36	AN1	A/D Input 1	Input
3	ED12/P0.12	External Data Bus/Port0	Input/Output	37	AN2	A/D Input 2	Input
4	ED13/P0.13	External Data Bus/Port0	Input/Output	38	AN3	A/D Input 3	Input
5	V_{DD}	Power Supply		39	V_{SS}	Ground	
6	ED14/P0.14	External Data Bus/Port0	Input/Output	40	P2.1/INT1	Port 2.1/Interrupt 1	Input/Output
7	V_{SS}	Ground		41	AVCC	Analog Power	
8	ED15/P0.15	External Data Bus/Port0	Input/Output	42	V_{DD}	Power Supply	
9	NC	No Connection		43	RD/$\overline{WR}$	R/W External Bus	Output
10	NC	No Connection		44	$\overline{HALT}$	Halt Execution	Input
11	ED3/P0.3	External Data Bus/Port0	Input/Output	45	EA0	Ext Address 0	Output
12	ED4/P0.4	External Data Bus/Port0	Input/Output	46	EA1	Ext Address 1	Output
13	V_{SS}	Ground		47	EA2	Ext Address 2	Output
14	V_{DD}	Power Supply		48	NC	No Connection	
15	ED5/P0.5	External Data Bus/Port0	Input/Output	49	V_{DD}	Power Supply	
16	P1.3/SDO	Port 1.3/Serial Output	Input/Output	50	P2.3/TMO1	Port2.3/Timer Output 1	Input/Output
17	ED6/P0.6	External Data Bus/Port0	Input/Output	51	$\overline{DS}$	Ext Data Strobe	Output
18	P1.4/SS	Port 1.4/Slave Select	Input/Output	52	P2.4/$\overline{WAIT}$	Port 2.4/Wait for ED	Input/Output
19	ED7/P0.7	External Data Bus/Port0	Input/Output	53	CLKI	Clock/Crystal In	Input
20	P1.5/SCLK	Port 1.5/Serial Clock	Input/Output	54	CLKO	Clock/Crystal Out	Output
21	P2.7	Port 2.7	Input/Output	55	P2.6/TMO2	Port 2.6/Timer Output 2	Input/Output
22	ED8/P0.8	External Data Bus/Port0	Input/Output	56	P2.2/TMO0	Port 2.2/Timer Output 0	Input/Output
23	ED9/P0.9	External Data Bus/Port0	Input/Output	57	P2.5/UI2	Port 2.5/User Input 2	Input/Output
24	V_{SS}	Ground		58	LPF	PLL Low Pass Filter	Input
25	ED10/P0.10	External Data Bus/Port0	Input/Output	59	$\overline{RESET}$	Reset	Input
26	V_{SS}	Ground		60	V_{SS}	Ground	
27	ED11/P0.11	External Data Bus/Port0	Input/Output	61	V_{DD}	Power Supply	
28	V_{DD}	Power Supply		62	V_{SS}	Ground	
29	VAHI	Analog High Ref. Voltage	Input	63	ED0/P0.0	External Data Bus/Port0	Input/Output
30	V_{SS}	Ground		64	ED1/P0.1	External Data Bus/Port0	Input/Output
31	P1.6/UI0	Port 1.6/User Input 0	Input/Output	65	ED2/P0.2	External Data Bus/Port0	Input/Output
32	VALO	Analog Low Ref. Voltage	Input	66	P1.0/INT2	Port 1.0/Interrupt 2	Input/Output
33	P1.7/UI1	Port 1.7/User Input 1	Input/Output	67	V_{SS}	Ground	
34	AGND	Analog Ground		68	P1.1/CLKOUT	Port 1.1/Clock Output	Input/Output

Table 5. 80-Pin PQFP Z89323/373 Pin Description

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	NC	No Connection		41	RD/$\overline{WR}$	R/W External Bus	Output
2	ED15/P0.15	External Data Bus/Port0	Input/Output	42	P3.5	Port 3.5	Output
3	NC	No Connection		43	NC	No Connection	
4	NC	No Connection		44	$\overline{HALT}$	Halt Execution	Input
5	ED3/P0.3	External Data Bus/Port0	Input/Output	45	EA0	Ext Address 0	Output
6	P3.2	Port 3.2	Input	46	P3.6	Port 3.6	Output
7	ED4/P0.4	External Data Bus/Port0	Input/Output	47	EA1	Ext Address 1	Output
8	V_{SS}	Ground		48	EA2	Ext Address 2	Output
9	V_{DD}	Power Supply		49	NC	No Connection	
10	ED5/P0.5	External Data Bus/Port0	Input/Output	50	V_{DD}	Power Supply	
11	P1.3/SDO	Port 1.3/Serial Output	Input/Output	51	P2.3/TMO1	Port 2.3/Timer Output 1	Input/Output
12	ED6/P0.6	External Data Bus/Port0	Input/Output	52	$\overline{DS}$	Ext Data Strobe	Output
13	P1.4/SS	Port 1.4/Slave Select	Input/Output	53	P2.4/$\overline{WAIT}$	Port 2.4/Wait for ED	Input/Output
14	ED7/P0.7	External Data Bus/Port0	Input/Output	54	CLKI	Clock/Crystal In	Input
15	P1.5/SCLK	Port 1.5/Serial Clock	Input/Output	55	CLKO	Clock/Crystal Out	Output
16	P2.7	Port 2 7	Input/Output	56	P2.6/TMO2	Port 2.6/Timer Output 2	Input/Output
17	ED8/P0.8	External Data Bus/Port0	Input/Output	57	P2.2/TMO0	Port 2.2/Timer Output 0	Input/Output
18	ED9/P0.9	External Data Bus/Port0	Input/Output	58	P2.5/UI2	Port 2.5/User Input 2	Input/Output
19	V_{SS}	Ground		59	LPF	PLL Low Pass Filter	Input
20	P3.3	Port 3 3	Input	60	P3.7	Port 3.7	Output
21	ED10/P0.10	External Data Bus/Port0	Input/Output	61	$\overline{RESET}$	Reset	Input
22	V_{SS}	Ground		62	V_{SS}	Ground	
23	NC	No Connection		63	V_{DD}	Power Supply	
24	P3.4	Port 3.4	Output	64	NC	No Connection	
25	ED11/P0.11	External Data Bus/Port0	Input/Output	65	V_{SS}	Ground	
26	V_{DD}	Power Supply		66	P3.0	Port 3.0	Input
27	VAHI	Analog High Ref. Voltage	Input	67	ED0/P0.0	External Data Bus/Port0	Input/Output
28	V_{SS}	Ground		68	ED1/P0.1	External Data Bus/Port0	Input/Output
29	P1.6/UI0	Port 1 6/User Input 0	Input/Output	69	ED2/P0.2	External Data Bus/Port0	Input/Output
30	VALO	Analog Low Ref. Voltage	Input	70	P1.0/INT2	Port 1.0/Interrupt 2	Input/Output
31	P1.7/UI1	Port 1 7/User Input 1	Input/Output	71	V_{SS}	Ground	
32	AGND	Analog Ground		72	P1.1/CLKOUT	Port 1.1/Clock Output	Input/Output
33	AN0	A/D Input 0	Input	73	P1.2/SDI	Port 1.2/Serial Input	Input/Output
34	AN1	A/D Input 1	Input	74	P2.0/INT0	Port 2.0/Interrupt 0	Input/Output
35	AN2	A/D Input 2	Input	75	ED12/P0.12	External Data Bus/Port0	Input/Output
36	AN3	A/D Input 3	Input	76	ED13/P0.13	External Data Bus/Port0	Input/Output
37	V_{SS}	Ground		77	V_{DD}	Power Supply	
38	P2.1/INT1	Port 2.1/Interrupt 1	Input/Output	78	ED14/P0.14	External Data Bus/Port0	Input/Output
39	AV_{CC}	Analog Power		79	V_{SS}	Ground	
40	V_{DD}	Power Supply		80	P3.1	Port 3.1	Input

AC ELECTRICAL CHARACTERISTICS

Table 8. V_{DD}= 5V ±10%, T_A = 0°C to +70°C for "S" Temperature Range T_A = –40°C to +85°C for "E" temperature range, unless otherwise noted

Symbol	Parameter	Min [ns]	Max [ns]
Clock			
TCY	CLKI Cycle Time for user-supplied clock	50	31250
CPWH	CLKI Pulse Width High	21	
CPWL	CLKI Pulse Width Low	21	
Tr	CLKI Rise Time for 20-MHz user-supplied clock		2
Tf	CLKI Fall Time for 20-MHz user-supplied clock		2
External Peripheral Bus			
EASET	EA Setup Time to $\overline{DS}$ Fall	10	
EAHOLD	EA Hold Time from $\overline{DS}$ Rise	4	
RWSET	Read/Write Setup Time to $\overline{DS}$ Fall	10	
RWHOLD	Read/Write Hold Time from $\overline{DS}$ Rise	0	
RDSET	Data Read Setup Time to $\overline{DS}$ Rise	15	
RDHOLD	Data Read Hold Time from $\overline{DS}$ Rise	0	
WRVALID	Data Write Valid Time from $\overline{DS}$ Fall		5
WRHOLD	Data Write Hold Time from $\overline{DS}$ Rise	2	
Reset			
RRISE	Reset Rise Time		20 TCY
RWIDTH	Reset Low Pulse Width	2 TCY	
Interrupt			
IWIDTH	Interrupt Pulse Width	1TCY	
Halt			
HWIDTH	Halt Low Pulse Width	3 TCY	
Wait State			
WLAT	Wait Latency Time from $\overline{DS}$ Fall		7
WDEA	Wait Deassert Setup Time to CLKOUT Rise	TBD	
SPI			
SDI–SCLK	Serial Data In to Serial Clock Setup Time	10	
SCLK–SDO	Serial Clock to Serial Data Out Valid	15	
SS–SCLK	Slave Select to Serial Clock Setup Time	1/2 SCLK Period	
SS–SDO	Slave Select to Serial Data Out Valid	15	
SCLK–SDI	Serial Clock to Serial Data In Hold Time	10	

Interrupts. The Z893x3 features three user interrupt inputs which can be programmed to be positive or negative edge-triggered. There are five interrupts generated by internal peripherals: the A/D converter, the Serial Peripheral Interface, and the three Counter/Timers. Internally there are three priority levels. The internal signals for Interrupt service Requests are denoted ISR0, ISR1, and ISR2, with ISR0 having the highest priority, and ISR2 the lowest. The user can program which interrupt sources are enabled, and which sources are serviced by the highest, middle, and lowest priority service routines. An interrupt is serviced at the end of an instruction execution. Two machine cycles are required to enter an interrupt instruction sequence. The PC is pushed onto the stack. The Interrupt Controller fetches the address of the interrupt service routine from the following locations in program memory:

Device	ISR0	ISR1	ISR2
Z89223/273/323/373	1FFFH	1FFEH	1FFDH

At the end of the interrupt service routine, a RET instruction is used to pop the stack into the PC.

The Set-Interrupt-Enable-Flag (SIEF) instruction enables the interrupts. Interrupts are automatically disabled when entering an interrupt service routine. Before exiting an interrupt service routine the SIEF instruction can be used to reenable interrupts.

Registers. In addition to the internal registers for processing, control, and configuration, the Z893x3 offers up to seven user-defined 16-bit external registers, EXT0–EXT6, depending on the Register Bank Select value. The external register address space is shared by the Z893x3 internal peripherals. Selecting banks 0–4 of the EXT Register Assignment allows access to/from three to seven of these addresses for general-purpose use.

I/O Ports. The Z893X3 DSP family features a user-configurable I/O structure. Most of the I/O pins include dual functions. The Counter/Timer, Serial Peripheral Interface, and External Interrupt Enables determine whether a pin is dedicated to peripheral or I/O port use.

Port0. A 16-bit user I/O port. Bits can be configured as input or output or globally as open-drain output. When enabled, Port0 consumes the 16 data lines used by the ED bus. Port0 function and ED bus use can be dynamically alternated by enabling and disabling Port0.

Port1. A multifunctional 8-bit port. Bits can be configured as input or output or globally as open-drain output. Port1 also supports INT2, CLKOUT, the Serial Peripheral Interface, and User Inputs 0 and 1.

Port2. A multifunctional 8-bit port. Bits can be configured as input or output or globally as open-drain output. Port2 also supports INT0 and INT1, all three Counter/Timer outputs, ED Bus, $\overline{WAIT}$, and UI2.

Port3. Port3 is an 8-bit user I/O port with 4 bits of input and 4 bits of output. It is available only on the 80-pin package.

External Register Usage. The external registers EXT0–EXT6 are accessed using the External Address Bus EA2–EA0, the External Data Bus (ED Bus) ED15–ED0, and control signals $\overline{DS}$, $\overline{WAIT}$, and RD/$\overline{WR}$. These provide a convenient data transfer capability with external peripherals. Data transfers can be performed in a single-cycle. An internal wait state generator is provided to accommodate slower external peripherals. A single wait state can be implemented through control register Bank15/EXT3. For additional wait states, the $\overline{WAIT}$ pin can be used. The $\overline{WAIT}$ pin is monitored only during execution of a read or write instruction to external peripherals on the ED bus.

Wait-State Generator. An internal Wait-State generator is provided to accommodate slow external peripherals. A single Wait-State can be implemented through a control register. For additional states, a dedicated pin ($\overline{WAIT}$) can be held Low. The $\overline{WAIT}$ pin is monitored only during execution of a read or write instruction to external peripherals (ED bus).

Analog to Digital Converter. The A/D Converter is a 4-channel, 8-bit half-flash converter. Two external reference voltages provide a scalable input range. The A/D sample rate is determined by a prescaler connected to the system clock. An interrupt is optionally generated at the end of a conversion. The four input channels can be programmed to operate on demand, continuously, or upon an event (timer or interrupt).

Counter/Timers (C/T0 and C/T1). These C/Ts are 16-bit with 8-bit prescalers. They also offer the option of being used as PWM generators and include both hardware and software Watch-Dog capabilities. Both C/Ts are identical and can be externally or internally clocked. Either C/T can drive TMO0 or TMO1. Either C/T can drive any of the three interrupt service requests (ISR0, ISR1, or ISR2).

Counter/Timer (C/T2). This C/T is 16-bits, externally or internally clocked, and can drive TMO2 and/or any of the three interrupt service requests (ISR0, ISR1, or ISR2).

Serial Peripheral Interface (SPI). The Serial Peripheral Interface provides a convenient means of inter-processor and processor-peripheral communication. It offers the capability to transmit and receive simultaneously. The SPI is designed to operate in either master or slave mode.

BANK/EXT REGISTER ASSIGNMENTS (Continued)

Interrupt Status/Bank Select Register—EXT7

Following is a description of EXT7. It contains both a Bank Select Field and Interrupt Status Bits.

Bank Select Field. The four LSBs of EXT7 denote which bank is selected as the current working bank.

Interrupt Status Bits. These bits can be read to identify which interrupts are pending. A "1" denotes interrupt pending, and a "0" denotes no interrupt. This ability to identify interrupts is particularly useful in polled interrupt operation or when servicing ISR2, which may come from several sources.

Note: Write "1" to a particular status bit to clear that bit. Before exiting an interrupt service routine, the relevant interrupt bit(s) should be cleared. To clear a bit efficiently:

- Load the value of EXT7 into a register or memory location
- Then load that value back into EXT7

Performing these steps clear all of the interrupts that were pending, but leave the Register Bank Select unchanged.

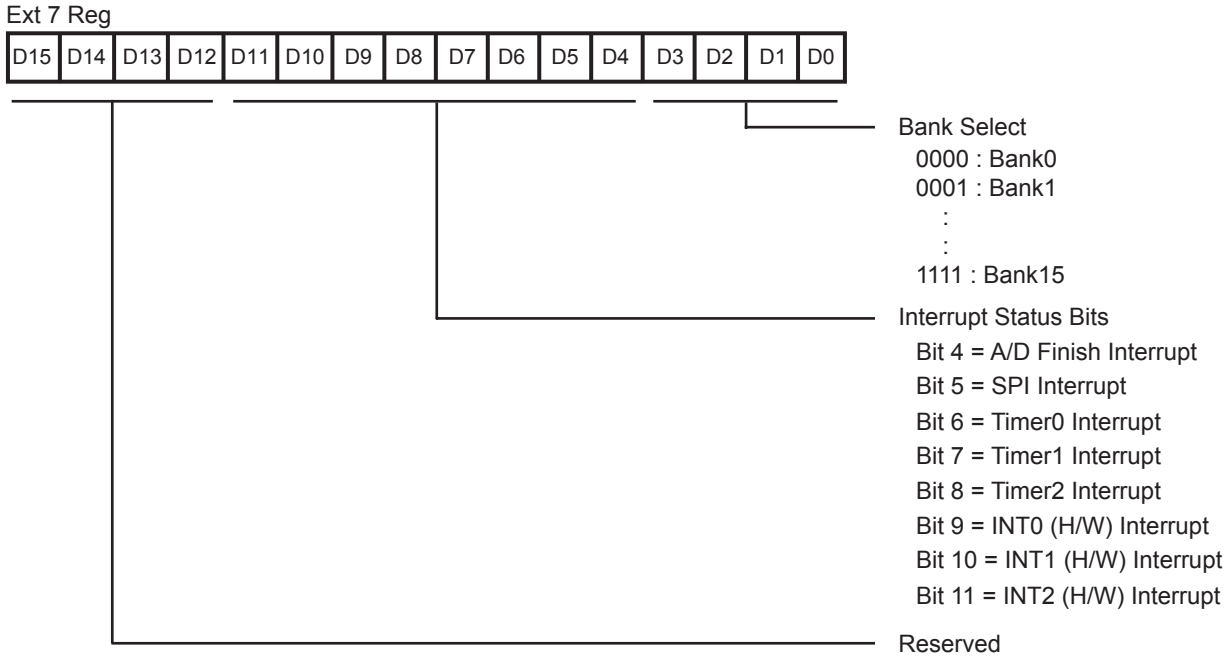


Figure 20. EXT7 Register

Interrupt Allocation Register—Bank15/EXT6

Bits 3–0 of the Interrupt Allocation Register define which unique interrupt source the highest priority, and is allocated to ISR0 (Interrupt Service Request 0).

Bits 7–4 of the Interrupt Allocation Register define which unique interrupt source has the second highest priority, and is allocated to ISR1 (Interrupt Service Request 1).

Bits 15–8 of the Interrupt Allocation Register are enable bits for common interrupt sources which have the lowest priority, and are all allocated to ISR2 (Interrupt Service Request 2). All the enabled interrupts which are not allocated to ISR0 or ISR1, are allocated to ISR2. When an ISR2 interrupt occurs, the interrupt service routine must read the Interrupt Status Register in EXT7 to determine the source. The Interrupt Status Register can be used for polling interrupts. An Interrupt that is not selected as a source to ISR0, ISR1, or ISR2, is disabled.

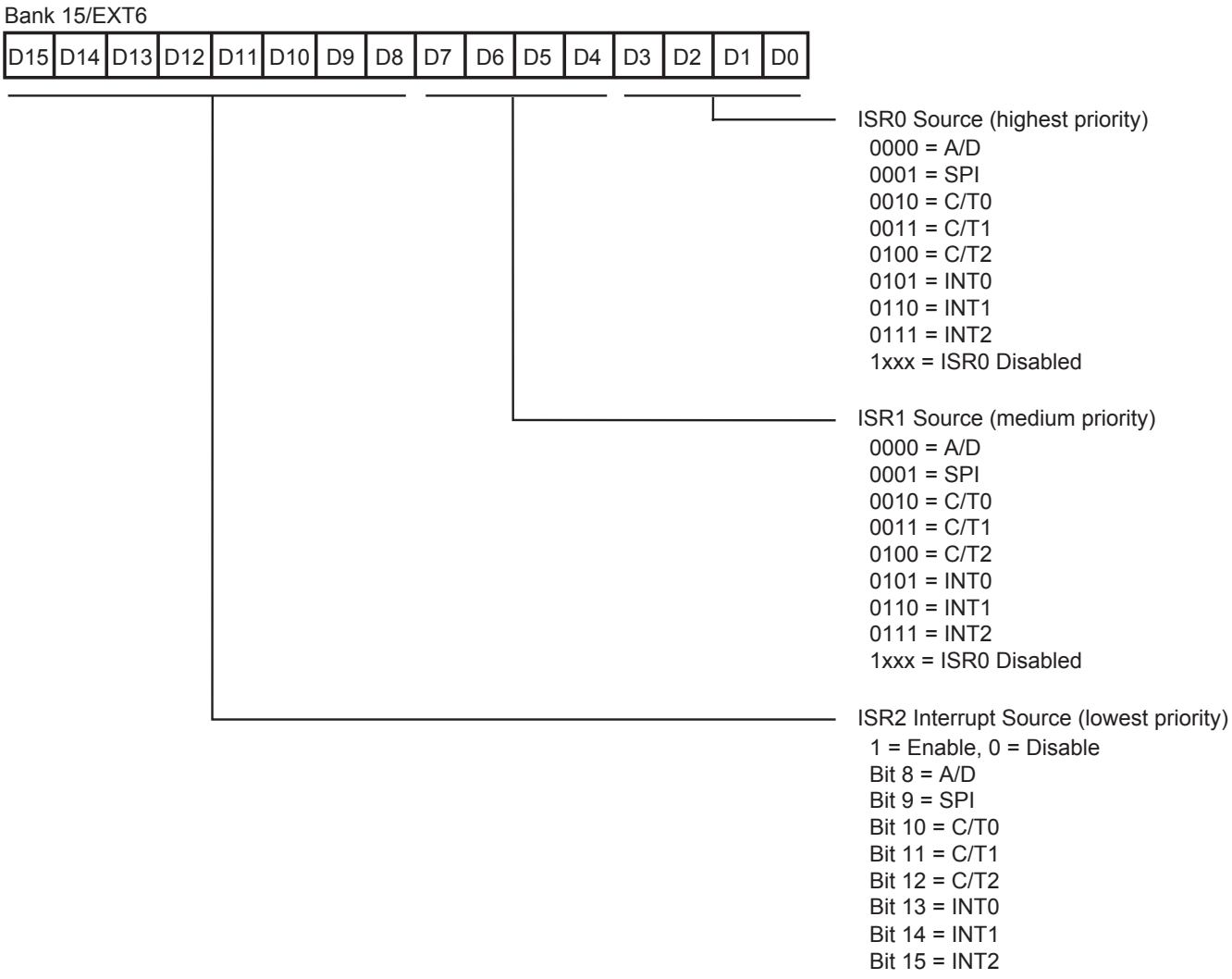


Figure 21. Interrupt Allocation Register

BANK/EXT REGISTER ASSIGNMENTS (Continued)

Interrupt Polarity Register—Bank14/EXT6

The trigger polarities, rising-edge or falling-edge, of all the external interrupts are programmable.

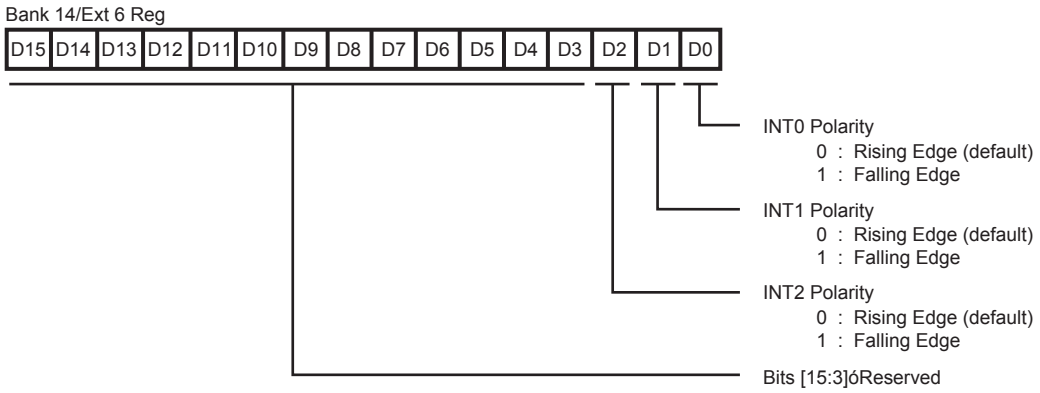


Figure 22. Interrupt Polarity Register

Wait-State Control Register—Bank15/EXT3

The Wait-State Control Register enables the insertion of wait states when the DSP accesses slow peripherals. This register enables the insertion of one wait state on the ED bus, providing 100 ns of access time instead of 50 ns when operating at 20 MHz. When more than one wait state is necessary, input pin P2.4/ $\overline{\text{WAIT}}$ can be used to provide additional wait states. The Wait-State Register enables the user to specify which EXT registers, EXT0–EXT6, and which operation, read and/or write, require a wait state. EXT7 is an internal register, and requires no wait state.

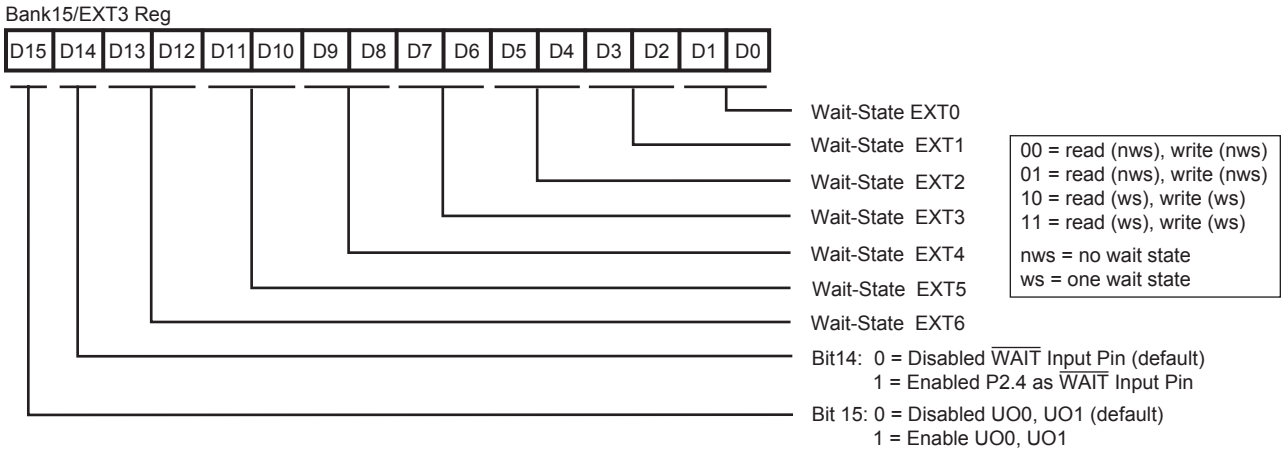


Figure 23. Wait-State Control Register

I/O PORTS

I/O pin allocation of ports for the different package types is designed to provide configuration flexibility. Each port line of Ports 0, 1, and 2 can be independently selected as an input or an output. Each port's output lines can be globally selected as push-pull or as open-drain outputs

Table 15. I/O Port Bit Allocations

Device Pins	44-Pin PLCC, 44-Pin PQFP	64-Pin TQFP, 68-Pin PLCC	80-Pin PQFP
P0 MSB	ED15–ED8, or P0.15–P0.8, or P1.7–P1.0	ED15–ED8, or P0.15–P0.8	ED15–ED8, or P0.15–P0.8
P0 LSB	ED7–ED0, or P0.7–P0.0	ED7–ED0, or P0.7–P0.0	ED7–ED0, or P0.7–P0.0
P1		P1.7–P1.0	P1.7–P1.0
P2	P2.4–P2.0	P2.7–P2.0	P2.7–P2.0
P3			P3.7–P3.0

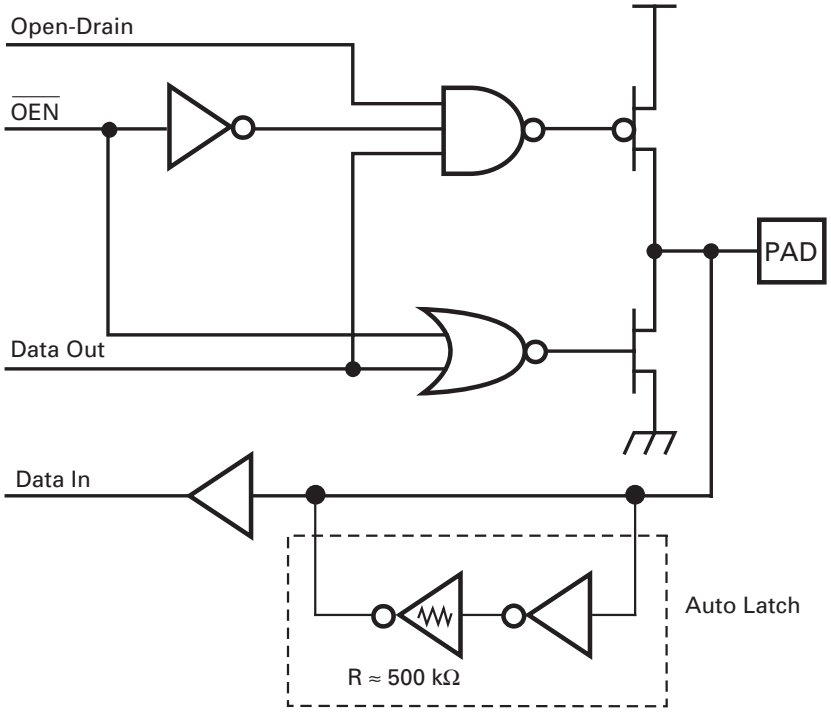


Figure 24. Port 0, 1 and 2 Configuration

I/O PORTS (Continued)

Port0—16-Bit Programmable I/O

Bank15/EXT0 is the Port0 direction control register. Bank15/EXT1 includes specific bits to enable and configure Port0. The Port0 data register is Ext4 in Banks 0, 1, or 5.

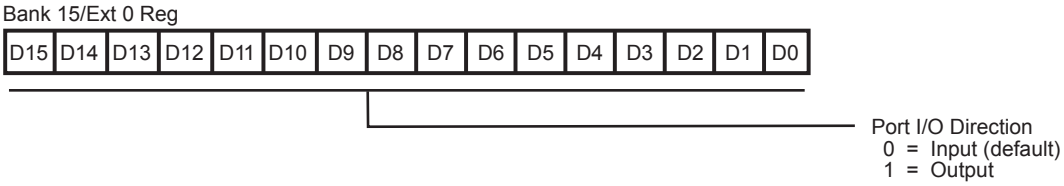


Figure 25. Port 0 Control Register

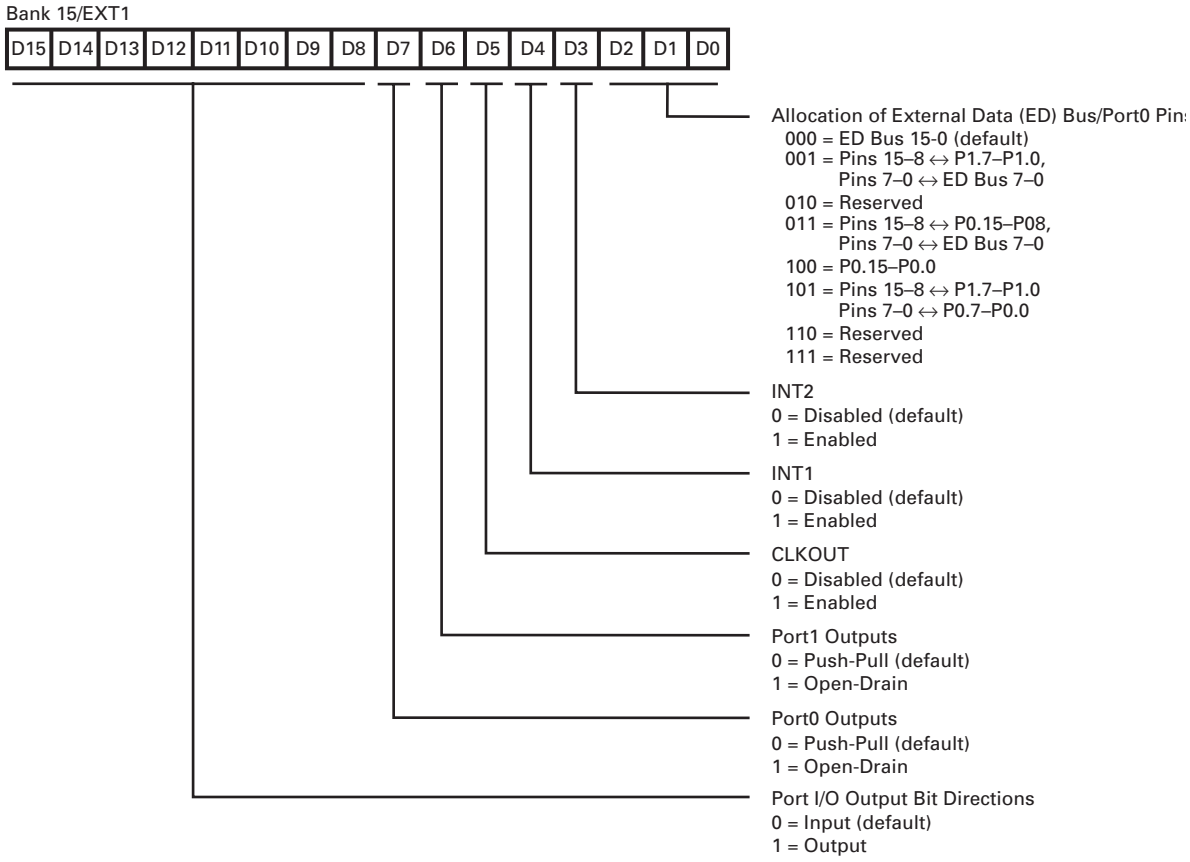


Figure 26. Bank15/EXT1 Register

PERIPHERALS

Analog to Digital Converter (A/D)

The A/D is a 4-channel 8-bit half-flash converter. It uses two reference resistor ladders, one for the upper 5 bits, and another for the lower 3 bits. Two external reference voltage input pins, VAHI and VALO, set the input voltage measurement conversion range. The converter is auto-zeroed prior to each sampling period. Bank13/EXT0 is the A/D control register.

The conversion time depends on the system clock frequency and the selection of the A/D prescaler value, bits DIV2–DIV0. The clock prescaler can be programmed to derive a 2 µs conversion time. For example, when deriving the A/D clock from a 20-MHz system clock, the A/D prescaler value should be set to divide by 40.

Bits ADST1–ADST0 determine one of the following start conversion options:

- Writing to the ADCTL control register
- ISR1
- C/T2 time-out
- C/T0 time-out

The start conversion operation may begin at any time. If a conversion is in progress, and a new start conversion signal is received, the conversion in progress will abort, and a new conversion will initiate.

Bits QUAD and SCAN determine one of the following Modes of operation:

- One channel is converted four times, with the results sequentially written to result registers 0, 1, 2 and 3.
- One channel is converted one time, with the respective result register updated.
- Four channels are converted one time each, with the respective four result registers updated.
- Four channels are converted repeatedly, with the respective four result registers constantly updated.

When one of the two four-channel modes is selected, the channel specified by CSEL1–CSEL0 will convert first. The other three channels will convert in sequence. In the sequence, AN0 follows AN3.

Bit ADIE enables the A/D to generate interrupts at the end of a conversion. Bit ADIT determines whether an interrupt occurs after the first or fourth conversion.

To reduce power consumption the A/D can be disabled by clearing the ADE bit.

Though the A/D will function with smaller input signals and reference voltages, the noise and offsets remain constant. The relative error of the converter will increase and the conversion time will also take longer.

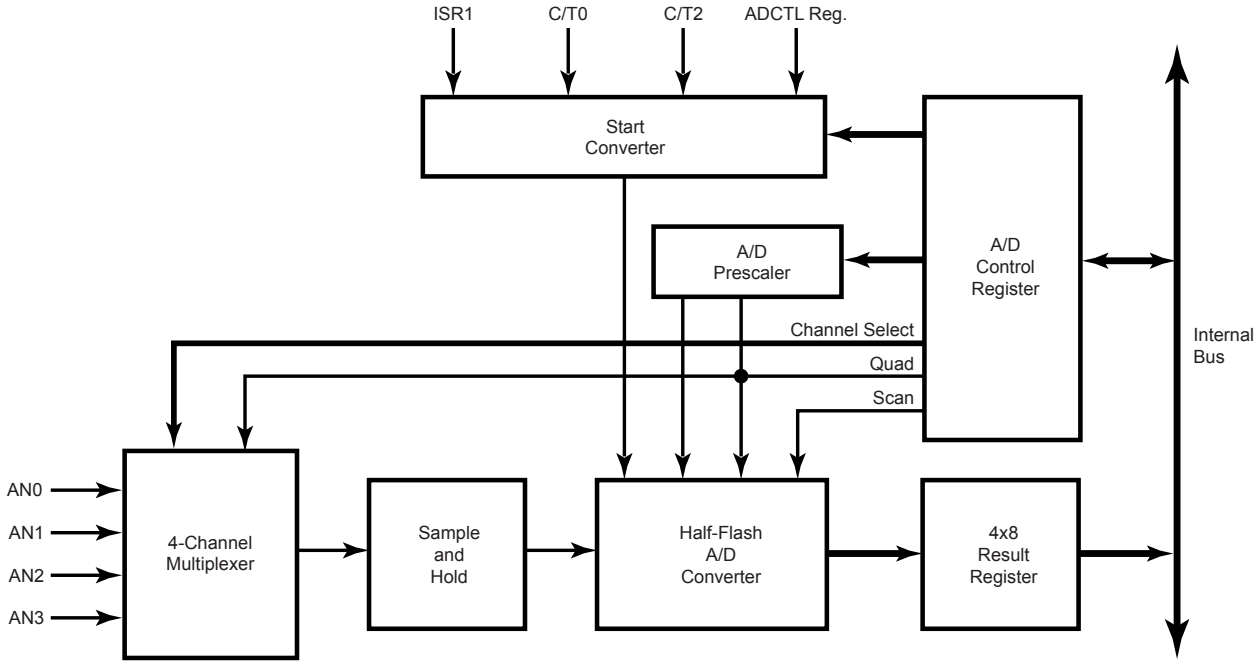


Figure 28. ADC Architecture

PERIPHERALS (Continued)

Counter/Timers (C/T0 and C/T1)

The Z893x3 features two 16-bit Counter/Timers (C/T) that can be independently configured to operate in various modes. Each is implemented as a 16-bit Load Register and a 16-bit down counter. Either C/T input can be selected from UI0 or UI1. Either C/T output can be directed to TMO0 or TMO1. The C/T clock is a scaled version of the system clock. Each C/T features an 8-bit prescaler. The clock rates of the two C/T are independent of each other. The C/Ts can be programmed to recognize clock events on the rising edge, the falling edge, or both rising and falling edges of the input signal. Outputs on TMO0 or TMO1 can be programmed to occur with either polarity.

If either C/T is enabled and an output pin TMO0 or TMO1 is selected, and at the same time User Outputs are enabled, the C/T takes precedence, and Status Register bits 5 or 6 do not affect the state of the selected pin.

C/T Modes of Operation:

MODE 0—Square Wave Output. The C/T is configured to generate a continuous square wave of 50% duty cycle. Writing a new value to the TMLR Register takes effect at the end of the current cycle, unless TMR is written.

MODE 1—Retriggerable One-Shot. The C/T is configured to generate a single pulse of programmable duration. The pulse may be either logic High or logic Low. Retriggering the one-shot before the end of the pulse causes it to retrigger for a new duration.

MODE 2—8-Bit PWM. The C/T is configured to generate a pulse-width modulated waveform. The duty cycle ranges from 0–100% (0/256 to 255/256; 8-bits) of a cycle in steps of 1/256 of a cycle. The asserted state of the waveform may be either logic High or logic Low. Writing a new pulse-width value to the TMLR Register takes effect at the end of current cycle, unless TMR is written.

MODE 3—16-Bit PWM. The C/T is configured to generate a pulse-width modulated waveform. The duty cycle ranges from 0–100% (0/65,536 to 65,535/65,536; 16-bits) of a cycle in steps of 1/65,536 of a cycle. The asserted state of the waveform may be either logic High or logic Low. Writing a new pulse-width value to the TMLR Register takes effect at the end of current cycle, unless TMR is written.

MODE 4—Finite Pulse String Generator. The C/T is configured to generate 1 to 65,535 pulses. The output pulses are actually from the Timer Clock Prescaler divided by 2 (TMCLK). They are gated to the output until the Timer Down-Counter underflows.

MODE 5—Externally Clocked One-Shot. The C/T is configured to generate an output pulse. The pulse may be either logic High or logic Low. It is deasserted when a programmable number of input events (up to 65,535) occur on the input pin, UI0 or UI1.

MODE 6—Software Watch-Dog Timer. The C/T is configured to generate a Hardware Reset on time-out, unless retriggered by software.

MODE 7—Hardware Watch-Dog Timer. The C/T is configured to generate a Hardware Reset on time-out unless retriggered by an event on the input pin, UI0 or UI1.

MODE 8—Pulse Stopwatch. The C/T is configured to measure the time during which its input is asserted.

MODE 9—Edge-to-Edge Stopwatch. The C/T is configured to measure the period from one rising (falling) edge to the next rising (falling) edge on the input.

MODE 10—Edge Counter. The C/T is configured to count a number of input edges (up to 65,535). Input edges may be selected as rising or falling or both.

MODE 11—Gated Edge Counter. The C/T is configured to count the number of input edges (up to 65,535) in a time window set by the second timer. Edges are counted until the second timer underflows. Input edges may be selected as rising, falling, or both.

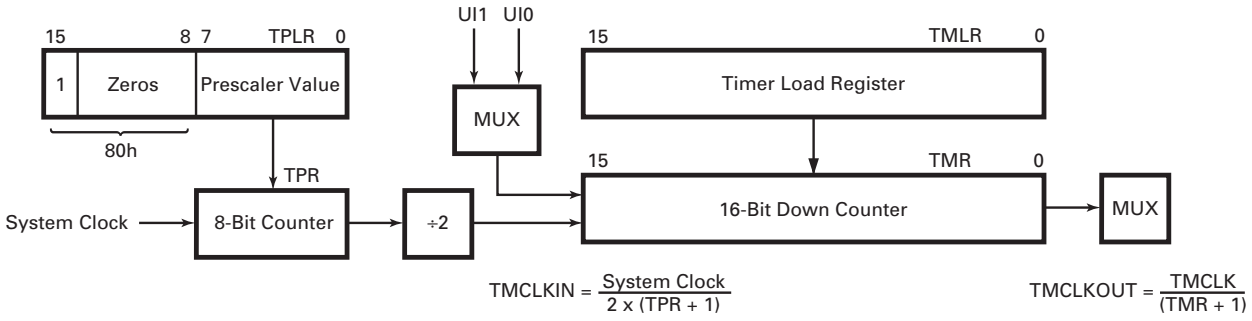


Figure 31. Counter/Timer 0 and 1 Block Diagram

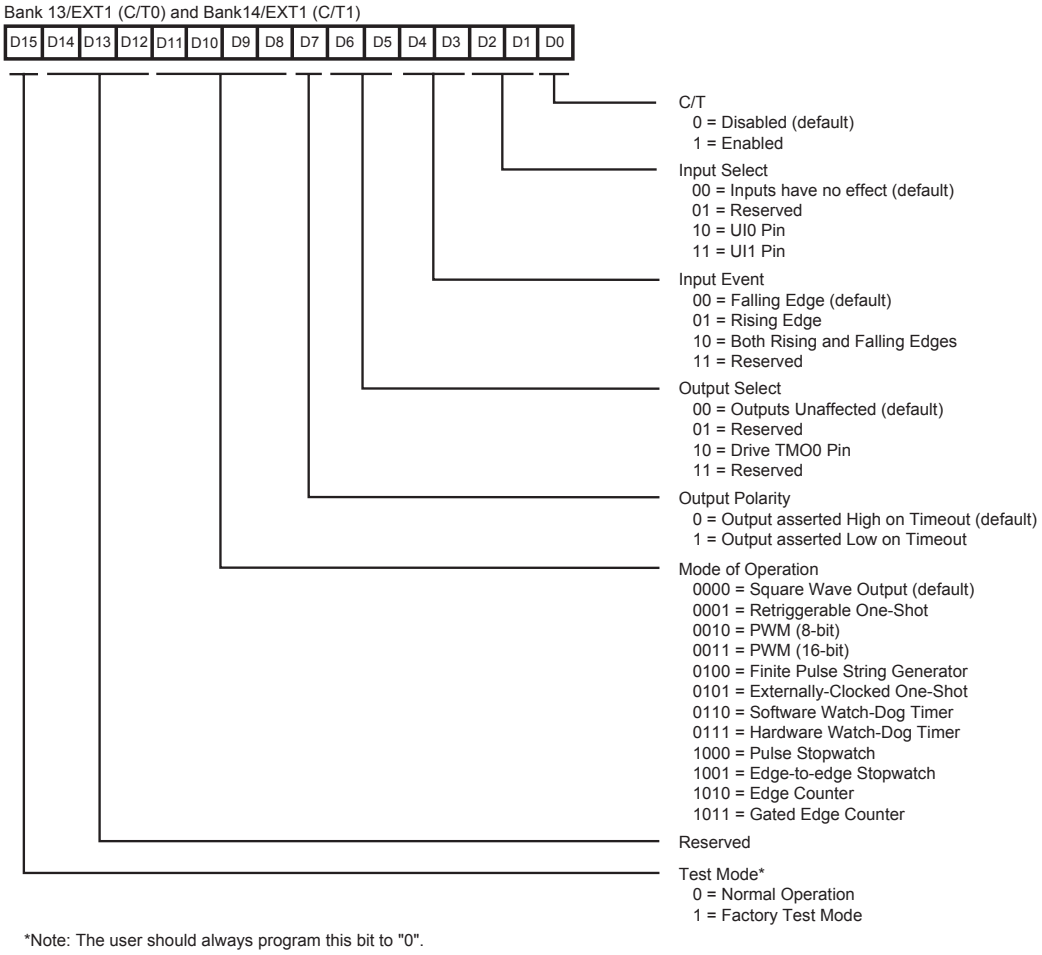


Figure 32. C/T0 and C/T1 Control Register

C/T Registers

Each C/T contains a set of five 16-bit Registers. Bank13 is used to access the registers for C/T0 and Bank14 is for the C/T1 registers. All accesses to C/T Registers occur with zero wait states.

Counter/Timer Control Register (Bank13,14/EXT1). The C/T Control register enables/disables the C/T, selects input and output options, and the mode of operation.

TMLR—Load Register (Bank13,14/EXT2). The 16-bit TMLR register holds the value that is loaded into TMR when TMR underflows.

TMR—Counter Register (Bank13,14/EXT3). TMR is a 16-bit down counter that holds the current C/T value. It can be read like any other ordinary register. However, writing to TMR is different than writing to an ordinary register. A write to TMR causes the contents of TMLR to be written into TMR, causing the C/T to be retriggered.

TPLR—Prescaler Load Register (Bank13,14/EXT4). The 16-bit TPLR register holds the prescaler load value in its lower 8 bits. Bit 15 must be written with a “1”, and bits 14–8 must be written with “0’s”.

Note: If the C/T interrupt is being used, this register must be re-written at the end of the interrupt service routine in order to enable the next interrupt. The number of clock cycles from the beginning of the interrupt service routine to the write must exceed the prescaler load value.

PERIPHERALS (Continued)

TPR—Prescaler Register (Bank13,14/EXT5). TPR is an 8-bit down counter that holds the current Prescaler Count Value. It can be read like any other ordinary register. However, writing to TPR is different than writing to an ordinary register. A write to TPR causes the lower 8-bit contents of TPLR to be written into TPR, causing the Prescaler to be retriggered.

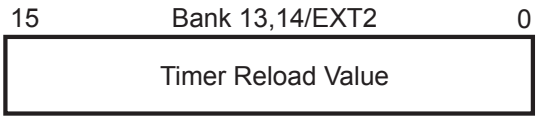


Figure 33. TMLR—Load Register

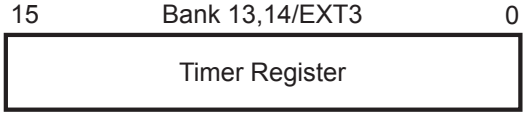


Figure 34. TMR—Counter Register

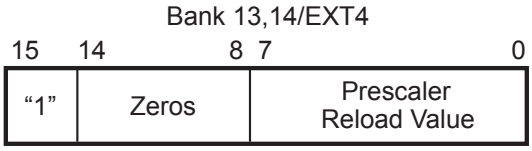


Figure 35. TPLR—Prescaler Load Register

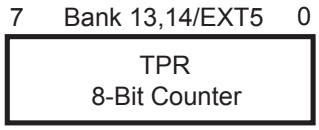


Figure 36. TPR—Prescaler Register

Prescaler Operation

The Prescaler section comprises TPLR and TPR, followed by a divide-by-two flip-flop. This operation generates a 50 percent duty cycle output, TMCLKIN. TPR's input clock is the system clock. The maximum prescaler output frequency is 1/2 the system clock frequency.

After TPR is loaded, it decrements at the system clock frequency and generates an output to the divide-by-two flip-flop. When the count reaches 0, the TPR counter is reloaded from the lower 8 bits of TPLR Register.

Two other events cause a reloading of the TPR counter:

1. Writing to TPR
2. Reloading TMR, which happens when TMR underflows, or when TMR is written.

Note: For C/T Modes 8–11, the external input signal on UI0 or UI1 is synchronized with TMCLKIN before being applied to TMR. The external input signal frequency must be no higher than 1/2 of the TMCLKIN frequency.

GENERAL-PURPOSE COUNTER/TIMER (C/T2)

This versatile16-bit C/T offers multiple uses, including Sleep Mode Wake-up. It can be clocked with the slow 32 kHz crystal clock (CLKI), while the DSP and other peripheral functions operate at a higher frequency generated by the PLL. Also included is an independent long duration timer.

GPT is a 16-bit down counter that holds the current C/T value. It can be read like any other ordinary register. GPTL and GPT share the same address, Bank14/EXT0. A write to GPTL reloads GPT, causing the C/T to be retriggered. When C/T2 underflows, it is reloaded with the most recent value written to GPTL. If the C/T2 interrupt is enabled, at underflow an interrupt is generated. The counting operation of the counter can be disabled. The C/T clock source can be selected to be CLKI, UI2, or the system clock divided by 2. When the C/T2 output is enabled, it drives the TMO2 pin.

Bank 15/EXT2 is the control register for C/T2, and for I/O Ports 2 and 3. Refer to the I/O Ports section, page 33, for a description of the I/O port bit allocation.

Table 22. C/T2 Bits D15 and D13

D15	D13	C/T2 Clock	Sleep/Wake-Up Mode
0	0	SYSCLK ÷ 2 (default)	n/a
0	1	UI2	n/a
1	0	CLKI	Disabled
1	1	CLKI	Enabled

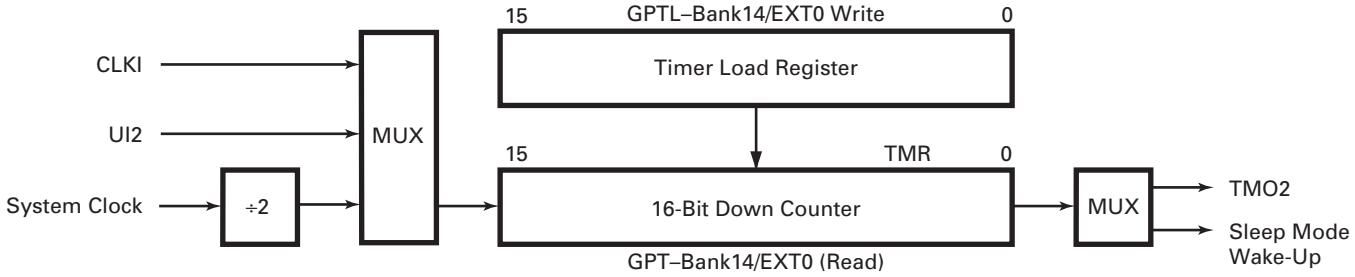


Figure 37. Counter/Timer2 Block Diagram

SERIAL PERIPHERAL INTERFACE (Continued)

Slave Mode Operation

SS must be asserted to enable a data transfer. Incoming data on the SDI pin is shifted into the SPI Shift Register one data bit per SCLK cycle. When a byte of data is received, the SPI Shift Register contents are automatically copied into RxBUF. The Receive Byte Available flag is set, and if enabled, an SPI interrupt is generated. The next byte of data may be received at this time. The current byte in RxBUF must be read before the next byte's reception is complete, or the Receive Byte Overrun flag will set, and the data in RxBUF will be overwritten. The Receive Byte Available flag is reset when RxBUF is read.

Unless the SPI output, SDO, is disabled, for every bit that is transferred into the slave through the SDI pin, a bit is transferred out through the SDO pin on the opposite clock edge. During slave operation, SCLK is an input.

Note: Slave Mode is not available on the 44-pin package.

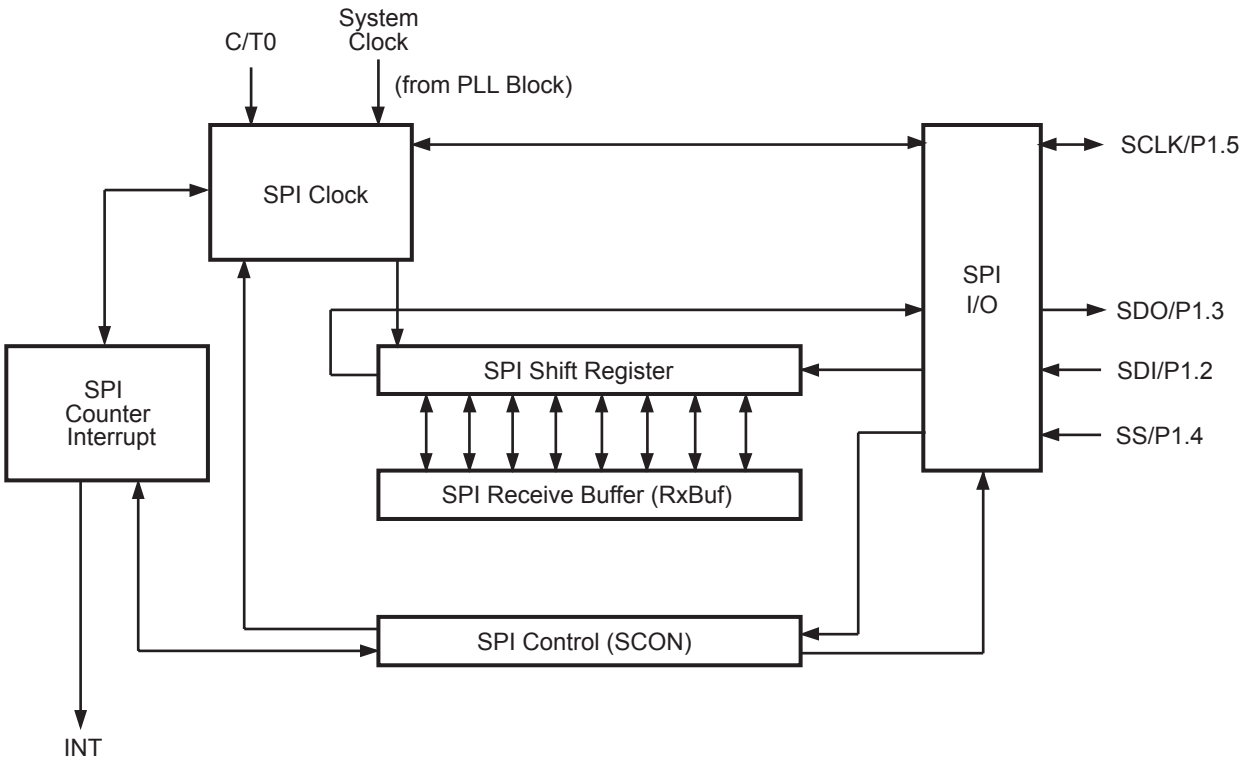
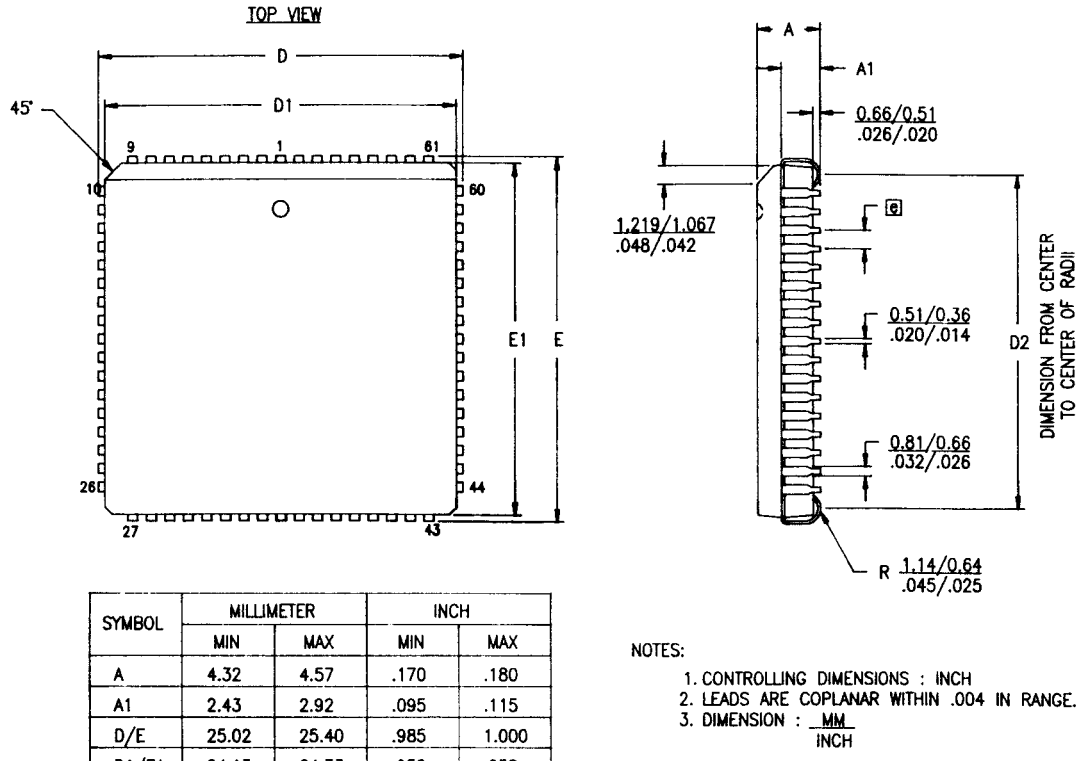


Figure 41. SPI Block Diagram

CONDITION CODES

The following Instruction Description defines the condition codes supported by the DSP assembler. If the instruction description refers to the <cc> (condition code) symbol in one of its addressing modes, the instruction only executes if the condition is true.

Code	Description
C	Carry
EQ	Equal (same as Z)
F	False
IE	Interrupts Enabled
MI	Minus
NC	No Carry
NE	Not Equal (same as NZ)
NIE	Not Interrupts Enabled
NOV	Not Overflow
NU0	Not User Zero
NU1	Not User One
NZ	Not zero
OV	Overflow
PL	Plus (Positive)
U0	User Zero
U1	User One
UGE	Unsigned Greater Than or Equal (Same as NC)
ULT	Unsigned Less Than (Same as C)
Z	Zero



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.32	4.57	.170	.180
A1	2.43	2.92	.095	.115
D/E	25.02	25.40	.985	1.000
D1/E1	24.13	24.33	.950	.958
D2	22.86	23.62	.900	.930
e	1.27 TYP		.050 TYP	

NOTES:

1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN RANGE.
3. DIMENSION : MM / INCH

Figure 47. 68-Pin PLCC Package Diagram

ZiLOG, Inc.
910 East Hamilton Avenue, Suite 110
Campbell, CA 95008
Telephone (408) 558-8500
FAX (408) 558-8300
Internet: http://www.zilog.com