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## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Obsolete |
| Type | Fixed Point |
| Interface | SPI, 3-Wire Serial |
| Clock Rate | 20MHz |
| Non-Volatile Memory | OTP (16kB) |
| On-Chip RAM | 1kB |
| Voltage - I/O | 5.00V |
| Voltage - Core | 5.00V |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-BQFP |
| Supplier Device Package | 80-PQFP (14x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8937320fsg |

**External Bus and External Registers.** The following is made to clarify naming conventions used in this specification. The external bus and external registers are external to the DSP core, and are used to access internal and external peripherals.

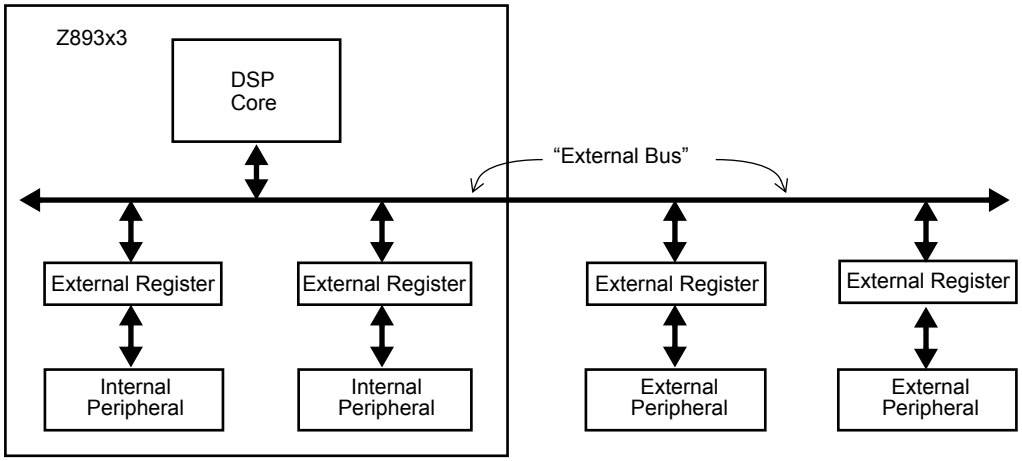



**Figure 2. "External" Bus**

**Table 1. 44-Pin PLCC Z89223/273 Pin Description**

| No | Symbol | Function | Direction | No | Symbol | Function | Direction |
|---|---|---|---|---|---|---|---|
| 1 | P2.0/INT0 | Port 2.0/Interrupt 0 | Input/Output | 23 | AN2 | A/D Input 2 | Input |
| 2 | ED12/P0.12 | External Data Bus/Port0 | Input/Output | 24 | AN3 | A/D Input 3 | Input |
| 3 | ED13/P0.13 | External Data Bus/Port0 | Input/Output | 25 | P2.1/INT1 | Port 2.1/Interrupt 1 | Input/Output |
| 4 | ED14/P0.14 | External Data Bus/Port0 | Input/Output | 26 | $AV_{CC}$ | Analog Power | |
| 5 | $V_{SS}$ | Ground | | 27 | $V_{DD}$ | Power Supply | |
| 6 | ED15/P0.15 | External Data Bus/Port0 | Input/Output | 28 | RD/$\overline{WR}$ | R/W External Bus | Output |
| 7 | ED3/P0.3 | External Data Bus/Port0 | Input/Output | 29 | EA0 | Ext Address 0 | Output |
| 8 | ED4/P0.4 | External Data Bus/Port0 | Input/Output | 30 | EA1 | Ext Address 1 | Output |
| 9 | $V_{SS}$ | Ground | | 31 | EA2 | Ext Address 2 | Output |
| 10 | ED5/P0.5 | External Data Bus/Port0 | Input/Output | 32 | P2.3/TMO1 | Port 2.3/Timer Output 1 | Input/Output |
| 11 | ED6/P0.6 | External Data Bus/Port0 | Input/Output | 33 | $\overline{DS}$ | Ext Data Strobe | Output |
| 12 | ED7/P0.7 | External Data Bus/Port0 | Input/Output | 34 | P2.4/$\overline{WAIT}$ | Port 2.4/Wait for ED | Input/Output |
| 13 | ED8/P0.8 | External Data Bus/Port0 | Input/Output | 35 | CLKI | Clock/Crystal In | Input |
| 14 | ED9/P0.9 | External Data Bus/Port0 | Input/Output | 36 | CLKO | Clock/Crystal Out | Output |
| 15 | $V_{SS}$ | Ground | | 37 | P2.2/TMO0 | Port 2.2/Timer Output 0 | Input/Output |
| 16 | ED10/P0.10 | External Data Bus/Port0 | Input/Output | 38 | LPF | PLL Low Pass Filter | Input |
| 17 | ED11/P0.11 | External Data Bus/Port0 | Input/Output | 39 | $\overline{RESET}$ | Reset | Input |
| 18 | VAHI | Analog High Ref. Voltage | Input | 40 | $V_{DD}$ | Power | |
| 19 | VALO | Analog Low Ref. Voltage | Input | 41 | ED0/P0.0 | External Data Bus/Port0 | Input/Output |
| 20 | AGND | Analog Ground | | 42 | ED1/P0.1 | External Data Bus/Port0 | Input/Output |
| 21 | AN0 | A/D Input 0 | Input | 43 | ED2/P0.2 | External Data Bus/Port0 | Input/Output |
| 22 | AN1 | A/D Input 1 | Input | 44 | $V_{SS}$ | Ground | |

**Table 3. 64-Pin TQFP Z89223/273 Pin Description**

| No | Symbol | Function | Direction | No | Symbol | Function | Direction |
|---|---|---|---|---|---|---|---|
| 1 | ED3/P0.3 | External Data Bus/Port0 | Input/Output | 33 | $\overline{HALT}$ | Halt Execution | Input |
| 2 | ED4/P0.4 | External Data Bus/Port0 | Input/Output | 34 | EA0 | Ext Address 0 | Output |
| 3 | $V_{SS}$ | Ground | | 35 | EA1 | Ext Address 1 | Output |
| 4 | $V_{DD}$ | Power Supply | | 36 | EA2 | Ext Address 2 | Output |
| 5 | ED5/P0.5 | External Data Bus/Port0 | Input/Output | 37 | $V_{DD}$ | Power Supply | |
| 6 | P1.3/SDO | Port 1.3/Serial Output | Input/Output | 38 | P2.3/TMO1 | Port2.3/Timer Output 1 | Input/Output |
| 7 | ED6/P0.6 | External Data Bus/Port0 | Input/Output | 39 | $\overline{DS}$ | Ext Data Strobe | Output |
| 8 | P1.4/SS | Port 1.4/Slave Select | Input/Output | 40 | P2.4/$\overline{WAIT}$ | Port 2.4/Wait for ED | Input/Output |
| 9 | ED7/P0.7 | External Data Bus/Port0 | Input/Output | 41 | CLKI | Clock/Crystal In | Input |
| 10 | P1.5/SCLK | Port 1.5/Serial Clock | Input/Output | 42 | CLKO | Clock/Crystal Out | Output |
| 11 | P2.7 | Port 2.7 | Input/Output | 43 | P2.6/TMO2 | Port 2.6/Timer Output 2 | Input/Output |
| 12 | ED8/P0.8 | External Data Bus/Port0 | Input/Output | 44 | P2.2/TMO0 | Port 2.2/Timer Output 0 | Input/Output |
| 13 | ED9/P0.9 | External Data Bus/Port0 | Input/Output | 45 | P2.5/UI2 | Port 2.5/User Input 2 | Input/Output |
| 14 | $V_{SS}$ | Ground | | 46 | LPF | PLL Low Pass Filter | Input |
| 15 | ED10/P0.10 | External Data Bus/Port0 | Input/Output | 47 | $\overline{RESET}$ | Reset | Input |
| 16 | $V_{SS}$ | Ground | | 48 | $V_{SS}$ | Ground | |
| 17 | ED11/P0.11 | External Data Bus/Port0 | Input/Output | 49 | $V_{DD}$ | Power Supply | |
| 18 | VAHI | Analog High Ref. Voltage | Input | 50 | $V_{SS}$ | Ground | |
| 19 | $V_{SS}$ | Ground | | 51 | ED0/P0.0 | External Data Bus/Port0 | Input/Output |
| 20 | P1.6/UI0 | Port 1.6/User Input 0 | Input/Output | 52 | ED1/P0.1 | External Data Bus/Port0 | Input/Output |
| 21 | VALO | Analog Low Ref. Voltage | Input | 53 | ED2/P0.2 | External Data Bus/Port0 | Input/Output |
| 22 | P1.7/UI1 | Port 1.7/User Input 1 | Input/Output | 54 | P1.0/INT2 | Port 1.0/Interrupt 2 | Input/Output |
| 23 | AGND | Analog Ground | | 55 | $V_{SS}$ | Ground | |
| 24 | AN0 | A/D Input 0 | Input | 56 | P1.1/CLKOUT | Port 1.1/Clock Output | Input/Output |
| 25 | AN1 | A/D Input 1 | Input | 57 | P1.2/SDI | Port 1.2/Serial Input | Input/Output |
| 26 | AN2 | A/D Input 2 | Input | 58 | P2.0/INT0 | Port 2.0/Interrupt 0 | Input/Output |
| 27 | AN3 | A/D Input 3 | Input | 59 | ED12/P0.12 | External Data Bus/Port0 | Input/Output |
| 28 | $V_{SS}$ | Ground | | 60 | ED13/P0.13 | External Data Bus/Port0 | Input/Output |
| 29 | P2.1/INT1 | Port 2.1/Interrupt 1 | Input/Output | 61 | $V_{DD}$ | Power Supply | |
| 30 | AVCC | Analog Power | | 62 | ED14/P0.14 | External Data Bus/Port0 | Input/Output |
| 31 | $V_{DD}$ | Power Supply | | 63 | $V_{SS}$ | Ground | |
| 32 | RD/$\overline{WR}$ | R/W External Bus | Output | 64 | ED15/P0.15 | External Data Bus/Port0 | Input/Output |

**Table 4. 68-Pin PLCC Z89323/373 Pin Description**

| No | Symbol | Function | Direction | No | Symbol | Function | Direction |
|---|---|---|---|---|---|---|---|
| 1 | P1.2/SDI | Port 1.2/Serial Input | Input/Output | 35 | AN0 | A/D Input 0 | Input |
| 2 | P2.0/INT0 | Port 2.0/Interrupt 0 | Input/Output | 36 | AN1 | A/D Input 1 | Input |
| 3 | ED12/P0.12 | External Data Bus/Port0 | Input/Output | 37 | AN2 | A/D Input 2 | Input |
| 4 | ED13/P0.13 | External Data Bus/Port0 | Input/Output | 38 | AN3 | A/D Input 3 | Input |
| 5 | $V_{DD}$ | Power Supply | | 39 | $V_{SS}$ | Ground | |
| 6 | ED14/P0.14 | External Data Bus/Port0 | Input/Output | 40 | P2.1/INT1 | Port 2.1/Interrupt 1 | Input/Output |
| 7 | $V_{SS}$ | Ground | | 41 | AVCC | Analog Power | |
| 8 | ED15/P0.15 | External Data Bus/Port0 | Input/Output | 42 | $V_{DD}$ | Power Supply | |
| 9 | NC | No Connection | | 43 | RD/$\overline{WR}$ | R/W External Bus | Output |
| 10 | NC | No Connection | | 44 | $\overline{HALT}$ | Halt Execution | Input |
| 11 | ED3/P0.3 | External Data Bus/Port0 | Input/Output | 45 | EA0 | Ext Address 0 | Output |
| 12 | ED4/P0.4 | External Data Bus/Port0 | Input/Output | 46 | EA1 | Ext Address 1 | Output |
| 13 | $V_{SS}$ | Ground | | 47 | EA2 | Ext Address 2 | Output |
| 14 | $V_{DD}$ | Power Supply | | 48 | NC | No Connection | |
| 15 | ED5/P0.5 | External Data Bus/Port0 | Input/Output | 49 | $V_{DD}$ | Power Supply | |
| 16 | P1.3/SDO | Port 1.3/Serial Output | Input/Output | 50 | P2.3/TMO1 | Port2.3/Timer Output 1 | Input/Output |
| 17 | ED6/P0.6 | External Data Bus/Port0 | Input/Output | 51 | $\overline{DS}$ | Ext Data Strobe | Output |
| 18 | P1.4/SS | Port 1.4/Slave Select | Input/Output | 52 | P2.4/$\overline{WAIT}$ | Port 2.4/Wait for ED | Input/Output |
| 19 | ED7/P0.7 | External Data Bus/Port0 | Input/Output | 53 | CLKI | Clock/Crystal In | Input |
| 20 | P1.5/SCLK | Port 1.5/Serial Clock | Input/Output | 54 | CLKO | Clock/Crystal Out | Output |
| 21 | P2.7 | Port 2.7 | Input/Output | 55 | P2.6/TMO2 | Port 2.6/Timer Output 2 | Input/Output |
| 22 | ED8/P0.8 | External Data Bus/Port0 | Input/Output | 56 | P2.2/TMO0 | Port 2.2/Timer Output 0 | Input/Output |
| 23 | ED9/P0.9 | External Data Bus/Port0 | Input/Output | 57 | P2.5/UI2 | Port 2.5/User Input 2 | Input/Output |
| 24 | $V_{SS}$ | Ground | | 58 | LPF | PLL Low Pass Filter | Input |
| 25 | ED10/P0.10 | External Data Bus/Port0 | Input/Output | 59 | $\overline{RESET}$ | Reset | Input |
| 26 | $V_{SS}$ | Ground | | 60 | $V_{SS}$ | Ground | |
| 27 | ED11/P0.11 | External Data Bus/Port0 | Input/Output | 61 | $V_{DD}$ | Power Supply | |
| 28 | $V_{DD}$ | Power Supply | | 62 | $V_{SS}$ | Ground | |
| 29 | VAHI | Analog High Ref. Voltage | Input | 63 | ED0/P0.0 | External Data Bus/Port0 | Input/Output |
| 30 | $V_{SS}$ | Ground | | 64 | ED1/P0.1 | External Data Bus/Port0 | Input/Output |
| 31 | P1.6/UI0 | Port 1.6/User Input 0 | Input/Output | 65 | ED2/P0.2 | External Data Bus/Port0 | Input/Output |
| 32 | VALO | Analog Low Ref. Voltage | Input | 66 | P1.0/INT2 | Port 1.0/Interrupt 2 | Input/Output |
| 33 | P1.7/UI1 | Port 1.7/User Input 1 | Input/Output | 67 | $V_{SS}$ | Ground | |
| 34 | AGND | Analog Ground | | 68 | P1.1/CLKOUT | Port 1.1/Clock Output | Input/Output |

## PIN CONFIGURATIONS (Continued)

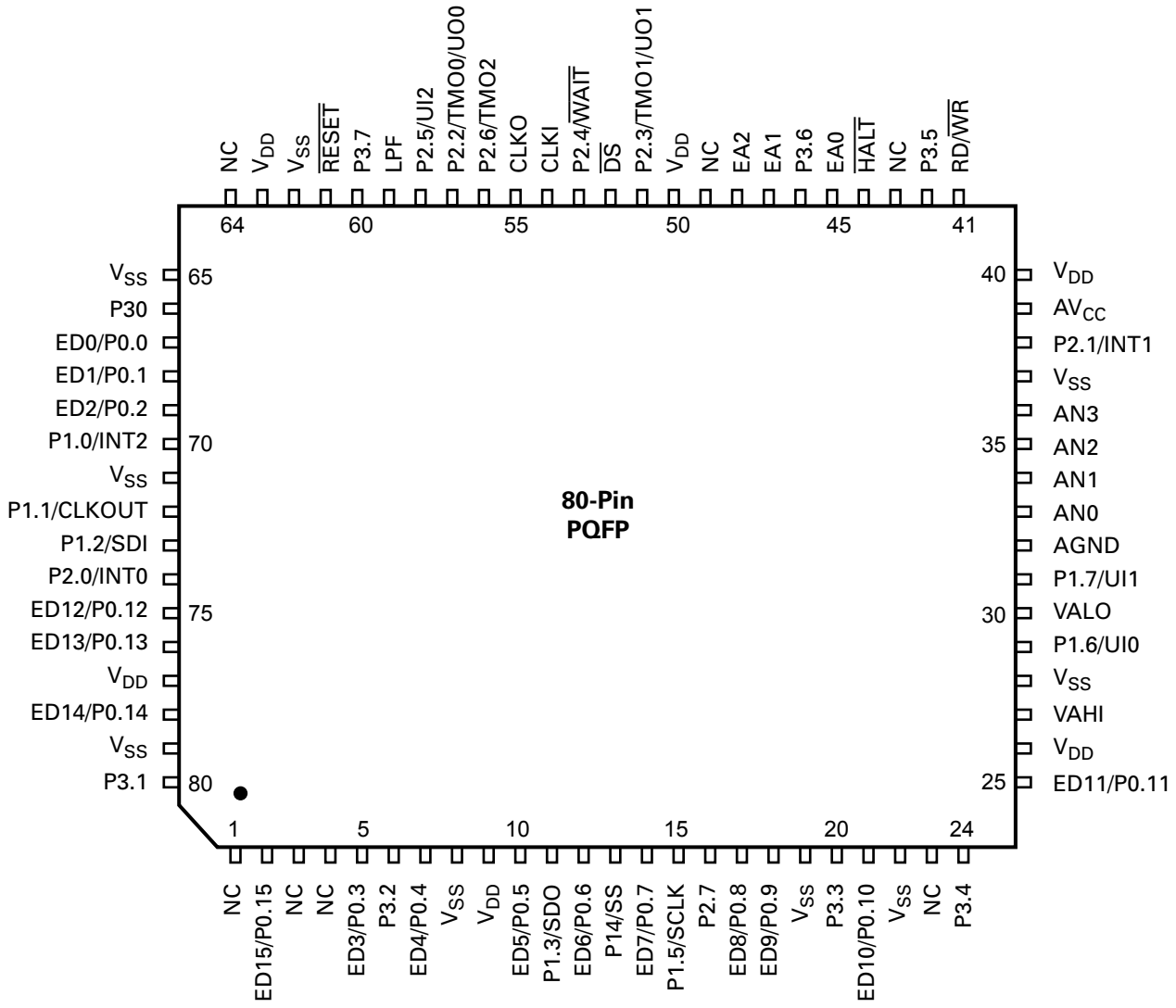



**Figure 7. 80-Pin PQFP Z89323/373 Pin Configuration**

**Table 5. 80-Pin PQFP Z89323/373 Pin Description**

| No | Symbol | Function | Direction | No | Symbol | Function | Direction |
|---|---|---|---|---|---|---|---|
| 1 | NC | No Connection | | 41 | RD/$\overline{WR}$ | R/W External Bus | Output |
| 2 | ED15/P0.15 | External Data Bus/Port0 | Input/Output | 42 | P3.5 | Port 3.5 | Output |
| 3 | NC | No Connection | | 43 | NC | No Connection | |
| 4 | NC | No Connection | | 44 | $\overline{HALT}$ | Halt Execution | Input |
| 5 | ED3/P0.3 | External Data Bus/Port0 | Input/Output | 45 | EA0 | Ext Address 0 | Output |
| 6 | P3.2 | Port 3.2 | Input | 46 | P3.6 | Port 3.6 | Output |
| 7 | ED4/P0.4 | External Data Bus/Port0 | Input/Output | 47 | EA1 | Ext Address 1 | Output |
| 8 | $V_{SS}$ | Ground | | 48 | EA2 | Ext Address 2 | Output |
| 9 | $V_{DD}$ | Power Supply | | 49 | NC | No Connection | |
| 10 | ED5/P0.5 | External Data Bus/Port0 | Input/Output | 50 | $V_{DD}$ | Power Supply | |
| 11 | P1.3/SDO | Port 1.3/Serial Output | Input/Output | 51 | P2.3/TMO1 | Port 2.3/Timer Output 1 | Input/Output |
| 12 | ED6/P0.6 | External Data Bus/Port0 | Input/Output | 52 | $\overline{DS}$ | Ext Data Strobe | Output |
| 13 | P1.4/SS | Port 1.4/Slave Select | Input/Output | 53 | P2.4/$\overline{WAIT}$ | Port 2.4/Wait for ED | Input/Output |
| 14 | ED7/P0.7 | External Data Bus/Port0 | Input/Output | 54 | CLKI | Clock/Crystal In | Input |
| 15 | P1.5/SCLK | Port 1.5/Serial Clock | Input/Output | 55 | CLKO | Clock/Crystal Out | Output |
| 16 | P2.7 | Port 2 7 | Input/Output | 56 | P2.6/TMO2 | Port 2.6/Timer Output 2 | Input/Output |
| 17 | ED8/P0.8 | External Data Bus/Port0 | Input/Output | 57 | P2.2/TMO0 | Port 2.2/Timer Output 0 | Input/Output |
| 18 | ED9/P0.9 | External Data Bus/Port0 | Input/Output | 58 | P2.5/UI2 | Port 2.5/User Input 2 | Input/Output |
| 19 | $V_{SS}$ | Ground | | 59 | LPF | PLL Low Pass Filter | Input |
| 20 | P3.3 | Port 3 3 | Input | 60 | P3.7 | Port 3.7 | Output |
| 21 | ED10/P0.10 | External Data Bus/Port0 | Input/Output | 61 | $\overline{RESET}$ | Reset | Input |
| 22 | $V_{SS}$ | Ground | | 62 | $V_{SS}$ | Ground | |
| 23 | NC | No Connection | | 63 | $V_{DD}$ | Power Supply | |
| 24 | P3.4 | Port 3.4 | Output | 64 | NC | No Connection | |
| 25 | ED11/P0.11 | External Data Bus/Port0 | Input/Output | 65 | $V_{SS}$ | Ground | |
| 26 | $V_{DD}$ | Power Supply | | 66 | P3.0 | Port 3.0 | Input |
| 27 | VAHI | Analog High Ref. Voltage | Input | 67 | ED0/P0.0 | External Data Bus/Port0 | Input/Output |
| 28 | $V_{SS}$ | Ground | | 68 | ED1/P0.1 | External Data Bus/Port0 | Input/Output |
| 29 | P1.6/UI0 | Port 1 6/User Input 0 | Input/Output | 69 | ED2/P0.2 | External Data Bus/Port0 | Input/Output |
| 30 | VALO | Analog Low Ref. Voltage | Input | 70 | P1.0/INT2 | Port 1.0/Interrupt 2 | Input/Output |
| 31 | P1.7/UI1 | Port 1 7/User Input 1 | Input/Output | 71 | $V_{SS}$ | Ground | |
| 32 | AGND | Analog Ground | | 72 | P1.1/CLKOUT | Port 1.1/Clock Output | Input/Output |
| 33 | AN0 | A/D Input 0 | Input | 73 | P1.2/SDI | Port 1.2/Serial Input | Input/Output |
| 34 | AN1 | A/D Input 1 | Input | 74 | P2.0/INT0 | Port 2.0/Interrupt 0 | Input/Output |
| 35 | AN2 | A/D Input 2 | Input | 75 | ED12/P0.12 | External Data Bus/Port0 | Input/Output |
| 36 | AN3 | A/D Input 3 | Input | 76 | ED13/P0.13 | External Data Bus/Port0 | Input/Output |
| 37 | $V_{SS}$ | Ground | | 77 | $V_{DD}$ | Power Supply | |
| 38 | P2.1/INT1 | Port 2.1/Interrupt 1 | Input/Output | 78 | ED14/P0.14 | External Data Bus/Port0 | Input/Output |
| 39 | $AV_{CC}$ | Analog Power | | 79 | $V_{SS}$ | Ground | |
| 40 | $V_{DD}$ | Power Supply | | 80 | P3.1 | Port 3.1 | Input |

## TIMING DIAGRAMS (Continued)

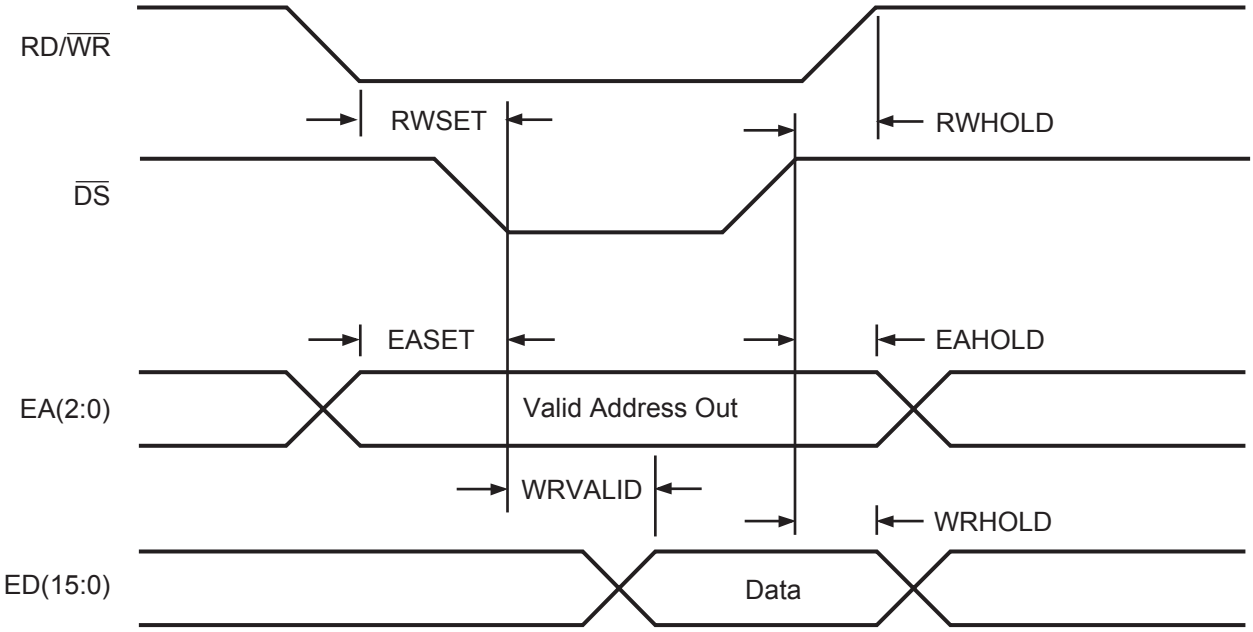



**Figure 13. Write Timing**

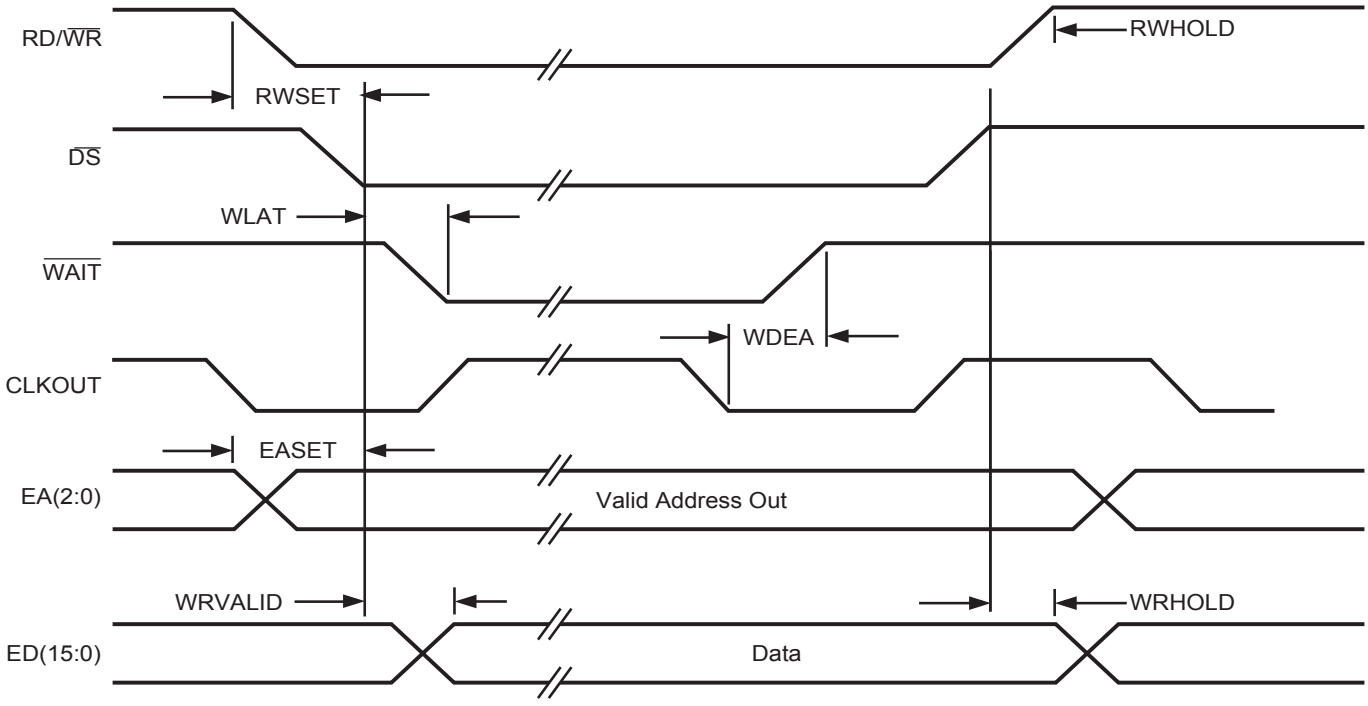
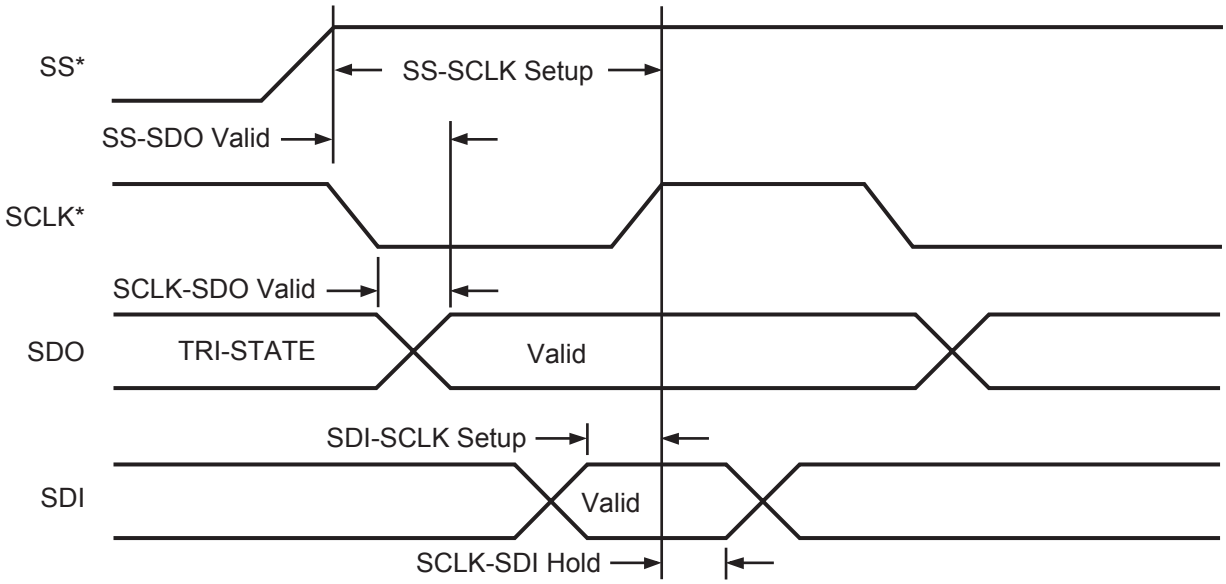



**Figure 14. Write Timing Using WAIT Pin**




*Notes: The polarity of SCLK and SS are programmable by the user. SS is used in Slave Mode only. This figure illustrates data transmission on the falling edge of SCLK, data reception on the rising edge of SCLK, with SS active Low (default).

**Figure 15. SPI Timing (Master and Slave Modes)**

## REGISTERS

Both external and internal registers are accessed in one machine cycle. The external registers are used to access the on-chip peripherals when they are enabled.

The internal registers of the Z893X3 are defined below:

| Register | Register Definition |
|---|---|
| X | Multiplier X Input, 16-bits |
| Y | Multiplier Y Input, 16-bits |
| P | Multiplier Output, 24-bits |
| A | Accumulator, 24-bits |
| Pn:b | Six Data RAM Pointers, 8-bits each |
| PC | Program Counter, 16-bits |
| SR | Status Register, 16-bits |
| EXT0 | depends on Bank Select #, 16-bits |
| EXT1 | depends on Bank Select #, 16-bits |
| EXT2 | depends on Bank Select #, 16-bits |
| EXT3 | depends on Bank Select #, 16-bits |
| EXT4 | depends on Bank Select #, 16-bits |
| EXT5 | depends on Bank Select #, 16-bits |
| EXT6 | depends on Bank Select #, 16-bits |
| EXT7 | Interrupt Status/Bank Select, 16-bits |

**X** and **Y** are two 16-bit input registers for the multiplier. These registers can be utilized as temporary registers when the multiplier is not being used.

**P** holds the result of multiplications and is read-only.

**A** is a 24-bit Accumulator. The output of the ALU is sent to this register. When 16-bit data is transferred into this register, it is placed into the 16 MSBs and the least significant eight bits are set to zero. Only the upper 16 bits are transferred to the destination register when the Accumulator is selected as a source register in transfer instructions.

**Pn:b** are the pointer registers for accessing data RAM where n = 0, 1, or 2, and b = 0 or 1. They can be directly read or written. They point to locations in data RAM.

**PC** is the Program Counter. Any instruction which may modify this register requires two clock cycles.

**SR** is the status register. It contains the ALU status and processor control bits. The status register can always be read in its entirety. S15–S10 are set/reset by hardware and can only be read by software. S9–S0 control hardware operations and can be written by software.

**Table 11. Status Register Bit Functions**

| SR Bit | Function | Read/Write |
|---|---|---|
| S15 (N) | ALU Negative | RO |
| S14 (OV) | ALU Overflow | RO |
| S13 (Z) | ALU Zero | RO |
| S12 (C) | Carry | RO |
| S11 (UI1) | User Input 1 | RO |
| S10 (UI0) | User Input 0 | RO |
| S9 (SH3) | MPY Output Arithmetically Shifted Right by Three Bits | R/W |
| S8 (OP) | Overflow Protection | R/W |
| S7 (IE) | Interrupt Enable | R/W |
| S6 ($\overline{UO1}$) | User Output 1 | R/W |
| S5 ($\overline{UO0}$) | User Output 0 | R/W |
| S4–S3 | "Short Form Direct" bits | R/W |
| S2–S0 (RPL) | RAM Pointer Loop Size | R/W |

**Note:** RO = read only, RW = read/write. The status register can always be read in its entirety.

**S15–S12** are set/reset by the ALU after an operation.

**S11–S10** are set/reset by the user input pins.

If **S9** is set and a multiply/shift option is used, the shifter shifts the result three bits right. This feature allows the data to be scaled and prevents overflows.

If **S8** is set, the hardware clamps at maximum positive or negative values instead of overflowing.

**S7** enables interrupts.

**S6–S5** are User Outputs. The complement of the value in the Status Register appears on bits 2 and 3 of Port2 if the User Outputs are enabled by writing a 1 to Bit 15 of Bank 15–EXT3, and Counter/Timer 0 and 1 are disabled.

**S4–S3** are the two MSBs in the "short form direct" mode of addressing.

**S2–S0** define the RAM pointer loop size as indicated in Table 12.

## BANK/EXT REGISTER ASSIGNMENTS (Continued)

### Interrupt Status/Bank Select Register—EXT7

Following is a description of EXT7. It contains both a Bank Select Field and Interrupt Status Bits.

**Bank Select Field.** The four LSBs of EXT7 denote which bank is selected as the current working bank.

**Interrupt Status Bits.** These bits can be read to identify which interrupts are pending. A "1" denotes interrupt pending, and a "0" denotes no interrupt. This ability to identify interrupts is particularly useful in polled interrupt operation or when servicing ISR2, which may come from several sources.

**Note:** Write "1" to a particular status bit to clear that bit. Before exiting an interrupt service routine, the relevant interrupt bit(s) should be cleared. To clear a bit efficiently:

- Load the value of EXT7 into a register or memory location
- Then load that value back into EXT7

Performing these steps clear all of the interrupts that were pending, but leave the Register Bank Select unchanged.

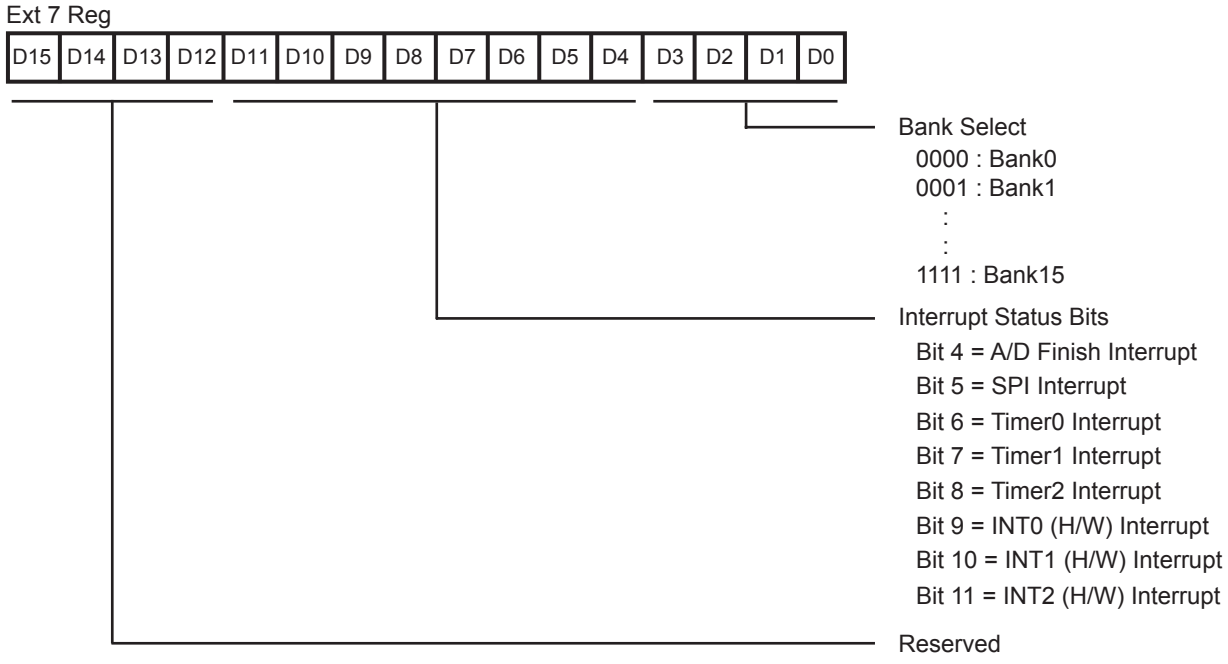



**Figure 20. EXT7 Register**

## Interrupt Allocation Register—Bank15/EXT6

Bits 3–0 of the Interrupt Allocation Register define which unique interrupt source the highest priority, and is allocated to ISR0 (Interrupt Service Request 0).

Bits 7–4 of the Interrupt Allocation Register define which unique interrupt source has the second highest priority, and is allocated to ISR1 (Interrupt Service Request 1).

Bits 15–8 of the Interrupt Allocation Register are enable bits for common interrupt sources which have the lowest priority, and are all allocated to ISR2 (Interrupt Service Request 2). All the enabled interrupts which are not allocated to ISR0 or ISR1, are allocated to ISR2. When an ISR2 interrupt occurs, the interrupt service routine must read the Interrupt Status Register in EXT7 to determine the source. The Interrupt Status Register can be used for polling interrupts. An Interrupt that is not selected as a source to ISR0, ISR1, or ISR2, is disabled.

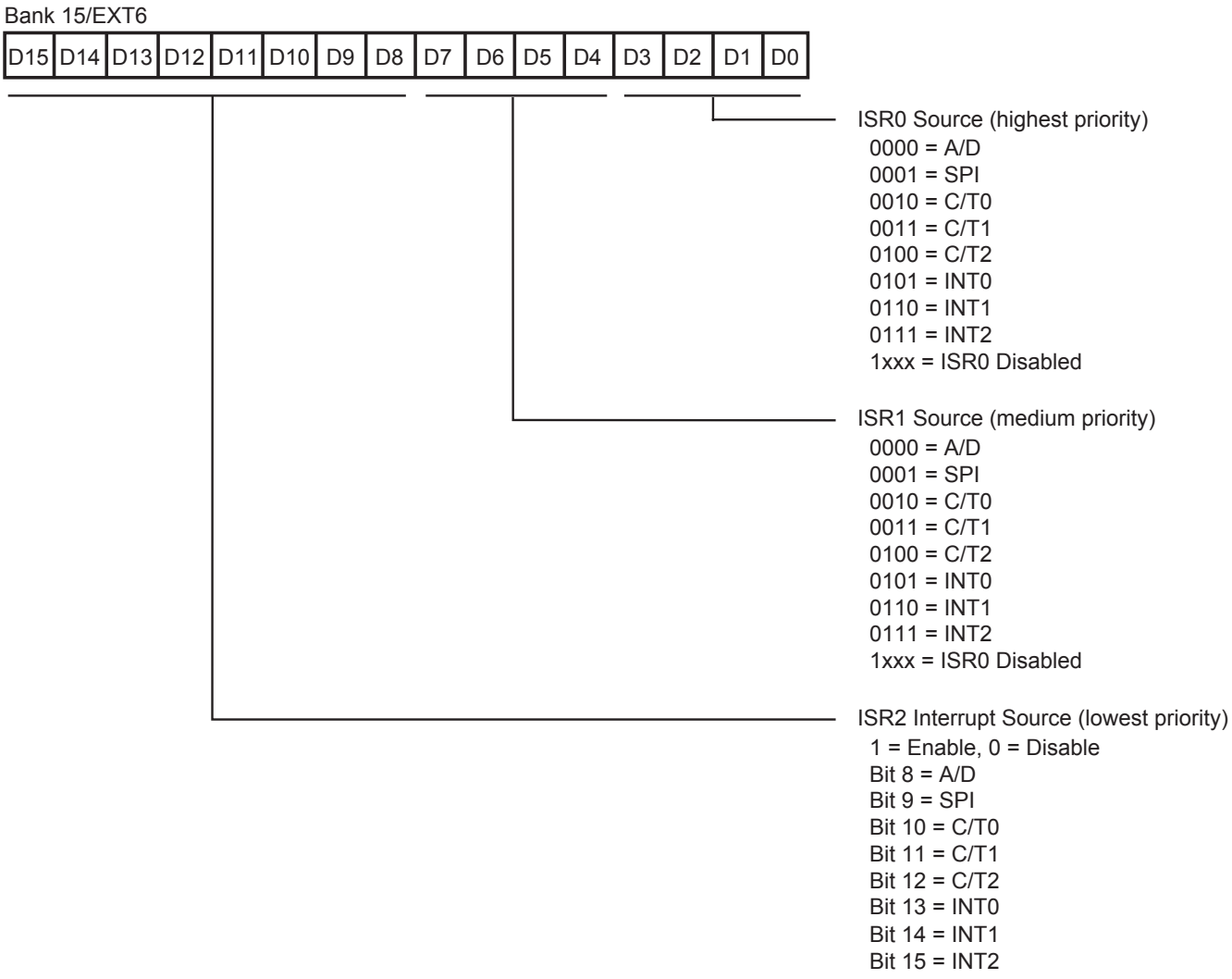



**Figure 21. Interrupt Allocation Register**

## I/O PORTS (Continued)

### Port0—16-Bit Programmable I/O

Bank15/EXT0 is the Port0 direction control register. Bank15/EXT1 includes specific bits to enable and configure Port0. The Port0 data register is Ext4 in Banks 0, 1, or 5.

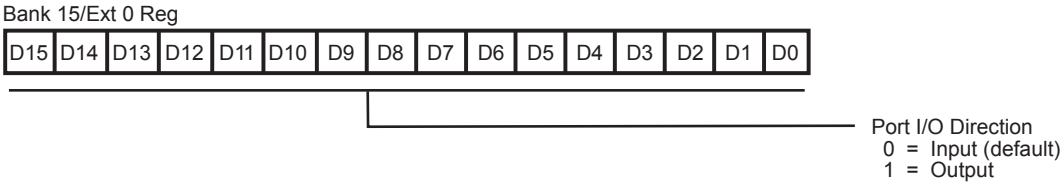



**Figure 25. Port 0 Control Register**

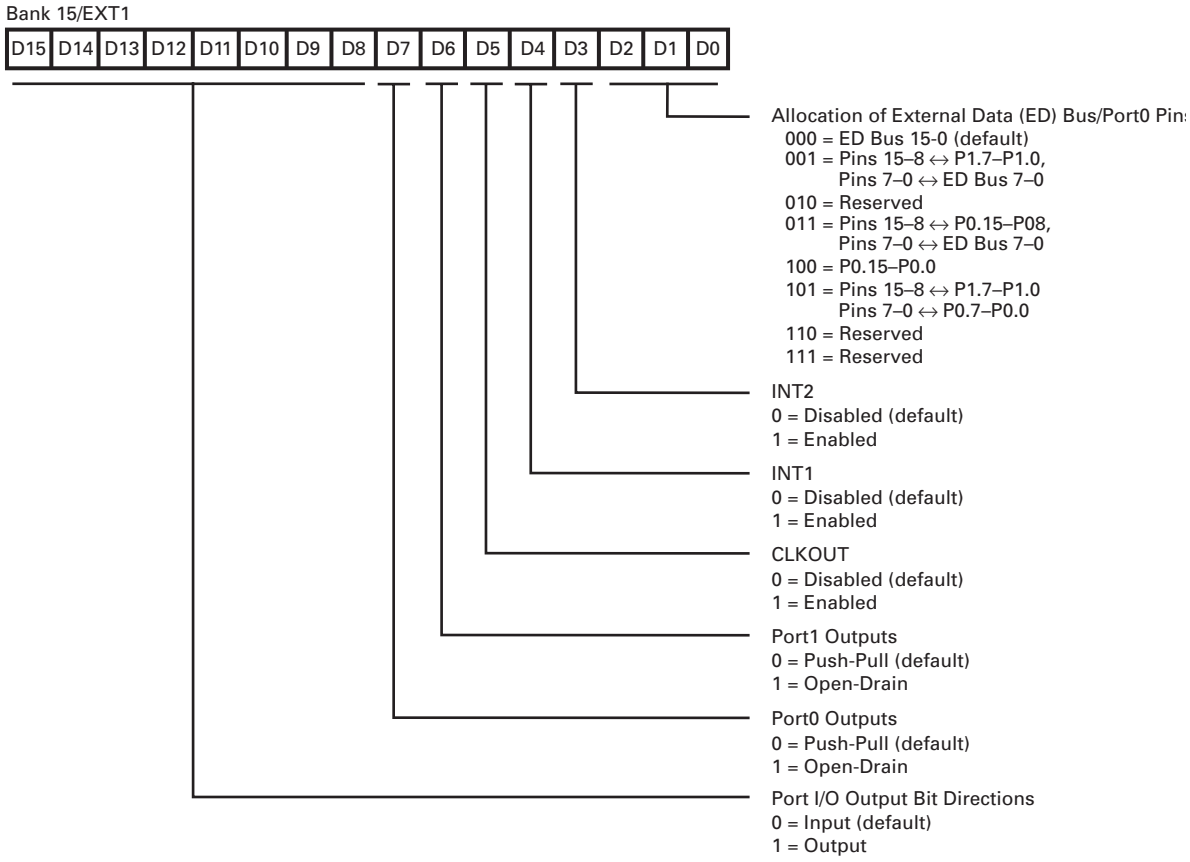



**Figure 26. Bank15/EXT1 Register**

## Port1—8-Bit Programmable I/O

Bank15/EXT1 is the Port1 control register. The MSB is the Port1 direction control. Port1 data is accessed as the LSB of EXT5 in Banks 0, 1, or 5. The Port1 pins can also be mapped to internal functions. When INT2, CLKOUT, UI0 and UI1, or the SPI are enabled, they use Port1 pins. The 44-pin packages do not feature Port1 pins, however, Port1 and its internal functions can be mapped to the MSB of the ED Bus/Port0 pins. See bits 2–0 of Bank15/EXT1.

**Table 16. Port1 Bit Function Allocation**

| Port Pin | IF | Condition | Then | Else |
|---|---|---|---|---|
| P1.0/INT2 | Bank15/EXT1 Bit 3 = 1 | Enable INT2 | INT2 | P1.0 |
| P1.1/CLKOUT | Bank15/EXT1 Bit 5 = 1 | Enable CLKOUT | CLKOUT | P1.1 |
| P1.2/SDI | Bank15/EXT4 Bit 0 = 1 | Enable SPI | SDI | P1.2 |
| P1.3/SDO | Bank15/EXT4 Bit 0 = 1 | Enable SPI | SDO | P1.3 |
| P1.4/SS | Bank15/EXT4 Bit 0 = 1 | Enable SPI | SS | P1.4 |
| P1.5/SCLK | Bank15/EXT4 Bit 0 = 1 | Enable SPI | SCLK | P1.5 |
| P1.6/UI0 | Bank13/EXT1 Bits [2,1] = 10, or Bank14/EXT1 Bits [2,1] = 10 | Enable UI0 | UI0 | P1.6 |
| P1.7/UI1 | Bank13/EXT1 Bits [2,1] = 11, or Bank14/EXT1 Bits [2,1] = 11 | Enable UI1 | UI1 | P1.7 |

## I/O PORTS (Continued)

### Port2—8-Bit Programmable I/O

Bank15/EXT2 is the Port2 control register. The LSB is the Port2 direction control. Port2 data is accessed as the MSB of EXT5 in Banks 0,1,or 5. The Port2 pins can also be mapped to internal functions. When INT0, INT1, TMO0, TMO1, $\overline{WAIT}$, UI2, or TMO2 are enabled, they use Port2 pins. The 44-pin packages do not feature Port2 pins P2.7–P2.5.

**Table 17. Port2 Bit Function Allocation**

| Port Pin | IF | Condition | Then | Else |
|---|---|---|---|---|
| P2.0/INT0 | Bank15/EXT2 Bit 9 = 1 | Enable INT0 | INT0 | P2.0 |
| P2.1/INT1 | Bank15/EXT1 Bit 4 = 1 | Enable INT1 | INT1 | P2.1 |
| P2.2/TMO0 | Bank13/EXT1 Bit [6,5] = 10, or<br>Bank14/EXT1 Bit [6,5] = 10 | Enable TMO0 | TMO0 | P2.2 |
| P2.3/TMO1 | Bank13/EXT1 Bit [6,5] = 11, or<br>Bank14/EXT1 Bit [6,5] = 11 | Enable TMO1 | TMO1 | P2.3 |
| P2.4/$\overline{WAIT}$ | Bank15/EXT3 Bit 14 = 1 | Enable $\overline{WAIT}$ | $\overline{WAIT}$ | P2.4 |
| P2.5/UI2 | Bank15/EXT2 Bit 13 = 1 | C/T2 clock is UI2 | UI2 | P2.5 |
| P2.6/TMO2 | Bank15/EXT2 Bits 14 = 1 | Enable TMO2 | TMO2 | P2.6 |
| P2.7 | | | P2.7 | P2.7 |

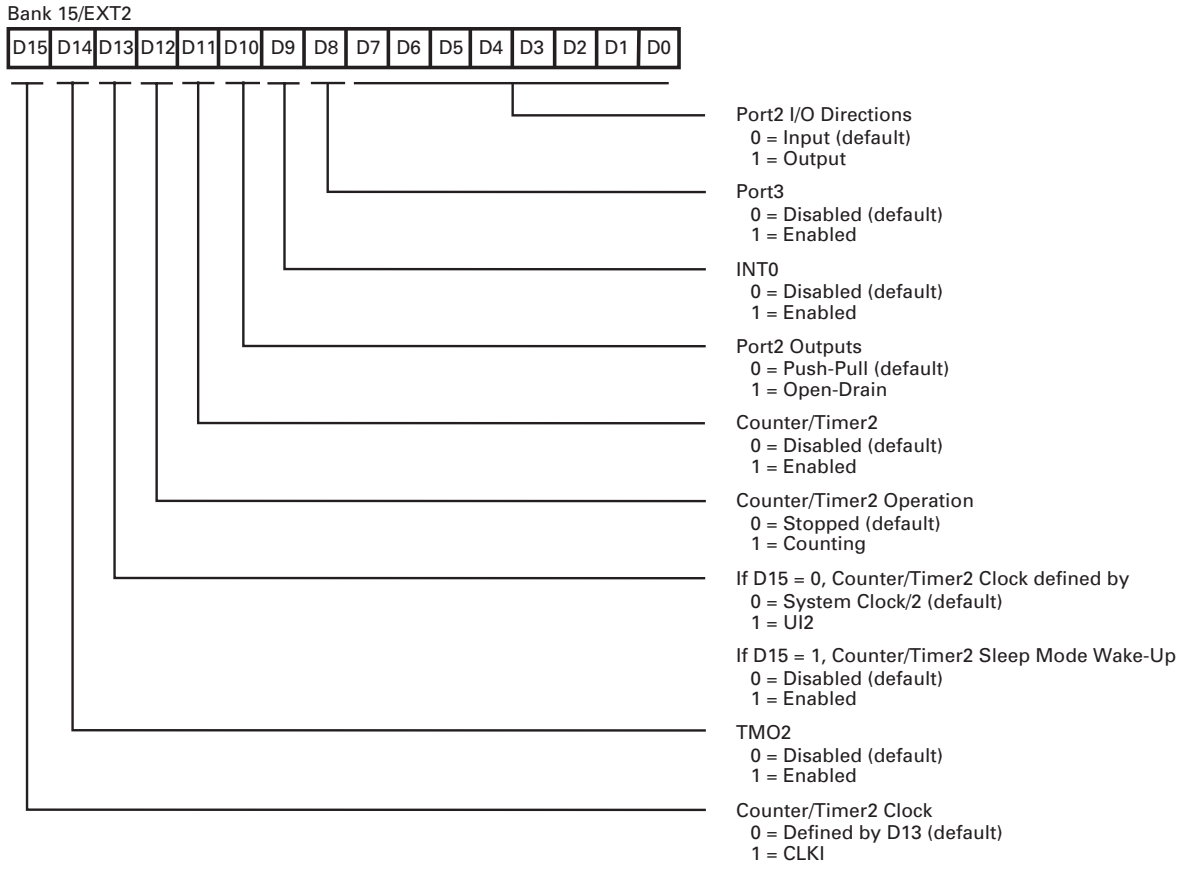



**Figure 27. Bank15/EXT2 Register**

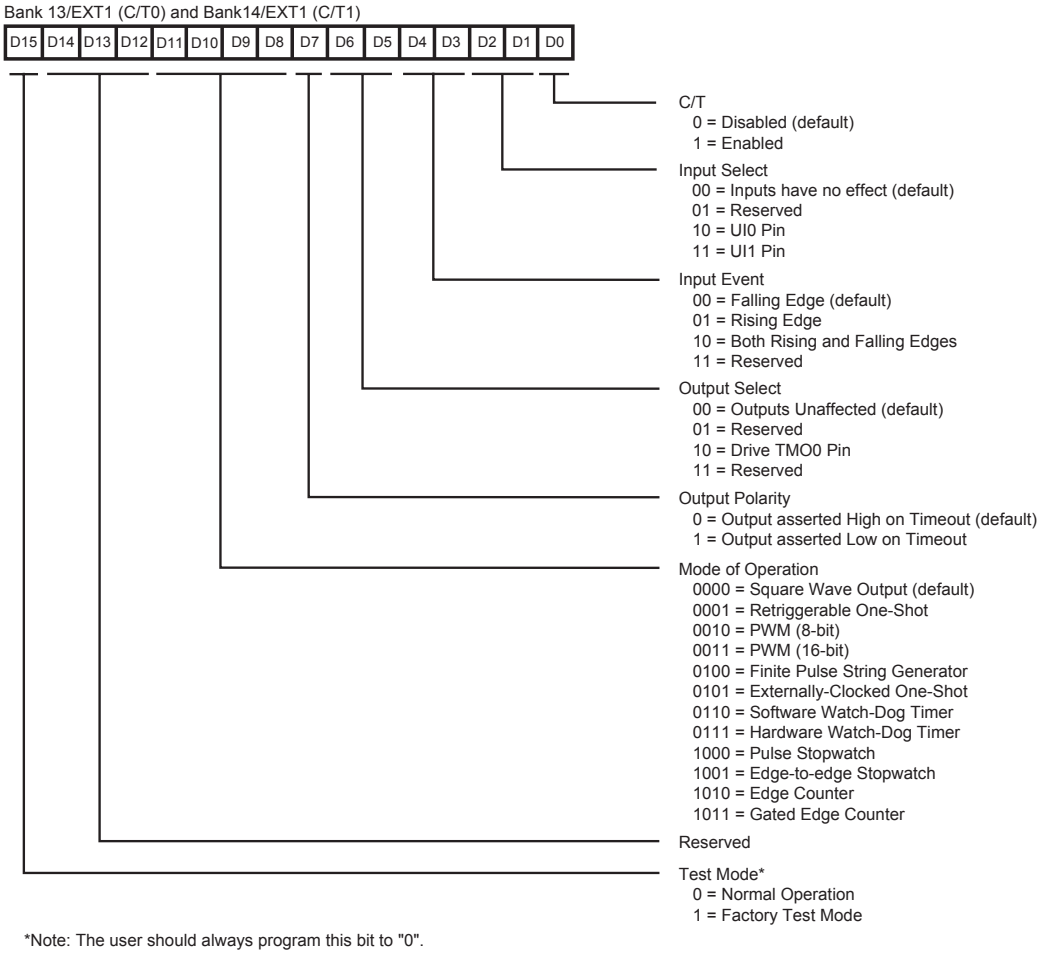



**Figure 32. C/T0 and C/T1 Control Register**

## C/T Registers

Each C/T contains a set of five 16-bit Registers. Bank13 is used to access the registers for C/T0 and Bank14 is for the C/T1 registers. All accesses to C/T Registers occur with zero wait states.

**Counter/Timer Control Register (Bank13,14/EXT1).** The C/T Control register enables/disables the C/T, selects input and output options, and the mode of operation.

**TMLR—Load Register (Bank13,14/EXT2).** The 16-bit TMLR register holds the value that is loaded into TMR when TMR underflows.

**TMR—Counter Register (Bank13,14/EXT3).** TMR is a 16-bit down counter that holds the current C/T value. It can be read like any other ordinary register. However, writing to TMR is different than writing to an ordinary register. A write to TMR causes the contents of TMLR to be written into TMR, causing the C/T to be retriggered.

**TPLR—Prescaler Load Register (Bank13,14/EXT4).** The 16-bit TPLR register holds the prescaler load value in its lower 8 bits. Bit 15 must be written with a “1”, and bits 14–8 must be written with “0’s”.

**Note:** If the C/T interrupt is being used, this register must be re-written at the end of the interrupt service routine in order to enable the next interrupt. The number of clock cycles from the beginning of the interrupt service routine to the write must exceed the prescaler load value.

## PERIPHERALS (Continued)

**TPR—Prescaler Register (Bank13,14/EXT5).** TPR is an 8-bit down counter that holds the current Prescaler Count Value. It can be read like any other ordinary register. However, writing to TPR is different than writing to an ordinary register. A write to TPR causes the lower 8-bit contents of TPLR to be written into TPR, causing the Prescaler to be retriggered.

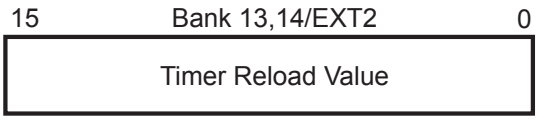



**Figure 33. TMLR—Load Register**

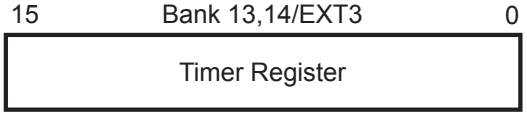



**Figure 34. TMR—Counter Register**

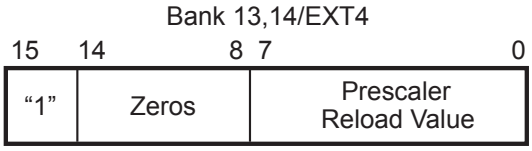



**Figure 35. TPLR—Prescaler Load Register**

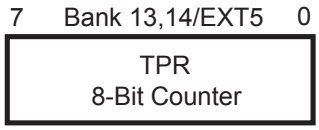



**Figure 36. TPR—Prescaler Register**

### Prescaler Operation

The Prescaler section comprises TPLR and TPR, followed by a divide-by-two flip-flop. This operation generates a 50 percent duty cycle output, TMCLKIN. TPR's input clock is the system clock. The maximum prescaler output frequency is 1/2 the system clock frequency.

After TPR is loaded, it decrements at the system clock frequency and generates an output to the divide-by-two flip-flop. When the count reaches 0, the TPR counter is reloaded from the lower 8 bits of TPLR Register.

Two other events cause a reloading of the TPR counter:

1. Writing to TPR
2. Reloading TMR, which happens when TMR underflows, or when TMR is written.

**Note:** For C/T Modes 8–11, the external input signal on UI0 or UI1 is synchronized with TMCLKIN before being applied to TMR. The external input signal frequency must be no higher than 1/2 of the TMCLKIN frequency.

## GENERAL-PURPOSE COUNTER/TIMER (C/T2)

This versatile16-bit C/T offers multiple uses, including Sleep Mode Wake-up. It can be clocked with the slow 32 kHz crystal clock (CLKI), while the DSP and other peripheral functions operate at a higher frequency generated by the PLL. Also included is an independent long duration timer.

GPT is a 16-bit down counter that holds the current C/T value. It can be read like any other ordinary register. GPTL and GPT share the same address, Bank14/EXT0. A write to GPTL reloads GPT, causing the C/T to be retriggered. When C/T2 underflows, it is reloaded with the most recent value written to GPTL. If the C/T2 interrupt is enabled, at underflow an interrupt is generated. The counting operation of the counter can be disabled. The C/T clock source can be selected to be CLKI, UI2, or the system clock divided by 2. When the C/T2 output is enabled, it drives the TMO2 pin.

Bank 15/EXT2 is the control register for C/T2, and for I/O Ports 2 and 3. Refer to the I/O Ports section, page 33, for a description of the I/O port bit allocation.

**Table 22. C/T2 Bits D15 and D13**

| D15 | D13 | C/T2 Clock | Sleep/Wake-Up Mode |
|---|---|---|---|
| 0 | 0 | SYSCLK ÷ 2 (default) | n/a |
| 0 | 1 | UI2 | n/a |
| 1 | 0 | CLKI | Disabled |
| 1 | 1 | CLKI | Enabled |

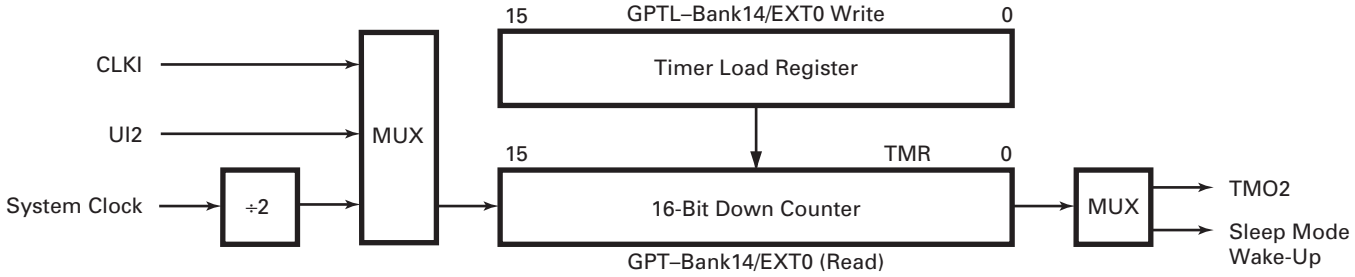



**Figure 37. Counter/Timer2 Block Diagram**

## SERIAL PERIPHERAL INTERFACE

The Z893x3 incorporates a Serial Peripheral Interface (SPI) for communication with other microcontrollers and peripherals. The SPI can be operated either as the system Master, or as a system Slave. The SPI consists of three registers: the SPI Control Register (Bank15/EXT4), the SPI Receive/Buffer Register (RxBUF), and the SPI Shift Register.

### SPI Data Access

Receive operations are double buffered. Bank0/EXT3 accesses both RxBUF for read (receive) operations, and the SPI shift register for write (transmit) operations.

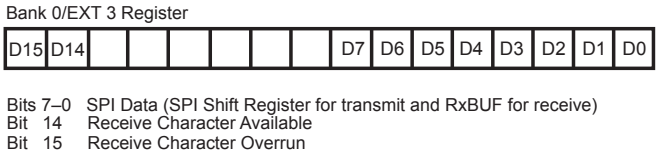



**Figure 39. SPI Data Access**

### SPI Control Register

This register is the Low byte of Bank15/EXT4. It is a read/write register that controls Master/Slave selection, SS polarity, clock source and phase selection, and indicates byte available and data overrun conditions. The control register is multifunction depending on Master/Slave mode selection.

In Master mode, Bit 6 defines the SPI clock source. A “1” selects SCLK = C/T0 output, and a “0” selects SCLK = System Clock divided down by 2, 4, 8, or 16, as determined by bits 1 and 2.

In Slave Mode, bit 1 is the Receive Byte Overrun flag. This flag can be cleared by writing a “0” to this bit. Bit 2 is the SDO output enable.A “0” tristates SDO, a “1” enables data output on SDO. Bit 4 signals that a receive byte is available in the RxBUF Register. If the associated interrupt enable bit is enabled, an interrupt is generated.

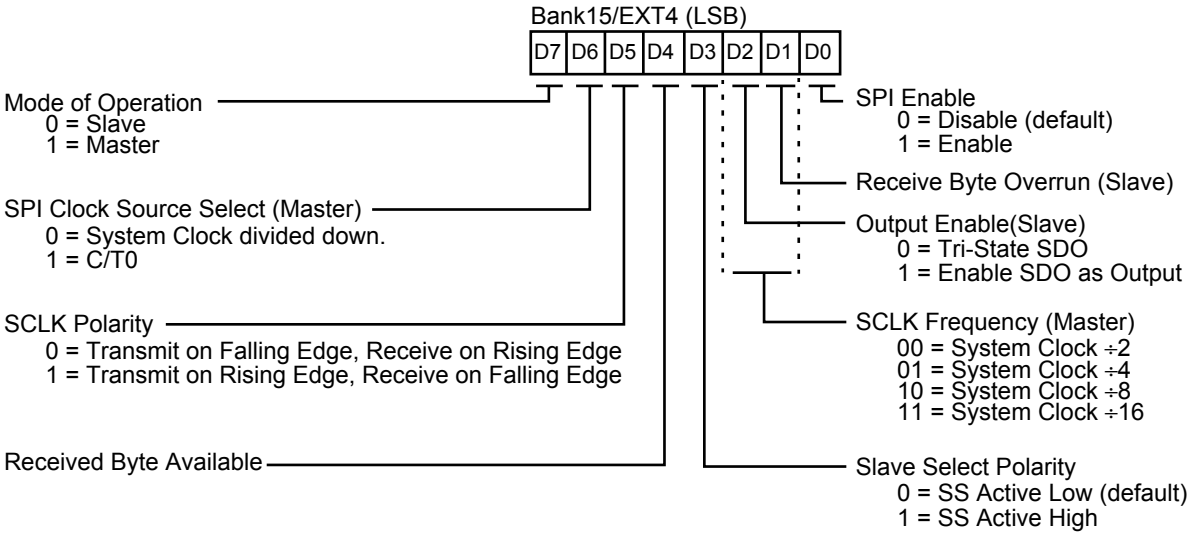



**Figure 40. SPI Control Register**

### Master Mode Operation

The DSP must first activate the target slave’s select pin through an I/O port. Loading data into the SPI Shift Register initiates the transfer. Data is transferred out the SDO pin to the slave one data bit per SCLK cycle. The MSB is shifted out first. At the conclusion of the transfer, the Receive Byte Available flag is set, and if enabled, an SPI interrupt is generated. The Receive Byte Available flag is reset when RxBUF is read.

## SERIAL PERIPHERAL INTERFACE (Continued)

### Slave Mode Operation

SS must be asserted to enable a data transfer. Incoming data on the SDI pin is shifted into the SPI Shift Register one data bit per SCLK cycle. When a byte of data is received, the SPI Shift Register contents are automatically copied into RxBUF. The Receive Byte Available flag is set, and if enabled, an SPI interrupt is generated. The next byte of data may be received at this time. The current byte in RxBUF must be read before the next byte's reception is complete, or the Receive Byte Overrun flag will set, and the data in RxBUF will be overwritten. The Receive Byte Available flag is reset when RxBUF is read.

Unless the SPI output, SDO, is disabled, for every bit that is transferred into the slave through the SDI pin, a bit is transferred out through the SDO pin on the opposite clock edge. During slave operation, SCLK is an input.

**Note:** Slave Mode is not available on the 44-pin package.

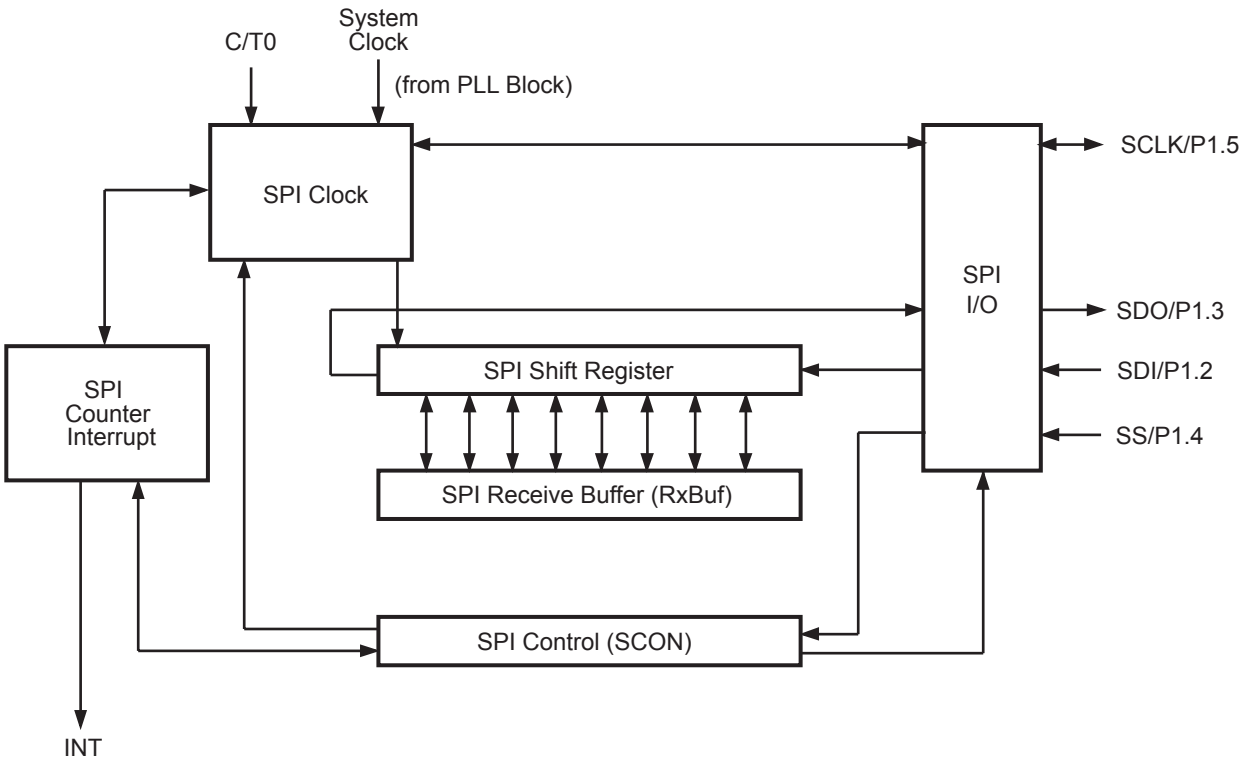



**Figure 41. SPI Block Diagram**

| Inst. | Description | Synopsis | Operands | Words | Cycles | Examples |
|---|---|---|---|---|---|---|
| **Notes:** | | | | | | |
| If src1 is <regind> it must be a bank 1 register. Src2's <regind> must be a bank 0 register. | | | | | | |
| <hwregs> for src1 cannot be X. | | | | | | |
| For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, <regind> the <bank switch> defaults to ON. | | | | | | |
| NEG | Negate | NEG <cc>,A | <cc>, A | 1 | 1 | NEG MI,A |
| | | | A | 1 | 1 | NEG A |
| NOP | No operation | NOP | None | 1 | 1 | NOP |
| OR | Bitwise OR | OR <dest>,<src> | A,<pregs> | 1 | 1 | OR A,P0:1 |
| | | | A,<dregs> | 1 | 1 | OR A, D0:1 |
| | | | A,<limm> | 2 | 2 | OR A,#%2C21 |
| | | | A,<memind> | 1 | 3 | OR A,@@P2:1+ |
| | | | A,<direct> | 1 | 1 | OR A, %2C |
| | | | A,<regind> | 1 | 1 | OR A,@P1:0–LOOP |
| | | | A,<hwregs> | 1 | 1 | OR A,EXT6 |
| | | | A,<simm> | 1 | 1 | OR A,#%12 |
| POP | Pop value from stack | POP <dest> | <pregs> | 1 | 1 | POP P0:0 |
| | | | <dregs> | 1 | 1 | POP D0:1 |
| | | | <regind> | 1 | 1 | POP @P0:0 |
| | | | <hwregs> | 1 | 1 | POP A |
| PUSH | Push value onto stack | PUSH <src> | <pregs> | 1 | 1 | PUSH P0:0 |
| | | | <dregs> | 1 | 1 | PUSH D0:1 |
| | | | <regind> | 1 | 1 | PUSH @P0:0 |
| | | | <hwregs> | 1 | 1 | PUSH BUS |
| | | | <limm> | 2 | 2 | PUSH #12345 |
| | | | <accind> | 1 | 3 | PUSH @A |
| | | | <memind> | 1 | 3 | PUSH @@P0:0 |
| RET | Return from subroutine | RET | None | 1 | 2 | RET |
| RL | Rotate Left | RL <cc>,A | <cc>,A | 1 | 1 | RL NZ,A |
| | | | A | 1 | 1 | RL A |
| RR | Rotate Right | RR <cc>,A | <cc>,A | 1 | 1 | RR C,A |
| | | | A | 1 | 1 | RR A |
| SCF | Set C flag | SCF | None | 1 | 1 | SCF |
| SIEF | Set IE flag | SIEF | None | 1 | 1 | SIEF |
| SLL | Shift left logical | SLL | [<cc>,]A | 1 | 1 | SLL NZ,A |
| | | | A | 1 | 1 | SLL A |
| SOPF | Set OP flag | SOPF | None | 1 | 1 | SOPF |
| SRA | Shift right arithmetic | SRA<cc>,A | <cc>,A | 1 | 1 | SRA NZ,A |
| | | | A | 1 | 1 | SRA A |
| SUB | Subtract | SUB<dest>,<src> | A,<pregs> | 1 | 1 | SUB A,P1:1 |
| | | | A,<dregs> | 1 | 1 | SUB A,D0:1 |
| | | | A,<limm> | 2 | 2 | SUB A,#%2C2C |
| | | | A,<memind> | 1 | 3 | SUB A,@D0:1 |
| | | | A,<direct> | 1 | 1 | SUB A,%15 |
| | | | A,<regind> | 1 | 1 | SUB A,@P2:0–LOOP |
| | | | A,<hwregs> | 1 | 1 | SUB A,STACK |
| | | | A,<simm> | 1 | 1 | SUB A, #%12 |