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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	SPI, 3-Wire Serial
Clock Rate	20MHz
Non-Volatile Memory	OTP (16kB)
On-Chip RAM	1kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8937320vsc00tr

PIN FUNCTIONS

EA2–EA0. External Address Bus (output, latched). These pins provide the External Register Address. This address bus is driven during both internal and external accesses. One of up to seven user-defined external registers is selected by the processor for reads or writes. EXT7 is always reserved for use by the processor.

ED15–ED0. External Data Bus (input/output). These pins are the data bus for the user-defined external registers, and are shared by Port0. These pins are normally tristated, except when these registers are specified as destination registers in a write instruction to an external peripheral, or when Port0 is enabled for output. This bus uses the control signals RD/$\overline{WR}$, $\overline{DS}$, and $\overline{WAIT}$, and address pins EA2–EA0.

$\overline{DS}$. Data Strobe (output). This pin provides the data strobe signal for the ED Bus. $\overline{DS}$ is active for transfers to/from external peripherals only.

RD/$\overline{WR}$. Read/$\overline{Write}$ Select (output). This pin controls the data direction signal for the External Data Bus. Data is available from the processor on ED15–ED0 when this signal and $\overline{DS}$ are both Low.

$\overline{WAIT}$. Wait State (input). This pin is sampled at the rising edge of the clock with appropriate setup and hold times. A single wait-state can be generated internally by setting the appropriate bits in the wait state register. The user must drive this line if multiple wait states are required. This pin is shared with Port2.

CLKI. Clock (input). This pin is the clock circuit input. It can be driven by a signal or connected to a 32 KHz crystal.

CLKO. Clock (output). This pin is the clock circuit output. It is used for operation with a 32 KHz crystal and the PLL to generate the system clock.

$\overline{HALT}$. Halt State (input). This pin stops program execution. The processor continuously executes NOPs and the program counter remains constant while this pin is held Low. This pin offers an internal pull-up.

$\overline{RESET}$. Reset (input). This pin resets the processor. It pushes the contents of the Program Counter (PC) onto the stack and then fetches a new PC value from program memory address 0FFCH after the $\overline{RESET}$ signal is released. The Status register is set to all zeros. At power-up RAM and other registers are undefined, however, they are left unchanged with subsequent resets. $\overline{RESET}$ can be asserted asynchronously.

AN0–AN3. Analog Inputs (input). These are the analog input pins. The analog input signal should be between VALO and VAHI for accurate conversions.

VAHI. Analog High Reference Voltage (input). This pin provides the reference for the full scale voltage of the analog input signals.

VALO. Analog Low Reference Voltage (input). This pin provides the reference for the zero voltage of the analog input signals.

AV_{CC}–AGND. Filtered Analog Power and Ground must be provided on separate pins to reduce digital noise in the analog circuits.

Multifunction Pins. The Z89223/273/323/373 DSP family offers a user-configurable I/O structure, which means that most of the I/O pins offer dual functions. The function, direction (input or output), and for output, the characteristics (push-pull or open drain) are all under user-control, by programming the configuration registers appropriately as described in the I/O Ports section. The following share I/O Port pins:

INT0–INT2. External Interrupts (input, edge-triggered). These pins provide three of the eight interrupt sources to the Interrupt Controller. Each is programmable to be rising-edge or falling-edge triggered. The other five interrupt sources are from the on-chip peripherals.

CLKOUT. System Clock (output). This pin provides access to the internal processor clock.

SDI. Serial Data In (input). This pin is the SPI serial data input.

SDO. Serial Data Out (output). This pin is the SPI serial data output.

SS. Slave Select (input). This pin is used in SPI Slave Mode only. SS advises the SPI that it is the target of a serial transfer from an external Master.

SCLK. SPI Clock (output/input). This pin is an output in Master mode and an input in Slave mode.

UI0, UI1. User inputs (input). These general-purpose input pins are directly tested by the conditional branch instructions. They can also be read as bits in the status register. These are asynchronous input signals that require no special clock synchronization. Counter/Timer0 and Counter/Timer1 may use either of these pins as input.

UI2. User Input (input). This pin is the input to Counter/Timer 2.

TMO0/UO0. Counter/Timer Output or User Output 0 (output). Counter/Timer 0 and Counter/Timer 1 can be programmed to provide output on this pin. When User Outputs are enabled, and the Counter/Timer is disabled, this pin provides the complement of Status Register bit 5.

TMO1/UO1. Counter/Timer Output or User Output 1 (output). Counter/Timer 0 and Counter/Timer 1 can be programmed to provide output on this pin. When User Outputs are enabled, and the Counter/Timer is disabled, this pin provides the complement of Status Register bit 6.

TMO2. Counter/Timer 2 Output (output). This pin is the output of Counter/Timer 2

P0.15–P0.0. Port0 (input/output). This is a 16-bit user I/O port. Bits can be configured as input or output or globally as open-drain output. When enabled, Port0 uses the 16 data lines of the ED bus. The function of these pins can be dynamically changed by writing to the Port0 configuration registers. The High byte can also be configured to Port1 as described in the I/O Port section.

P1.7–P1.0. Port1 (input/output). These pins are Port1 inputs or outputs when not configured for use as special purpose peripheral interface. The following eight pin functions preempt use of these pins when enabled. INT2, CLKOUT, SDI, SDO, SS, SCLK, UI0, UI1.

Note: These pins are not bonded out on the 44-pin packages.

P2.7–P2.0. Port2 (input/output). These pins are Port2 inputs or outputs when not configured as peripheral interfaces. The following seven pin functions preempt use of P2.6–P2.0 when enabled. INT0, INT1, TMO0/UO0, TMO1/UO1, $\overline{\text{WAIT}}$, UI2, TMO2. P2.7 does not include a dual function.

Note: P2.7–P2.5 are not bonded out on the 44-pin packages.

The following port pins are available only on the 80-pin package:

P3.7–P3.4. Port3 (output). These pins are Port3 outputs.

P3.3–P3.0. Port3 (input). These pins are Port3 inputs.

PIN CONFIGURATIONS (Continued)

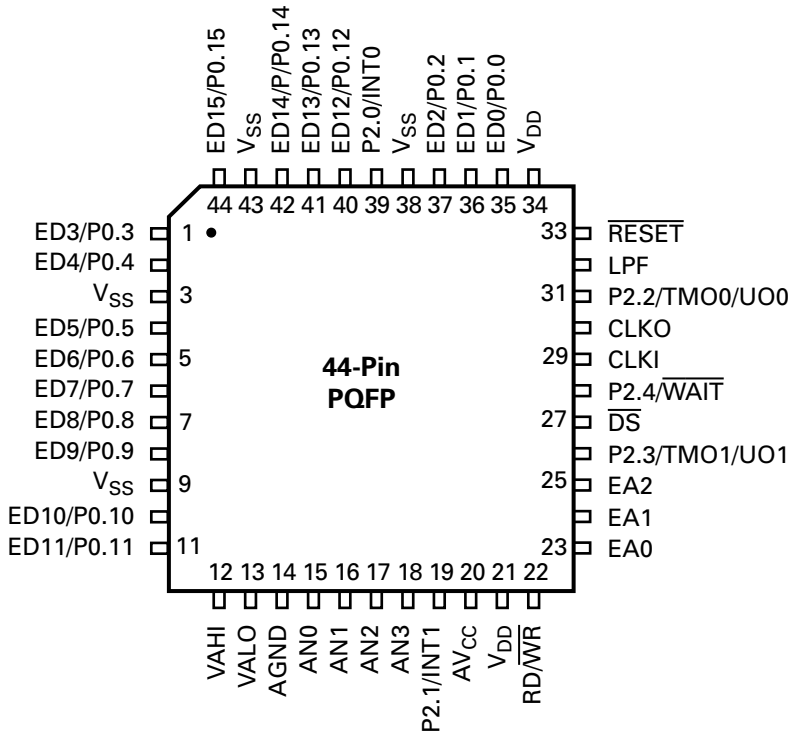


Figure 4. 44-Pin PQFP Z89223/273 Pin Configuration

Table 2. 44-Pin PQFP Z89223/273 Pin Description

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	ED3/P0.3	External Data Bus/Port0	Input/Output	23	EA0	Ext Address 0	Output
2	ED4/P0.4	External Data Bus/Port0	Input/Output	24	EA1	Ext Address 1	Output
3	V_{SS}	Ground		25	EA2	Ext Address 2	Output
4	ED5/P0.5	External Data Bus/Port0	Input/Output	26	P2.3/TMO1	Port 2.3/Timer Output 1	Input/Output
5	ED6/P0.6	External Data Bus/Port0	Input/Output	27	$\overline{DS}$	Ext Data Strobe	Output
6	ED7/P0.7	External Data Bus/Port0	Input/Output	28	P2.4/$\overline{WAIT}$	Port 2.4/Wait for ED	Input/Output
7	ED8/P0.8	External Data Bus/Port0	Input/Output	29	CLKI	Clock/Crystal In	Input
8	ED9/P0.9	External Data Bus/Port0	Input/Output	30	CLKO	Clock/Crystal Out	Output
9	V_{SS}	Ground		31	P2.2/TMO0	Port 2.2/Timer Output 0	Input/Output
10	ED10/P0.10	External Data Bus/Port0	Input/Output	32	LPF	PLL Low Pass Filter	Input
11	ED11/P0.11	External Data Bus/Port0	Input/Output	33	$\overline{RESET}$	Reset	Input
12	VAHI	Analog High Ref. Voltage	Input	34	V_{DD}	Power Supply	
13	VALO	Analog Low Ref. Voltage	Input	35	ED0/P0.0	External Data Bus/Port0	Input/Output
14	AGND	Analog Ground		36	ED1/P0.1	External Data Bus/Port0	Input/Output
15	AN0	A/D Input 0	Input	37	ED2/P0.2	External Data Bus/Port0	Input/Output
16	AN1	A/D Input 1	Input	38	V_{SS}	Ground	
17	AN2	A/D Input 2	Input	39	P2.0/INT0	Port 2.0/Interrupt 0	Input/Output
18	AN3	A/D Input 3	Input	40	ED12/P0.12	External Data Bus/Port0	Input/Output
19	P2.1/INT1	Port 2.1/Interrupt 1	Input/Output	41	ED13/P0.13	External Data Bus/Port0	Input/Output
20	AV_{CC}	Analog Power		42	ED14/P0.14	External Data Bus/Port0	Input/Output
21	V_{DD}	Power		43	V_{SS}	Ground	
22	RD/$\overline{WR}$	R/W Exteral Output Bus		44	ED15/P0.15	External Data Bus/Port0	Input/Output

Table 3. 64-Pin TQFP Z89223/273 Pin Description

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	ED3/P0.3	External Data Bus/Port0	Input/Output	33	$\overline{HALT}$	Halt Execution	Input
2	ED4/P0.4	External Data Bus/Port0	Input/Output	34	EA0	Ext Address 0	Output
3	V_{SS}	Ground		35	EA1	Ext Address 1	Output
4	V_{DD}	Power Supply		36	EA2	Ext Address 2	Output
5	ED5/P0.5	External Data Bus/Port0	Input/Output	37	V_{DD}	Power Supply	
6	P1.3/SDO	Port 1.3/Serial Output	Input/Output	38	P2.3/TMO1	Port2.3/Timer Output 1	Input/Output
7	ED6/P0.6	External Data Bus/Port0	Input/Output	39	$\overline{DS}$	Ext Data Strobe	Output
8	P1.4/SS	Port 1.4/Slave Select	Input/Output	40	P2.4/$\overline{WAIT}$	Port 2.4/Wait for ED	Input/Output
9	ED7/P0.7	External Data Bus/Port0	Input/Output	41	CLKI	Clock/Crystal In	Input
10	P1.5/SCLK	Port 1.5/Serial Clock	Input/Output	42	CLKO	Clock/Crystal Out	Output
11	P2.7	Port 2.7	Input/Output	43	P2.6/TMO2	Port 2.6/Timer Output 2	Input/Output
12	ED8/P0.8	External Data Bus/Port0	Input/Output	44	P2.2/TMO0	Port 2.2/Timer Output 0	Input/Output
13	ED9/P0.9	External Data Bus/Port0	Input/Output	45	P2.5/UI2	Port 2.5/User Input 2	Input/Output
14	V_{SS}	Ground		46	LPF	PLL Low Pass Filter	Input
15	ED10/P0.10	External Data Bus/Port0	Input/Output	47	$\overline{RESET}$	Reset	Input
16	V_{SS}	Ground		48	V_{SS}	Ground	
17	ED11/P0.11	External Data Bus/Port0	Input/Output	49	V_{DD}	Power Supply	
18	VAHI	Analog High Ref. Voltage	Input	50	V_{SS}	Ground	
19	V_{SS}	Ground		51	ED0/P0.0	External Data Bus/Port0	Input/Output
20	P1.6/UI0	Port 1.6/User Input 0	Input/Output	52	ED1/P0.1	External Data Bus/Port0	Input/Output
21	VALO	Analog Low Ref. Voltage	Input	53	ED2/P0.2	External Data Bus/Port0	Input/Output
22	P1.7/UI1	Port 1.7/User Input 1	Input/Output	54	P1.0/INT2	Port 1.0/Interrupt 2	Input/Output
23	AGND	Analog Ground		55	V_{SS}	Ground	
24	AN0	A/D Input 0	Input	56	P1.1/CLKOUT	Port 1.1/Clock Output	Input/Output
25	AN1	A/D Input 1	Input	57	P1.2/SDI	Port 1.2/Serial Input	Input/Output
26	AN2	A/D Input 2	Input	58	P2.0/INT0	Port 2.0/Interrupt 0	Input/Output
27	AN3	A/D Input 3	Input	59	ED12/P0.12	External Data Bus/Port0	Input/Output
28	V_{SS}	Ground		60	ED13/P0.13	External Data Bus/Port0	Input/Output
29	P2.1/INT1	Port 2.1/Interrupt 1	Input/Output	61	V_{DD}	Power Supply	
30	AVCC	Analog Power		62	ED14/P0.14	External Data Bus/Port0	Input/Output
31	V_{DD}	Power Supply		63	V_{SS}	Ground	
32	RD/$\overline{WR}$	R/W External Bus	Output	64	ED15/P0.15	External Data Bus/Port0	Input/Output

PIN CONFIGURATIONS (Continued)

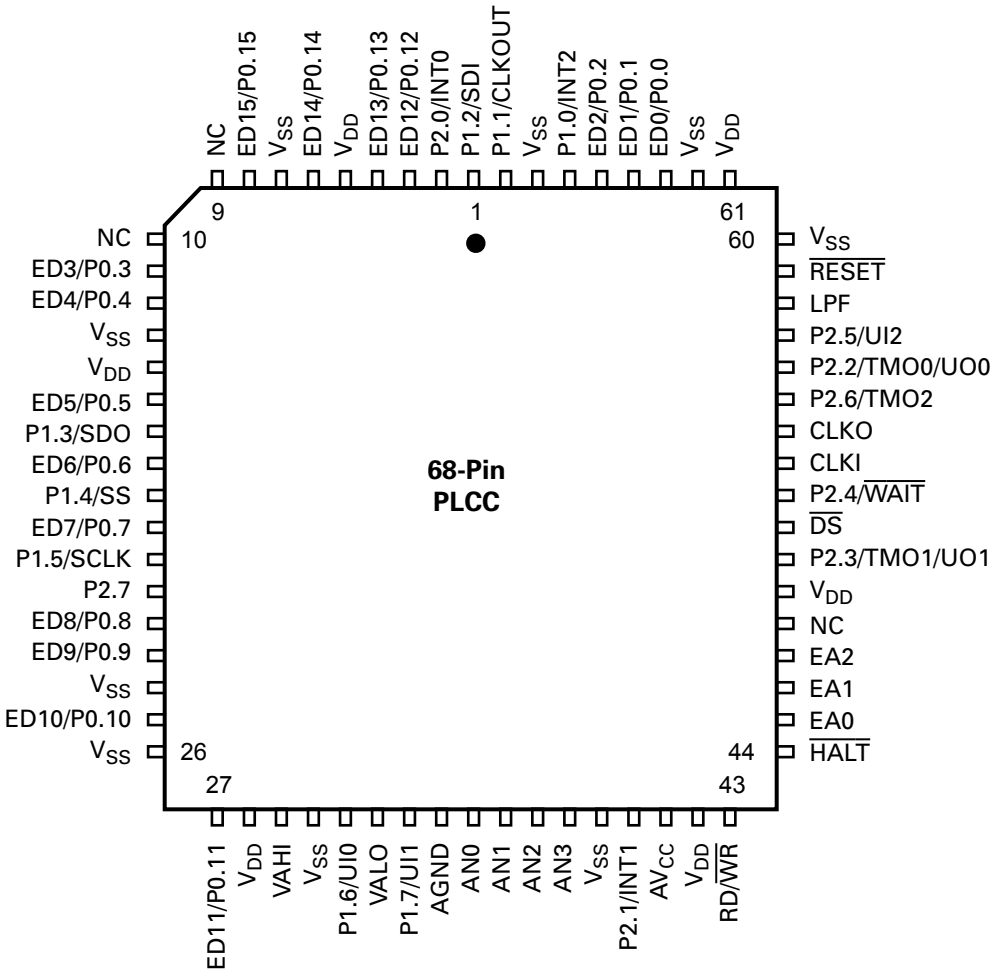


Figure 6. 68-Pin PLCC Z89323/373 Pin Configuration

PIN CONFIGURATIONS (Continued)

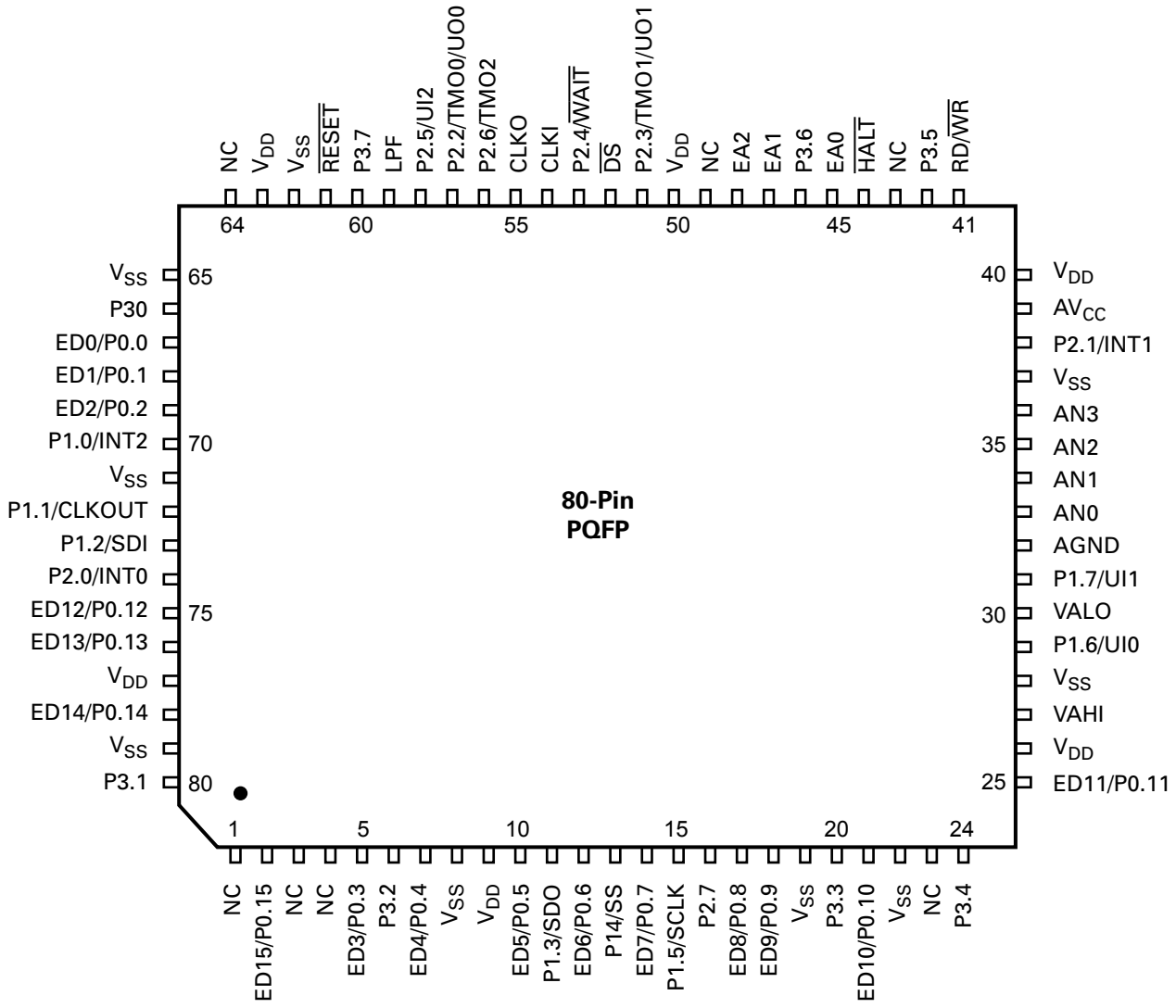
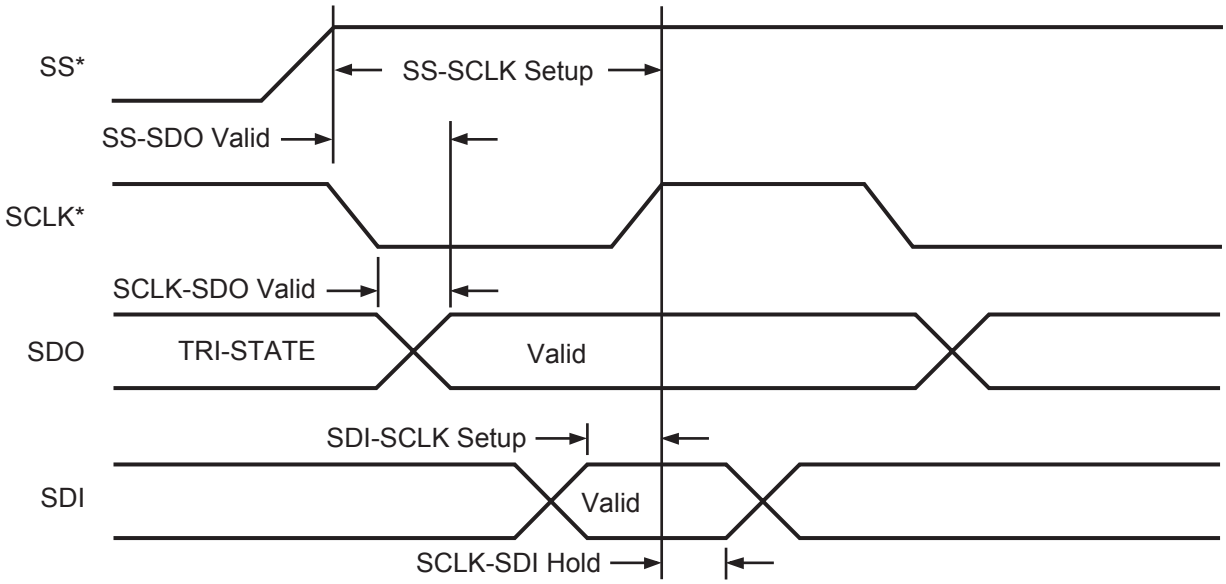


Figure 7. 80-Pin PQFP Z89323/373 Pin Configuration



*Notes: The polarity of SCLK and SS are programmable by the user. SS is used in Slave Mode only. This figure illustrates data transmission on the falling edge of SCLK, data reception on the rising edge of SCLK, with SS active Low (default).

Figure 15. SPI Timing (Master and Slave Modes)

FUNCTIONAL DESCRIPTION

Instruction Timing. Most instructions are executed in one machine cycle. A multiplication or multiply/accumulate instruction requires a single cycle. Long immediate instructions, and Jump or Call instructions, are executed in two machine cycles. Specific instruction cycle times are described in the Instruction Description section.

Multiply/Accumulate. The multiplier can perform a 16-bit x 16-bit multiply, or multiply/accumulate, in one machine cycle using the Accumulator and/or both the X and Y inputs. The multiplier produces a 32-bit result, however, only the 24 most significant bits are saved for the next instruction or accumulation. For operations on very small numbers where the least significant bits are important, the data should first be scaled to avoid truncation errors.

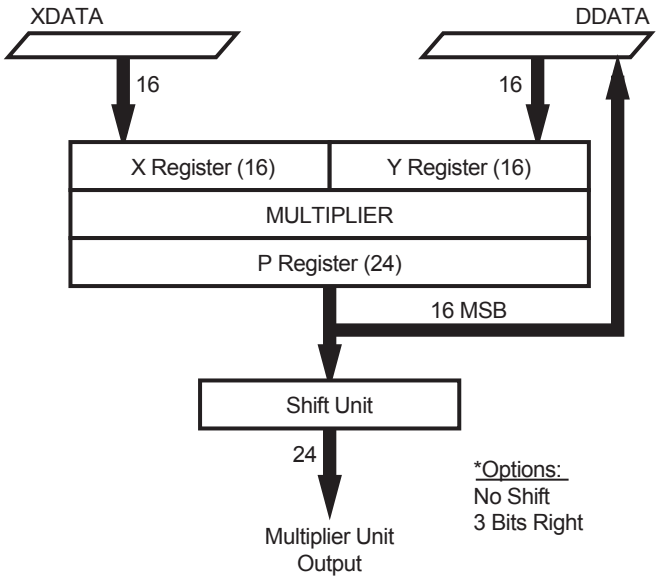


Figure 16. Multiplier Block Diagram

All inputs to the multiplier should be fractional two's-complement, 16-bit binary numbers, which places them in the range [–1 to 0.9999695]. The result is in 24 bits, so the range is [–1 to 0.9999999].

If 8000H is loaded into both the X and Y registers, the multiplication produces an incorrect result. Positive one cannot be represented in fractional notation, and the multiplier actually yields the result 8000H x 8000H = 8000H (–1 x –1 = –1). The user should avoid this case to prevent erroneous results.

A shifter between the P Register and the Multiplier Unit Output can shift the data by three bits right or no shift.

Data Bus Bank Switch. There is a switch that connects the X Bus to the DDATA Bus that allows both the X and Y registers to be loaded with the same operand for a one cycle squaring operation. The switch is also used to read the X register.

ALU. The ALU features two input ports. One is connected to the output of the 24-bit Accumulator. The other input selects either the Multiplier Unit Output or the 16-bit DDATA bus (left-justified with zeros in the eight LSBs). The ALU performs arithmetic, logic, and shift operations.

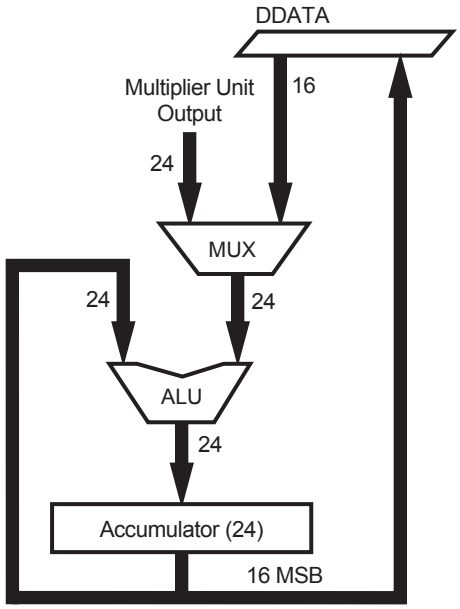


Figure 17. ALU Block Diagram

Hardware Stack. A six-level hardware stack is connected to the DDATA bus to hold subroutine return addresses or data. The CALL instruction pushes PC+2 onto the stack, and the RET instruction pops the contents of the stack to the PC.

User Inputs and Outputs. The Z893x3 features three User Inputs, UI0, UI1, and UI2. Pins UI0 and UI1 are connected directly to status register bits S10 and S11, and can be read, or used as a condition code in any conditional instruction. Pins UI0, UI1 and UI2 may also be used to clock the Counter/Timers. There are two user output bits, UO0 and UO1, which share pins with the timer outputs TMO0 and TMO1 on Port2. When the User Outputs are enabled, they are the complements of bits S5 and S6 of the Status Register.

Interrupts. The Z893x3 features three user interrupt inputs which can be programmed to be positive or negative edge-triggered. There are five interrupts generated by internal peripherals: the A/D converter, the Serial Peripheral Interface, and the three Counter/Timers. Internally there are three priority levels. The internal signals for Interrupt service Requests are denoted ISR0, ISR1, and ISR2, with ISR0 having the highest priority, and ISR2 the lowest. The user can program which interrupt sources are enabled, and which sources are serviced by the highest, middle, and lowest priority service routines. An interrupt is serviced at the end of an instruction execution. Two machine cycles are required to enter an interrupt instruction sequence. The PC is pushed onto the stack. The Interrupt Controller fetches the address of the interrupt service routine from the following locations in program memory:

Device	ISR0	ISR1	ISR2
Z89223/273/323/373	1FFFH	1FFEH	1FFDH

At the end of the interrupt service routine, a RET instruction is used to pop the stack into the PC.

The Set-Interrupt-Enable-Flag (SIEF) instruction enables the interrupts. Interrupts are automatically disabled when entering an interrupt service routine. Before exiting an interrupt service routine the SIEF instruction can be used to reenable interrupts.

Registers. In addition to the internal registers for processing, control, and configuration, the Z893x3 offers up to seven user-defined 16-bit external registers, EXT0–EXT6, depending on the Register Bank Select value. The external register address space is shared by the Z893x3 internal peripherals. Selecting banks 0–4 of the EXT Register Assignment allows access to/from three to seven of these addresses for general-purpose use.

I/O Ports. The Z893X3 DSP family features a user-configurable I/O structure. Most of the I/O pins include dual functions. The Counter/Timer, Serial Peripheral Interface, and External Interrupt Enables determine whether a pin is dedicated to peripheral or I/O port use.

Port0. A 16-bit user I/O port. Bits can be configured as input or output or globally as open-drain output. When enabled, Port0 consumes the 16 data lines used by the ED bus. Port0 function and ED bus use can be dynamically alternated by enabling and disabling Port0.

Port1. A multifunctional 8-bit port. Bits can be configured as input or output or globally as open-drain output. Port1 also supports INT2, CLKOUT, the Serial Peripheral Interface, and User Inputs 0 and 1.

Port2. A multifunctional 8-bit port. Bits can be configured as input or output or globally as open-drain output. Port2 also supports INT0 and INT1, all three Counter/Timer outputs, ED Bus, $\overline{WAIT}$, and UI2.

Port3. Port3 is an 8-bit user I/O port with 4 bits of input and 4 bits of output. It is available only on the 80-pin package.

External Register Usage. The external registers EXT0–EXT6 are accessed using the External Address Bus EA2–EA0, the External Data Bus (ED Bus) ED15–ED0, and control signals $\overline{DS}$, $\overline{WAIT}$, and RD/$\overline{WR}$. These provide a convenient data transfer capability with external peripherals. Data transfers can be performed in a single-cycle. An internal wait state generator is provided to accommodate slower external peripherals. A single wait state can be implemented through control register Bank15/EXT3. For additional wait states, the $\overline{WAIT}$ pin can be used. The $\overline{WAIT}$ pin is monitored only during execution of a read or write instruction to external peripherals on the ED bus.

Wait-State Generator. An internal Wait-State generator is provided to accommodate slow external peripherals. A single Wait-State can be implemented through a control register. For additional states, a dedicated pin ($\overline{WAIT}$) can be held Low. The $\overline{WAIT}$ pin is monitored only during execution of a read or write instruction to external peripherals (ED bus).

Analog to Digital Converter. The A/D Converter is a 4-channel, 8-bit half-flash converter. Two external reference voltages provide a scalable input range. The A/D sample rate is determined by a prescaler connected to the system clock. An interrupt is optionally generated at the end of a conversion. The four input channels can be programmed to operate on demand, continuously, or upon an event (timer or interrupt).

Counter/Timers (C/T0 and C/T1). These C/Ts are 16-bit with 8-bit prescalers. They also offer the option of being used as PWM generators and include both hardware and software Watch-Dog capabilities. Both C/Ts are identical and can be externally or internally clocked. Either C/T can drive TMO0 or TMO1. Either C/T can drive any of the three interrupt service requests (ISR0, ISR1, or ISR2).

Counter/Timer (C/T2). This C/T is 16-bits, externally or internally clocked, and can drive TMO2 and/or any of the three interrupt service requests (ISR0, ISR1, or ISR2).

Serial Peripheral Interface (SPI). The Serial Peripheral Interface provides a convenient means of inter-processor and processor-peripheral communication. It offers the capability to transmit and receive simultaneously. The SPI is designed to operate in either master or slave mode.

BANK/EXT REGISTER ASSIGNMENTS (Continued)

Interrupt Polarity Register—Bank14/EXT6

The trigger polarities, rising-edge or falling-edge, of all the external interrupts are programmable.

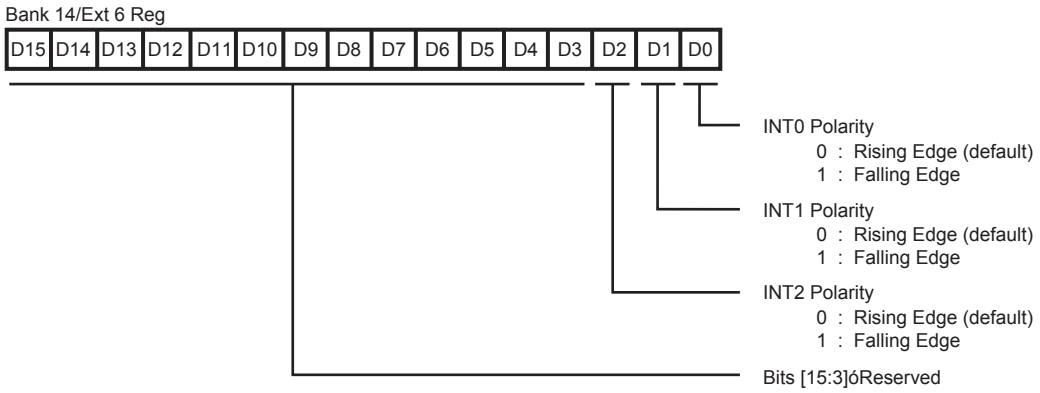


Figure 22. Interrupt Polarity Register

Wait-State Control Register—Bank15/EXT3

The Wait-State Control Register enables the insertion of wait states when the DSP accesses slow peripherals. This register enables the insertion of one wait state on the ED bus, providing 100 ns of access time instead of 50 ns when operating at 20 MHz. When more than one wait state is necessary, input pin P2.4/ $\overline{\text{WAIT}}$ can be used to provide additional wait states. The Wait-State Register enables the user to specify which EXT registers, EXT0–EXT6, and which operation, read and/or write, require a wait state. EXT7 is an internal register, and requires no wait state.

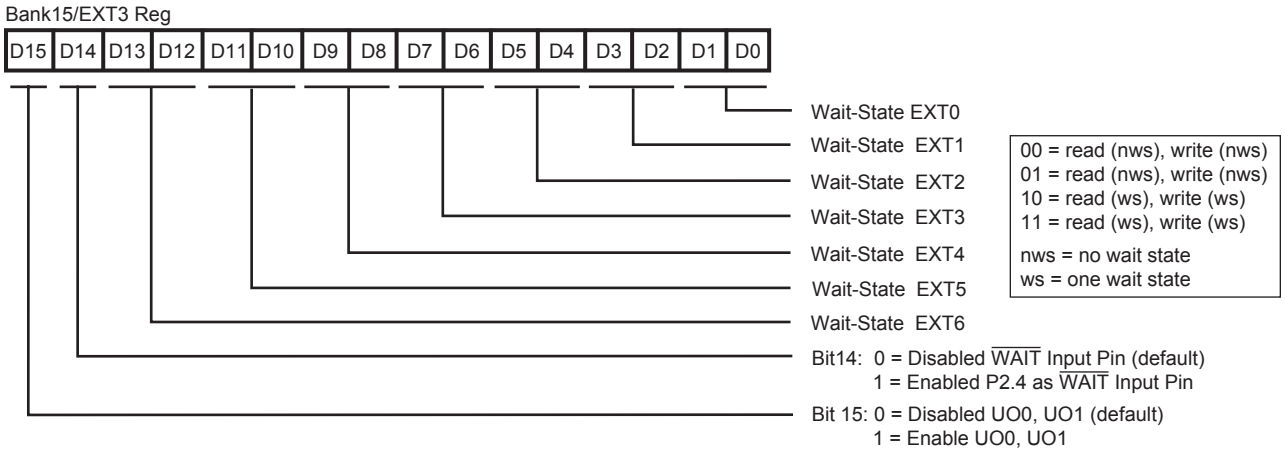


Figure 23. Wait-State Control Register

I/O PORTS (Continued)

Port0—16-Bit Programmable I/O

Bank15/EXT0 is the Port0 direction control register. Bank15/EXT1 includes specific bits to enable and configure Port0. The Port0 data register is Ext4 in Banks 0, 1, or 5.

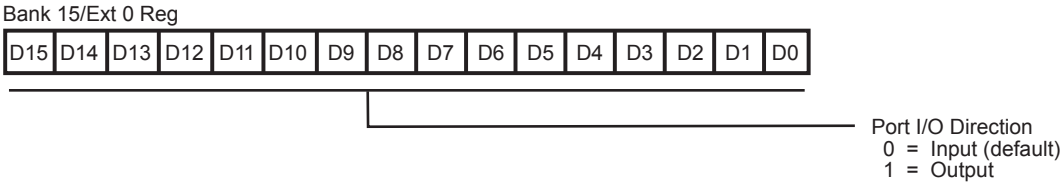


Figure 25. Port 0 Control Register

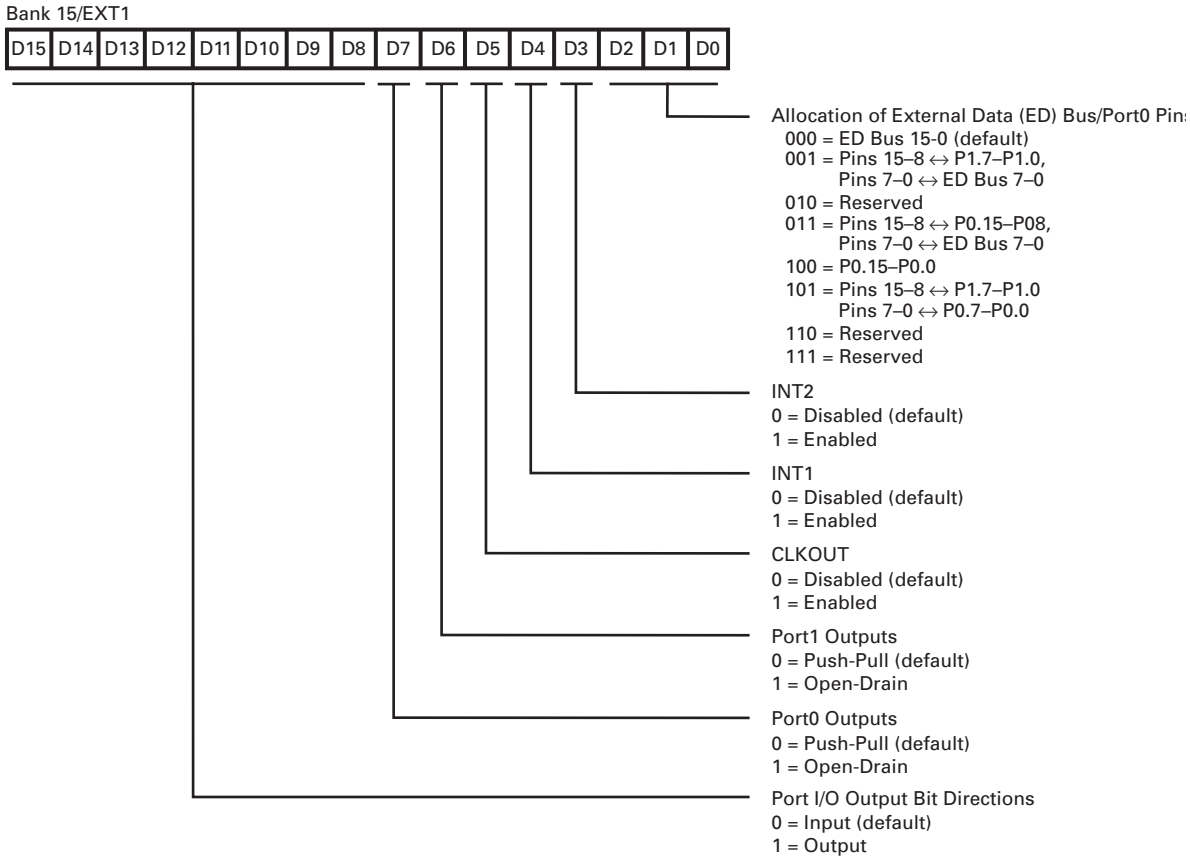


Figure 26. Bank15/EXT1 Register

Port1—8-Bit Programmable I/O

Bank15/EXT1 is the Port1 control register. The MSB is the Port1 direction control. Port1 data is accessed as the LSB of EXT5 in Banks 0, 1, or 5. The Port1 pins can also be mapped to internal functions. When INT2, CLKOUT, UI0 and UI1, or the SPI are enabled, they use Port1 pins. The 44-pin packages do not feature Port1 pins, however, Port1 and its internal functions can be mapped to the MSB of the ED Bus/Port0 pins. See bits 2–0 of Bank15/EXT1.

Table 16. Port1 Bit Function Allocation

Port Pin	IF	Condition	Then	Else
P1.0/INT2	Bank15/EXT1 Bit 3 = 1	Enable INT2	INT2	P1.0
P1.1/CLKOUT	Bank15/EXT1 Bit 5 = 1	Enable CLKOUT	CLKOUT	P1.1
P1.2/SDI	Bank15/EXT4 Bit 0 = 1	Enable SPI	SDI	P1.2
P1.3/SDO	Bank15/EXT4 Bit 0 = 1	Enable SPI	SDO	P1.3
P1.4/SS	Bank15/EXT4 Bit 0 = 1	Enable SPI	SS	P1.4
P1.5/SCLK	Bank15/EXT4 Bit 0 = 1	Enable SPI	SCLK	P1.5
P1.6/UI0	Bank13/EXT1 Bits [2,1] = 10, or Bank14/EXT1 Bits [2,1] = 10	Enable UI0	UI0	P1.6
P1.7/UI1	Bank13/EXT1 Bits [2,1] = 11, or Bank14/EXT1 Bits [2,1] = 11	Enable UI1	UI1	P1.7

PERIPHERALS

Analog to Digital Converter (A/D)

The A/D is a 4-channel 8-bit half-flash converter. It uses two reference resistor ladders, one for the upper 5 bits, and another for the lower 3 bits. Two external reference voltage input pins, VAHI and VALO, set the input voltage measurement conversion range. The converter is auto-zeroed prior to each sampling period. Bank13/EXT0 is the A/D control register.

The conversion time depends on the system clock frequency and the selection of the A/D prescaler value, bits DIV2–DIV0. The clock prescaler can be programmed to derive a 2 µs conversion time. For example, when deriving the A/D clock from a 20-MHz system clock, the A/D prescaler value should be set to divide by 40.

Bits ADST1–ADST0 determine one of the following start conversion options:

- Writing to the ADCTL control register
- ISR1
- C/T2 time-out
- C/T0 time-out

The start conversion operation may begin at any time. If a conversion is in progress, and a new start conversion signal is received, the conversion in progress will abort, and a new conversion will initiate.

Bits QUAD and SCAN determine one of the following Modes of operation:

- One channel is converted four times, with the results sequentially written to result registers 0, 1, 2 and 3.
- One channel is converted one time, with the respective result register updated.
- Four channels are converted one time each, with the respective four result registers updated.
- Four channels are converted repeatedly, with the respective four result registers constantly updated.

When one of the two four-channel modes is selected, the channel specified by CSEL1–CSEL0 will convert first. The other three channels will convert in sequence. In the sequence, AN0 follows AN3.

Bit ADIE enables the A/D to generate interrupts at the end of a conversion. Bit ADIT determines whether an interrupt occurs after the first or fourth conversion.

To reduce power consumption the A/D can be disabled by clearing the ADE bit.

Though the A/D will function with smaller input signals and reference voltages, the noise and offsets remain constant. The relative error of the converter will increase and the conversion time will also take longer.

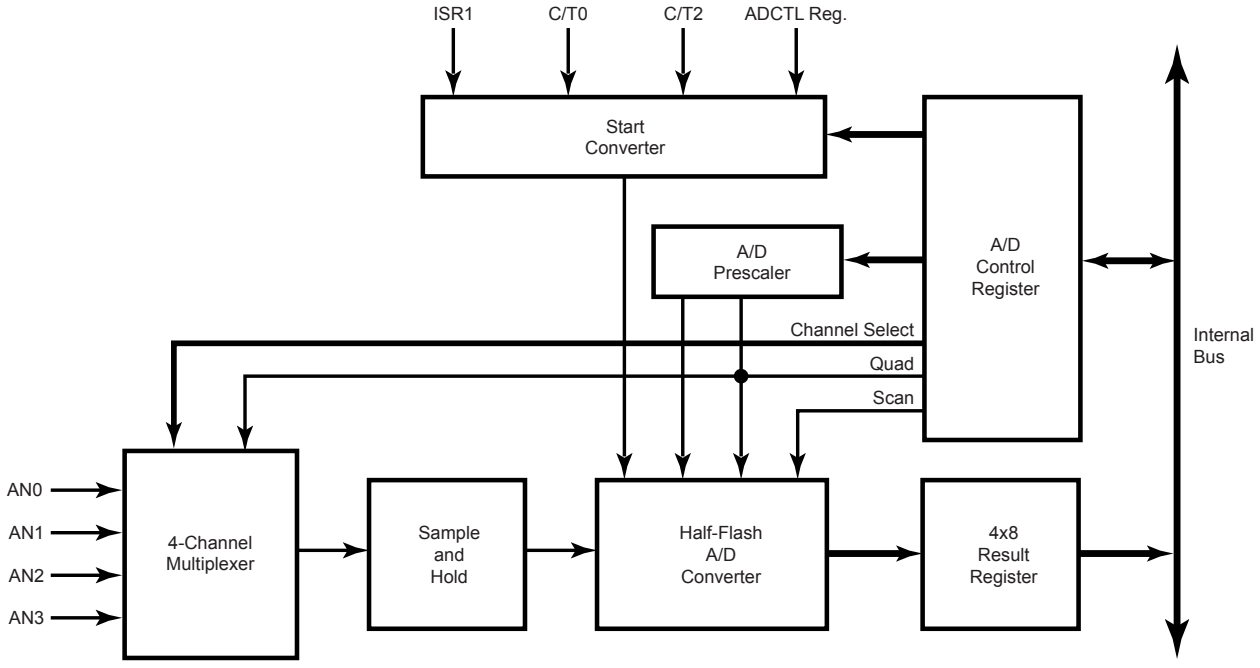


Figure 28. ADC Architecture

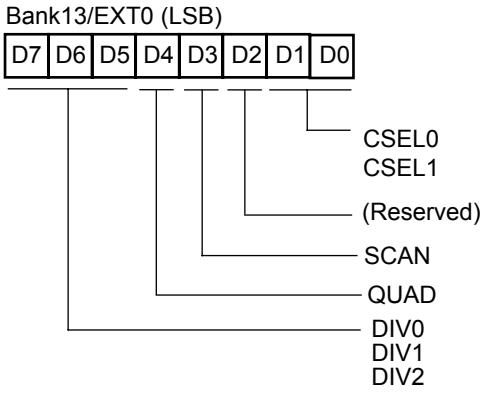


Figure 29. ADCTL Register (LSB)

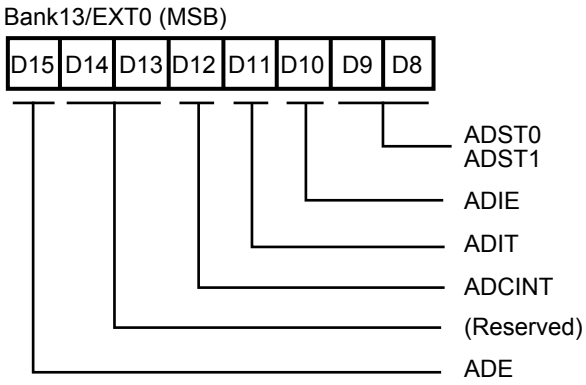


Figure 30. ADCTL Register (MSB)

Table 18. A/D Prescaler Values (Bits 7, 6, 5)

DIV2	DIV1	DIV0	A/D Prescaler (Crystal divided by)
0	0	0	8
0	0	1	16
0	1	0	24
0	1	1	32
1	0	0	40
1	0	1	48
1	1	0	56
1	1	1	64

Table 19. Operating Modes (Bits 4, 3)

QUAD	SCAN	Option
0	0	Convert selected channel 4 times, then stop
0	1	Convert selected channel, then stop.
1	0	Convert 4 channels, then stop.
1	1	Convert 4 channels continuously.

Table 20. Channel Select (Bits 1, 0)

CSEL1	CSEL0	Channel
0	0	AN0
0	1	AN1
1	0	AN2
1	1	AN3

ADE (Bit 15). A "0" disables any A/D conversions or accessing any A/D registers, except writing to the ADE bit. A "1" enables all A/D accesses.

Reserved (Bits 14, 13). Reserved for future use.

ADCINT (Bit 12). The A/D interrupt bit is read-only. The ADCINT will reset every time this register is written.

ADIT (Bit 11). Selects when to set the A/D interrupt if interrupts are enabled (ADIE=1). A value of "0" sets the interrupt after the first A/D conversion is complete. A value of "1" sets the interrupt after the fourth A/D conversion is complete.

ADIE (Bit 10). A/D Interrupt Enable. A value of "0" disables the A/D Interrupt. A value of "1" enables the A/D Interrupt.

Table 21. START (Bits 9, 8)

ADST1	ADST0	Option
0	0	Conversion starts when this register is written.
0	1	Conversion starts on INT1 per Interrupt Allocation Register
1	0	Conversion starts on C/T2 time-out.
1	1	Conversion starts on C/T0 time-out.

There are four A/D result registers. See the EXT Register Assignments for their location in the different banks.

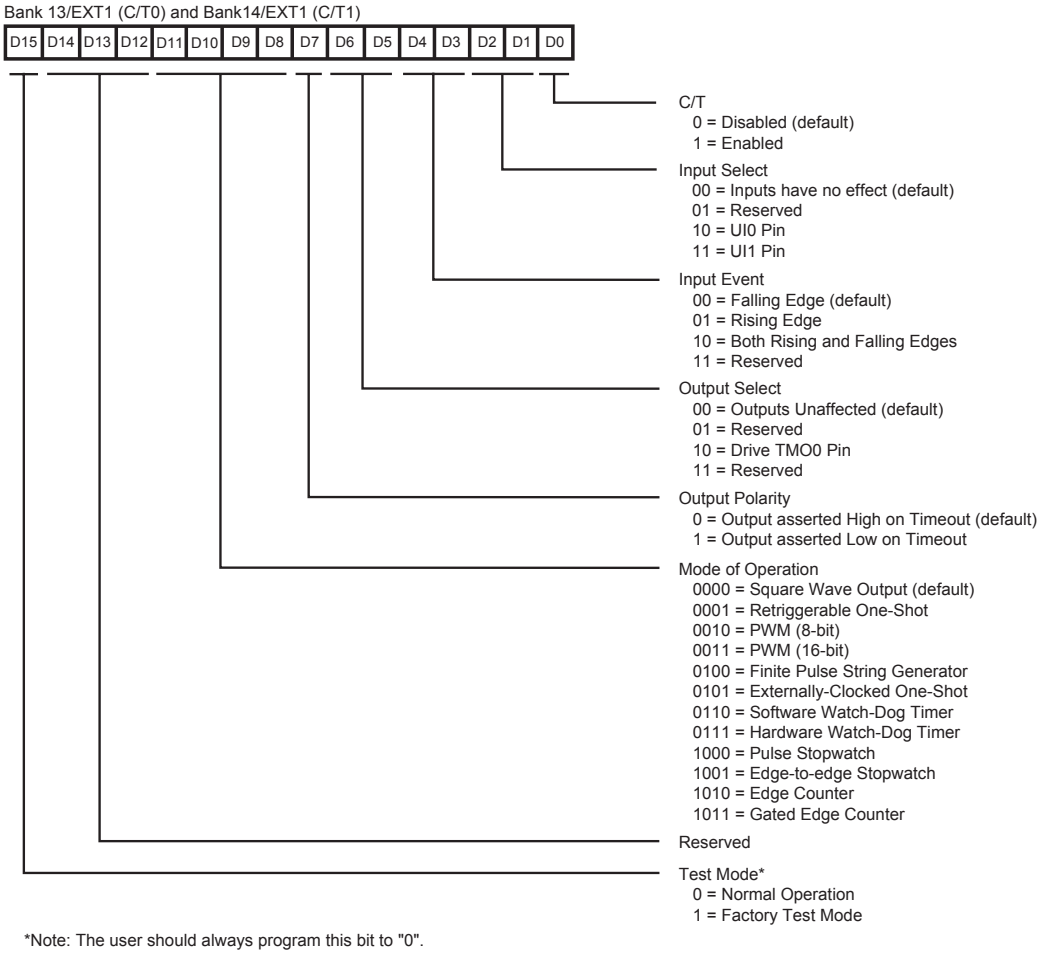


Figure 32. C/T0 and C/T1 Control Register

C/T Registers

Each C/T contains a set of five 16-bit Registers. Bank13 is used to access the registers for C/T0 and Bank14 is for the C/T1 registers. All accesses to C/T Registers occur with zero wait states.

Counter/Timer Control Register (Bank13,14/EXT1). The C/T Control register enables/disables the C/T, selects input and output options, and the mode of operation.

TMLR—Load Register (Bank13,14/EXT2). The 16-bit TMLR register holds the value that is loaded into TMR when TMR underflows.

TMR—Counter Register (Bank13,14/EXT3). TMR is a 16-bit down counter that holds the current C/T value. It can be read like any other ordinary register. However, writing to TMR is different than writing to an ordinary register. A write to TMR causes the contents of TMLR to be written into TMR, causing the C/T to be retriggered.

TPLR—Prescaler Load Register (Bank13,14/EXT4). The 16-bit TPLR register holds the prescaler load value in its lower 8 bits. Bit 15 must be written with a “1”, and bits 14–8 must be written with “0’s”.

Note: If the C/T interrupt is being used, this register must be re-written at the end of the interrupt service routine in order to enable the next interrupt. The number of clock cycles from the beginning of the interrupt service routine to the write must exceed the prescaler load value.

SERIAL PERIPHERAL INTERFACE (Continued)

Slave Mode Operation

SS must be asserted to enable a data transfer. Incoming data on the SDI pin is shifted into the SPI Shift Register one data bit per SCLK cycle. When a byte of data is received, the SPI Shift Register contents are automatically copied into RxBUF. The Receive Byte Available flag is set, and if enabled, an SPI interrupt is generated. The next byte of data may be received at this time. The current byte in RxBUF must be read before the next byte's reception is complete, or the Receive Byte Overrun flag will set, and the data in RxBUF will be overwritten. The Receive Byte Available flag is reset when RxBUF is read.

Unless the SPI output, SDO, is disabled, for every bit that is transferred into the slave through the SDI pin, a bit is transferred out through the SDO pin on the opposite clock edge. During slave operation, SCLK is an input.

Note: Slave Mode is not available on the 44-pin package.

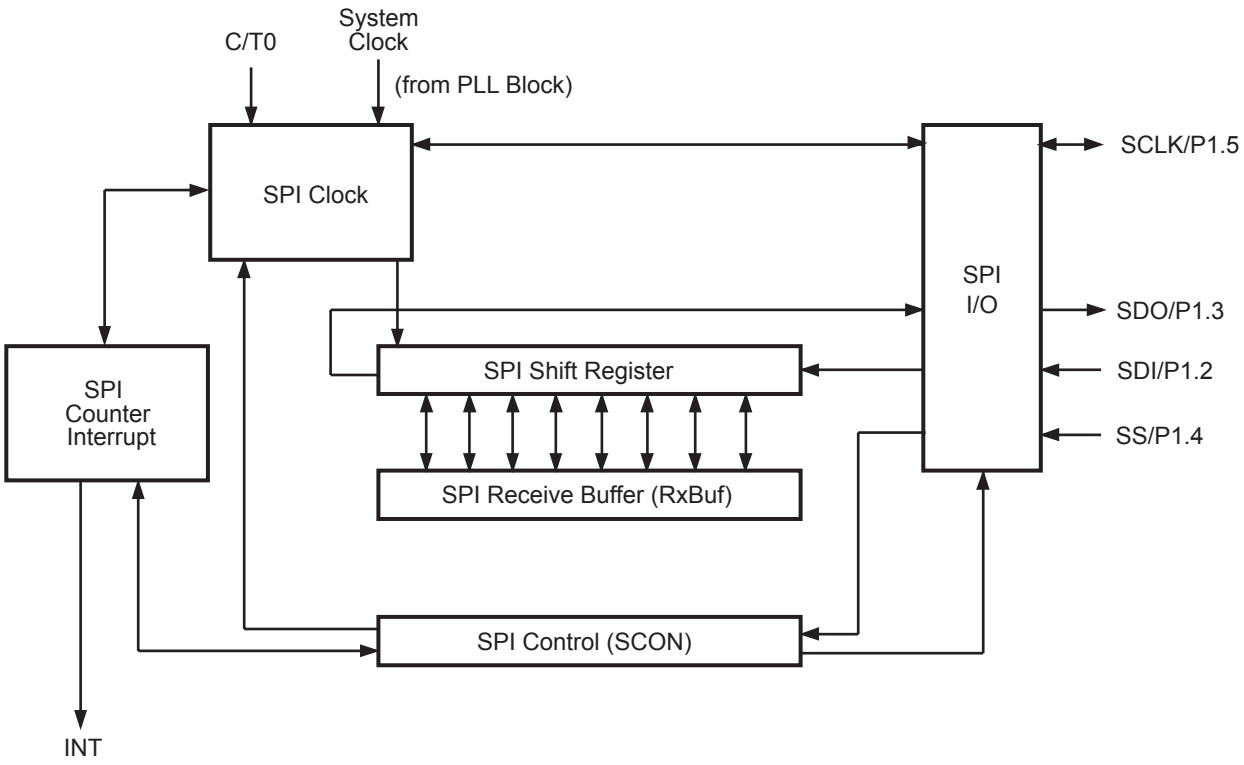


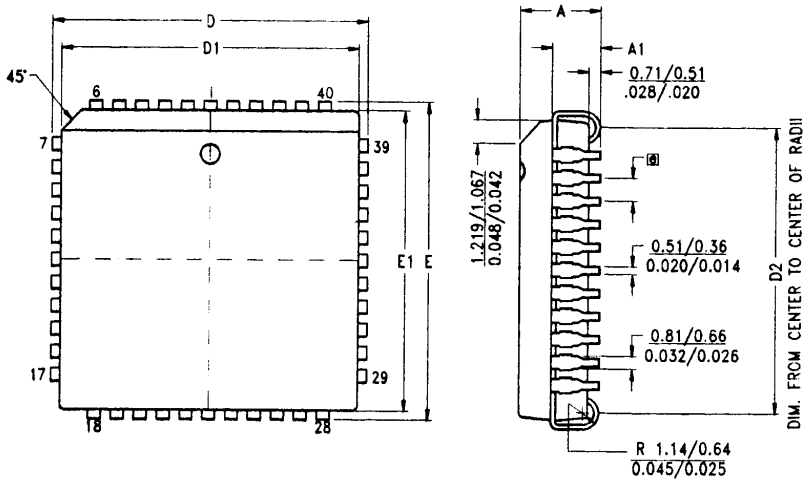
Figure 41. SPI Block Diagram

CONDITION CODES

The following Instruction Description defines the condition codes supported by the DSP assembler. If the instruction description refers to the <cc> (condition code) symbol in one of its addressing modes, the instruction only executes if the condition is true.

Code	Description
C	Carry
EQ	Equal (same as Z)
F	False
IE	Interrupts Enabled
MI	Minus
NC	No Carry
NE	Not Equal (same as NZ)
NIE	Not Interrupts Enabled
NOV	Not Overflow
NU0	Not User Zero
NU1	Not User One
NZ	Not zero
OV	Overflow
PL	Plus (Positive)
U0	User Zero
U1	User One
UGE	Unsigned Greater Than or Equal (Same as NC)
ULT	Unsigned Less Than (Same as C)
Z	Zero

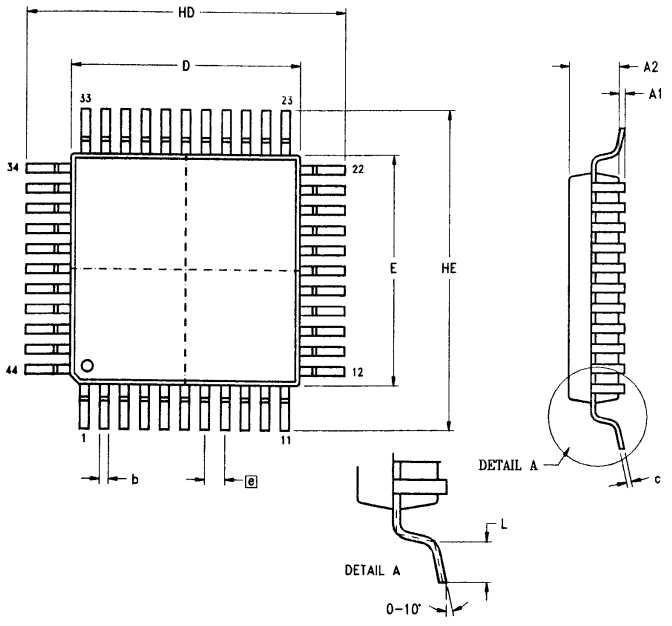
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 TYP		0.050 TYP	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM / INCH

Figure 44. 44-Pin PLCC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 TYP		.0315 TYP	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 / .004"

Figure 45. 44-Pin PQFP Package Diagram

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