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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	SPI, 3-Wire Serial
Clock Rate	20MHz
Non-Volatile Memory	OTP (16kB)
On-Chip RAM	1kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8937320vsg

GENERAL DESCRIPTION (Continued)

OTP version of the Z89223/323, is ideal for prototypes and early production builds.

Throughout this specification, references to the Z893x3 device apply equally to the Z89223/273/323/373, unless otherwise specified.

Notes: All signals with an overline are active Low. For example, in RD/$\overline{WR}$, RD is active High and $\overline{WR}$ is active Low. For I/O ports, P1.3 denotes Port1 bit 3. Pins called NC are "No Connection"—they do not connect any power, grounds, or signals.

Power connections follow conventional descriptions:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

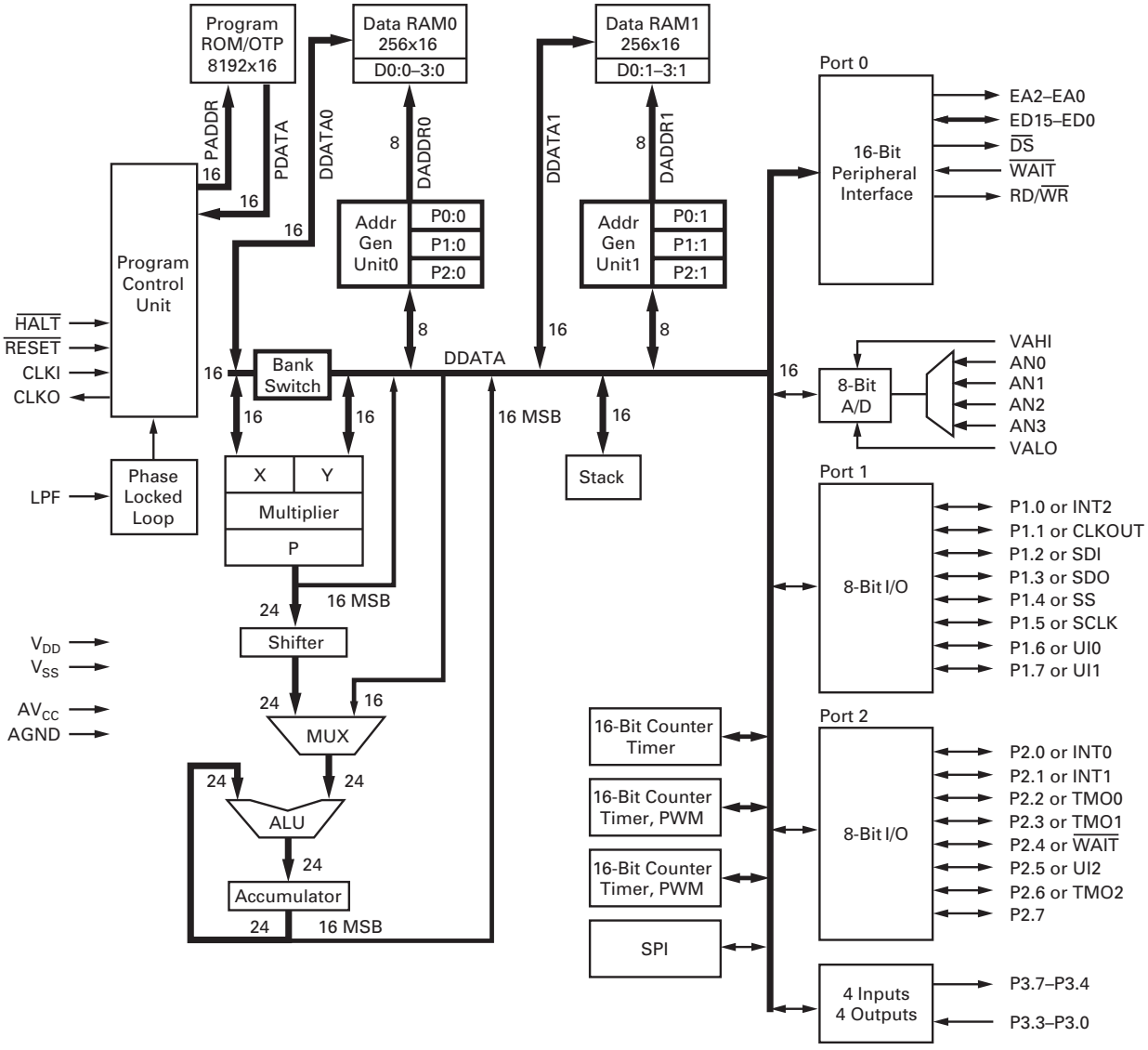


Figure 1. Z892X3/3x3 Functional Block Diagram

External Bus and External Registers. The following is made to clarify naming conventions used in this specification. The external bus and external registers are external to the DSP core, and are used to access internal and external peripherals.

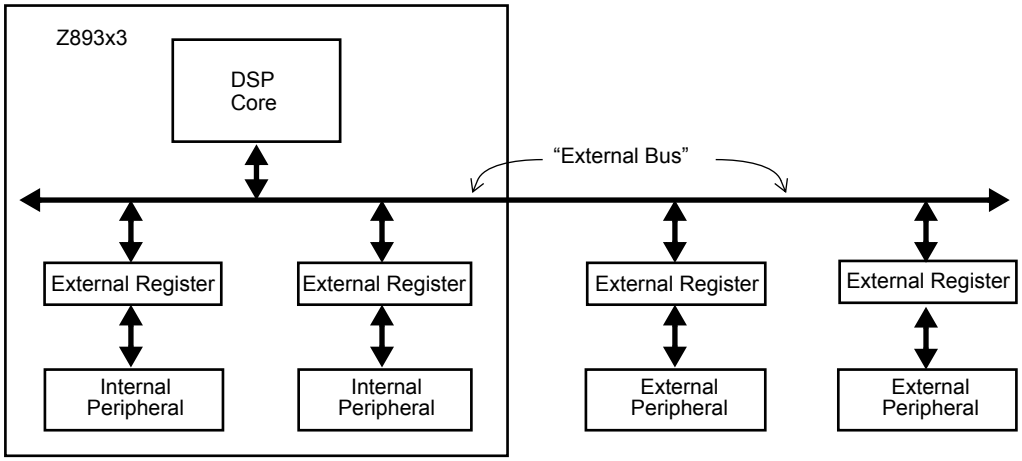


Figure 2. "External" Bus

TMO1/UO1. Counter/Timer Output or User Output 1 (output). Counter/Timer 0 and Counter/Timer 1 can be programmed to provide output on this pin. When User Outputs are enabled, and the Counter/Timer is disabled, this pin provides the complement of Status Register bit 6.

TMO2. Counter/Timer 2 Output (output). This pin is the output of Counter/Timer 2

P0.15–P0.0. Port0 (input/output). This is a 16-bit user I/O port. Bits can be configured as input or output or globally as open-drain output. When enabled, Port0 uses the 16 data lines of the ED bus. The function of these pins can be dynamically changed by writing to the Port0 configuration registers. The High byte can also be configured to Port1 as described in the I/O Port section.

P1.7–P1.0. Port1 (input/output). These pins are Port1 inputs or outputs when not configured for use as special purpose peripheral interface. The following eight pin functions preempt use of these pins when enabled. INT2, CLKOUT, SDI, SDO, SS, SCLK, UI0, UI1.

Note: These pins are not bonded out on the 44-pin packages.

P2.7–P2.0. Port2 (input/output). These pins are Port2 inputs or outputs when not configured as peripheral interfaces. The following seven pin functions preempt use of P2.6–P2.0 when enabled. INT0, INT1, TMO0/UO0, TMO1/UO1, $\overline{\text{WAIT}}$, UI2, TMO2. P2.7 does not include a dual function.

Note: P2.7–P2.5 are not bonded out on the 44-pin packages.

The following port pins are available only on the 80-pin package:

P3.7–P3.4. Port3 (output). These pins are Port3 outputs.

P3.3–P3.0. Port3 (input). These pins are Port3 inputs.

Table 2. 44-Pin PQFP Z89223/273 Pin Description

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	ED3/P0.3	External Data Bus/Port0	Input/Output	23	EA0	Ext Address 0	Output
2	ED4/P0.4	External Data Bus/Port0	Input/Output	24	EA1	Ext Address 1	Output
3	V_{SS}	Ground		25	EA2	Ext Address 2	Output
4	ED5/P0.5	External Data Bus/Port0	Input/Output	26	P2.3/TMO1	Port 2.3/Timer Output 1	Input/Output
5	ED6/P0.6	External Data Bus/Port0	Input/Output	27	$\overline{DS}$	Ext Data Strobe	Output
6	ED7/P0.7	External Data Bus/Port0	Input/Output	28	P2.4/$\overline{WAIT}$	Port 2.4/Wait for ED	Input/Output
7	ED8/P0.8	External Data Bus/Port0	Input/Output	29	CLKI	Clock/Crystal In	Input
8	ED9/P0.9	External Data Bus/Port0	Input/Output	30	CLKO	Clock/Crystal Out	Output
9	V_{SS}	Ground		31	P2.2/TMO0	Port 2.2/Timer Output 0	Input/Output
10	ED10/P0.10	External Data Bus/Port0	Input/Output	32	LPF	PLL Low Pass Filter	Input
11	ED11/P0.11	External Data Bus/Port0	Input/Output	33	$\overline{RESET}$	Reset	Input
12	VAHI	Analog High Ref. Voltage	Input	34	V_{DD}	Power Supply	
13	VALO	Analog Low Ref. Voltage	Input	35	ED0/P0.0	External Data Bus/Port0	Input/Output
14	AGND	Analog Ground		36	ED1/P0.1	External Data Bus/Port0	Input/Output
15	AN0	A/D Input 0	Input	37	ED2/P0.2	External Data Bus/Port0	Input/Output
16	AN1	A/D Input 1	Input	38	V_{SS}	Ground	
17	AN2	A/D Input 2	Input	39	P2.0/INT0	Port 2.0/Interrupt 0	Input/Output
18	AN3	A/D Input 3	Input	40	ED12/P0.12	External Data Bus/Port0	Input/Output
19	P2.1/INT1	Port 2.1/Interrupt 1	Input/Output	41	ED13/P0.13	External Data Bus/Port0	Input/Output
20	AV_{CC}	Analog Power		42	ED14/P0.14	External Data Bus/Port0	Input/Output
21	V_{DD}	Power		43	V_{SS}	Ground	
22	RD/$\overline{WR}$	R/W Exteral Output Bus		44	ED15/P0.15	External Data Bus/Port0	Input/Output

Table 4. 68-Pin PLCC Z89323/373 Pin Description

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	P1.2/SDI	Port 1.2/Serial Input	Input/Output	35	AN0	A/D Input 0	Input
2	P2.0/INT0	Port 2.0/Interrupt 0	Input/Output	36	AN1	A/D Input 1	Input
3	ED12/P0.12	External Data Bus/Port0	Input/Output	37	AN2	A/D Input 2	Input
4	ED13/P0.13	External Data Bus/Port0	Input/Output	38	AN3	A/D Input 3	Input
5	V_{DD}	Power Supply		39	V_{SS}	Ground	
6	ED14/P0.14	External Data Bus/Port0	Input/Output	40	P2.1/INT1	Port 2.1/Interrupt 1	Input/Output
7	V_{SS}	Ground		41	AVCC	Analog Power	
8	ED15/P0.15	External Data Bus/Port0	Input/Output	42	V_{DD}	Power Supply	
9	NC	No Connection		43	RD/$\overline{WR}$	R/W External Bus	Output
10	NC	No Connection		44	$\overline{HALT}$	Halt Execution	Input
11	ED3/P0.3	External Data Bus/Port0	Input/Output	45	EA0	Ext Address 0	Output
12	ED4/P0.4	External Data Bus/Port0	Input/Output	46	EA1	Ext Address 1	Output
13	V_{SS}	Ground		47	EA2	Ext Address 2	Output
14	V_{DD}	Power Supply		48	NC	No Connection	
15	ED5/P0.5	External Data Bus/Port0	Input/Output	49	V_{DD}	Power Supply	
16	P1.3/SDO	Port 1.3/Serial Output	Input/Output	50	P2.3/TMO1	Port2.3/Timer Output 1	Input/Output
17	ED6/P0.6	External Data Bus/Port0	Input/Output	51	$\overline{DS}$	Ext Data Strobe	Output
18	P1.4/SS	Port 1.4/Slave Select	Input/Output	52	P2.4/$\overline{WAIT}$	Port 2.4/Wait for ED	Input/Output
19	ED7/P0.7	External Data Bus/Port0	Input/Output	53	CLKI	Clock/Crystal In	Input
20	P1.5/SCLK	Port 1.5/Serial Clock	Input/Output	54	CLKO	Clock/Crystal Out	Output
21	P2.7	Port 2.7	Input/Output	55	P2.6/TMO2	Port 2.6/Timer Output 2	Input/Output
22	ED8/P0.8	External Data Bus/Port0	Input/Output	56	P2.2/TMO0	Port 2.2/Timer Output 0	Input/Output
23	ED9/P0.9	External Data Bus/Port0	Input/Output	57	P2.5/UI2	Port 2.5/User Input 2	Input/Output
24	V_{SS}	Ground		58	LPF	PLL Low Pass Filter	Input
25	ED10/P0.10	External Data Bus/Port0	Input/Output	59	$\overline{RESET}$	Reset	Input
26	V_{SS}	Ground		60	V_{SS}	Ground	
27	ED11/P0.11	External Data Bus/Port0	Input/Output	61	V_{DD}	Power Supply	
28	V_{DD}	Power Supply		62	V_{SS}	Ground	
29	VAHI	Analog High Ref. Voltage	Input	63	ED0/P0.0	External Data Bus/Port0	Input/Output
30	V_{SS}	Ground		64	ED1/P0.1	External Data Bus/Port0	Input/Output
31	P1.6/UI0	Port 1.6/User Input 0	Input/Output	65	ED2/P0.2	External Data Bus/Port0	Input/Output
32	VALO	Analog Low Ref. Voltage	Input	66	P1.0/INT2	Port 1.0/Interrupt 2	Input/Output
33	P1.7/UI1	Port 1.7/User Input 1	Input/Output	67	V_{SS}	Ground	
34	AGND	Analog Ground		68	P1.1/CLKOUT	Port 1.1/Clock Output	Input/Output

DC ELECTRICAL CHARACTERISTICS (Continued)

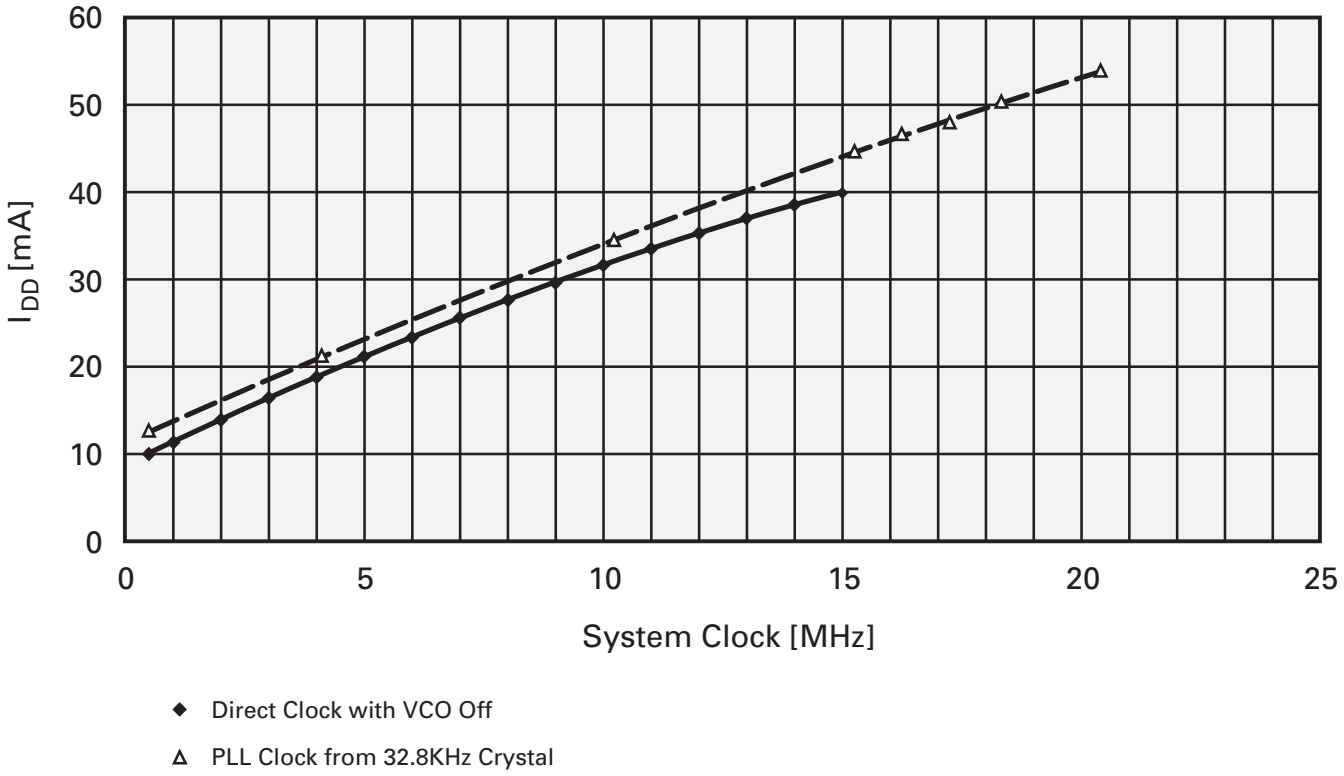
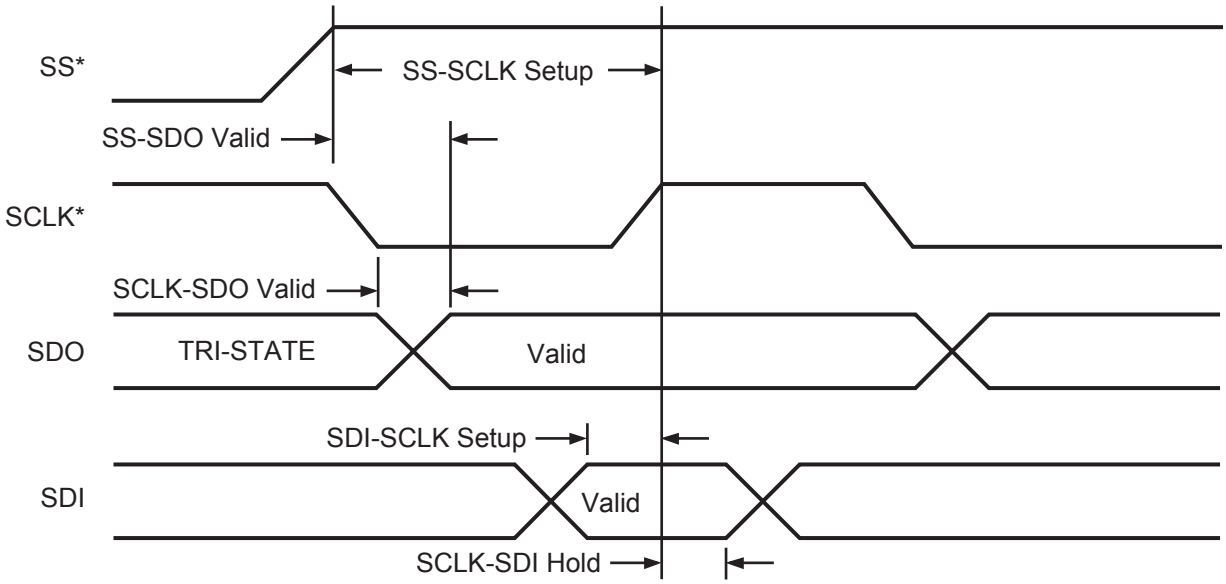


Figure 9. Z89373 Typical OTP Current Consumption



*Notes: The polarity of SCLK and SS are programmable by the user. SS is used in Slave Mode only. This figure illustrates data transmission on the falling edge of SCLK, data reception on the rising edge of SCLK, with SS active Low (default).

Figure 15. SPI Timing (Master and Slave Modes)

MEMORY MAP

Program Memory. Programs of up to 8K words can be masked into internal ROM (Z89323) or programmed into OTP (Z89373). Four locations are dedicated to the vector addresses for the three interrupt service routines (1FFDH–1FFFH) and for the starting address following a $\overline{\text{RESET}}$ (1FFCH). Internal ROM is mapped from 0000H to 1FFFH, and the highest location for program instructions is 1FFBH.

Internal Data RAM. All Z893x3 family members feature internal 512 x 16-bit data RAM organized as two banks of 256 x 16-bit words each (RAM0 and RAM1). The three addressing modes available to access the data RAM are direct addressing, short form direct, and register indirect.

The contents of both data RAM banks can be read simultaneously and loaded into the X and Y inputs of the multiplier during a multiply instruction.

The addresses for each data RAM bank are:

0–255 (0000H–00FFH) for RAM0

256–511 (0100H–01FFH) for RAM1

Data RAM Pointers. In register indirect, each data RAM bank is addressed by one of three data RAM address pointers:

Example: Pn:b, where
n = pointer number = 0, 1, or 2
b = bank = 0 or 1,

thus,

P0:0, P1:0, P2:0 for RAM0
P0:1, P1:1, P2:1 for RAM1

In auto-increment, loop-increment, and loop-decrement indirect addressing, the pointer is automatically modified.

The data RAM pointers, which may be read or written directly, are 8-bit registers connected to the lower byte of the internal 16-bit DDATA Bus.

Program Memory Pointers. The first 16 locations of each data RAM bank can be used as pointers to locations in Program Memory. These pointers provide an efficient way to address coefficients. The programmer selects a pointer location using two bits in the status register and two bits in the operand. At any one time, there are eight usable pointers, four per bank, and the four pointers are in consecutive locations.

Example: Dn:b, where
n = pointer number = 0, 1, 2, or 3
b = bank = 0 or 1,

thus,

D0:0, D1:0, D2:0, D3:0 for RAM0
D0:1, D1:1, D2:1, D3:1 for RAM1

If S3/S4 = 01 in the status register, then D0:0/D1:0/D2:0/D3:0 refer to register locations 4/5/6/7 in data RAM Bank 0.

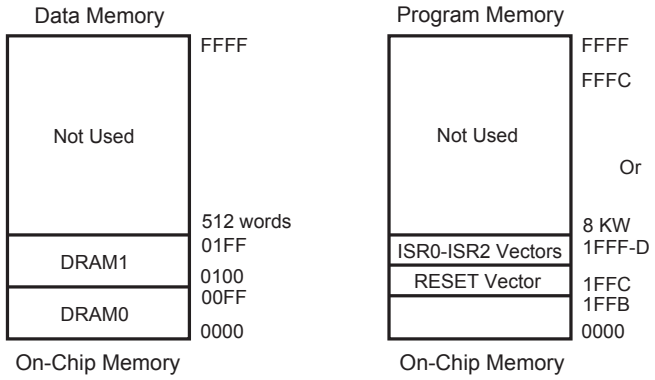


Figure 18. Memory Map

I/O PORTS

I/O pin allocation of ports for the different package types is designed to provide configuration flexibility. Each port line of Ports 0, 1, and 2 can be independently selected as an input or an output. Each port's output lines can be globally selected as push-pull or as open-drain outputs

Table 15. I/O Port Bit Allocations

Device Pins	44-Pin PLCC, 44-Pin PQFP	64-Pin TQFP, 68-Pin PLCC	80-Pin PQFP
P0 MSB	ED15–ED8, or P0.15–P0.8, or P1.7–P1.0	ED15–ED8, or P0.15–P0.8	ED15–ED8, or P0.15–P0.8
P0 LSB	ED7–ED0, or P0.7–P0.0	ED7–ED0, or P0.7–P0.0	ED7–ED0, or P0.7–P0.0
P1		P1.7–P1.0	P1.7–P1.0
P2	P2.4–P2.0	P2.7–P2.0	P2.7–P2.0
P3			P3.7–P3.0

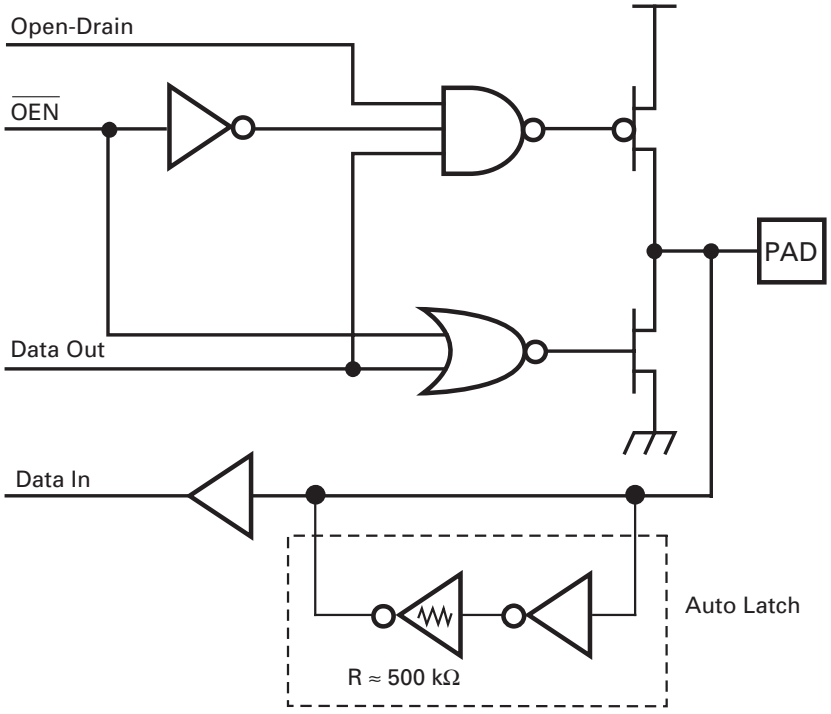


Figure 24. Port 0, 1 and 2 Configuration

I/O PORTS (Continued)

Port0—16-Bit Programmable I/O

Bank15/EXT0 is the Port0 direction control register. Bank15/EXT1 includes specific bits to enable and configure Port0. The Port0 data register is Ext4 in Banks 0, 1, or 5.

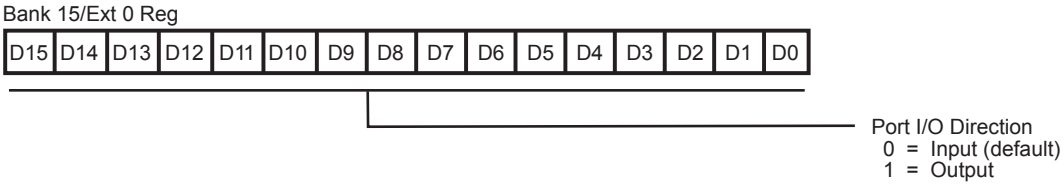


Figure 25. Port 0 Control Register

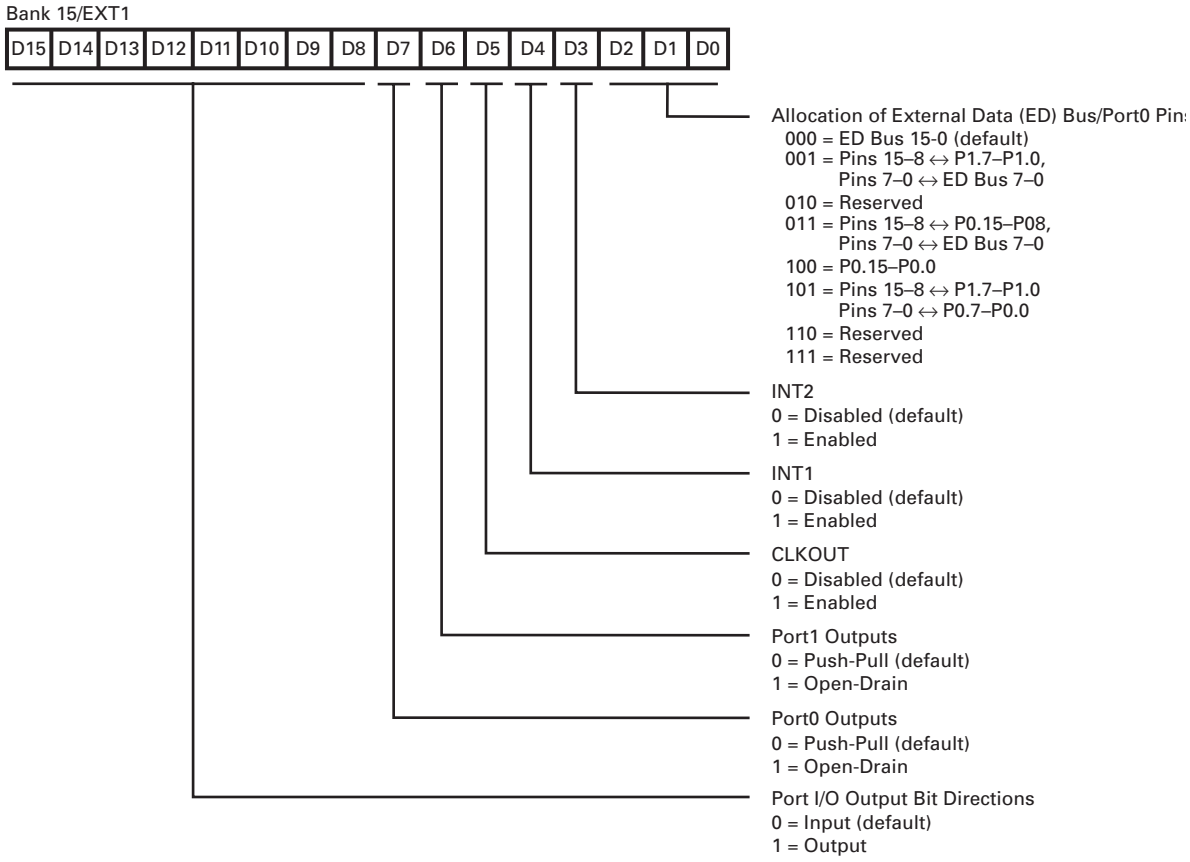


Figure 26. Bank15/EXT1 Register

Port3—8-Bit Programmable I/O

Port3 is an additional I/O port available only in the 80-pin package. P3.3–P3.0 are inputs and P3.7–P3.4 are outputs. Bit 8 of Bank15/EXT2 enables and disables Port3. The LSB of Bank2/EXT5 is the Port3 Data Register.

GENERAL-PURPOSE COUNTER/TIMER (C/T2) (Continued)

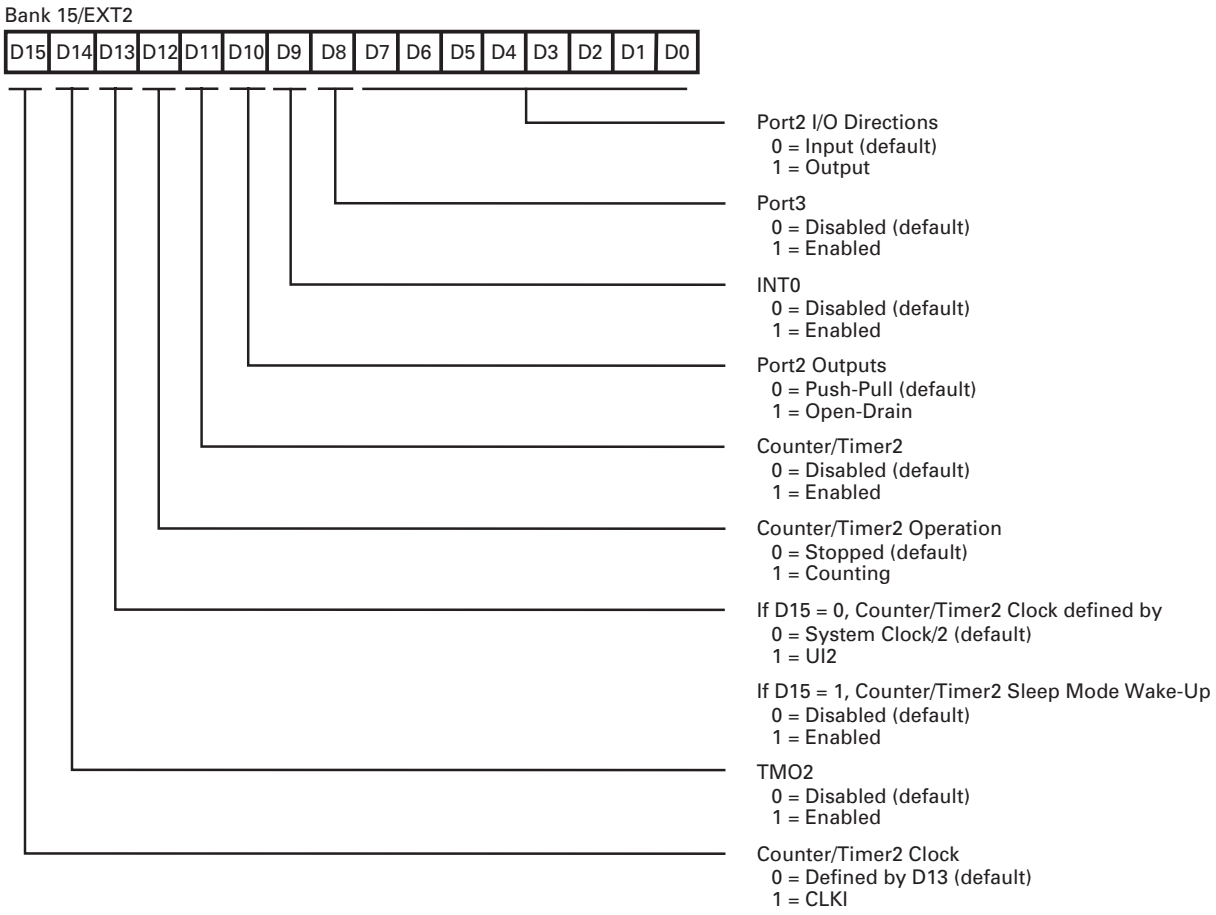


Figure 38. Counter/Timer2 Control Register

SERIAL PERIPHERAL INTERFACE (Continued)

Slave Mode Operation

SS must be asserted to enable a data transfer. Incoming data on the SDI pin is shifted into the SPI Shift Register one data bit per SCLK cycle. When a byte of data is received, the SPI Shift Register contents are automatically copied into RxBUF. The Receive Byte Available flag is set, and if enabled, an SPI interrupt is generated. The next byte of data may be received at this time. The current byte in RxBUF must be read before the next byte's reception is complete, or the Receive Byte Overrun flag will set, and the data in RxBUF will be overwritten. The Receive Byte Available flag is reset when RxBUF is read.

Unless the SPI output, SDO, is disabled, for every bit that is transferred into the slave through the SDI pin, a bit is transferred out through the SDO pin on the opposite clock edge. During slave operation, SCLK is an input.

Note: Slave Mode is not available on the 44-pin package.

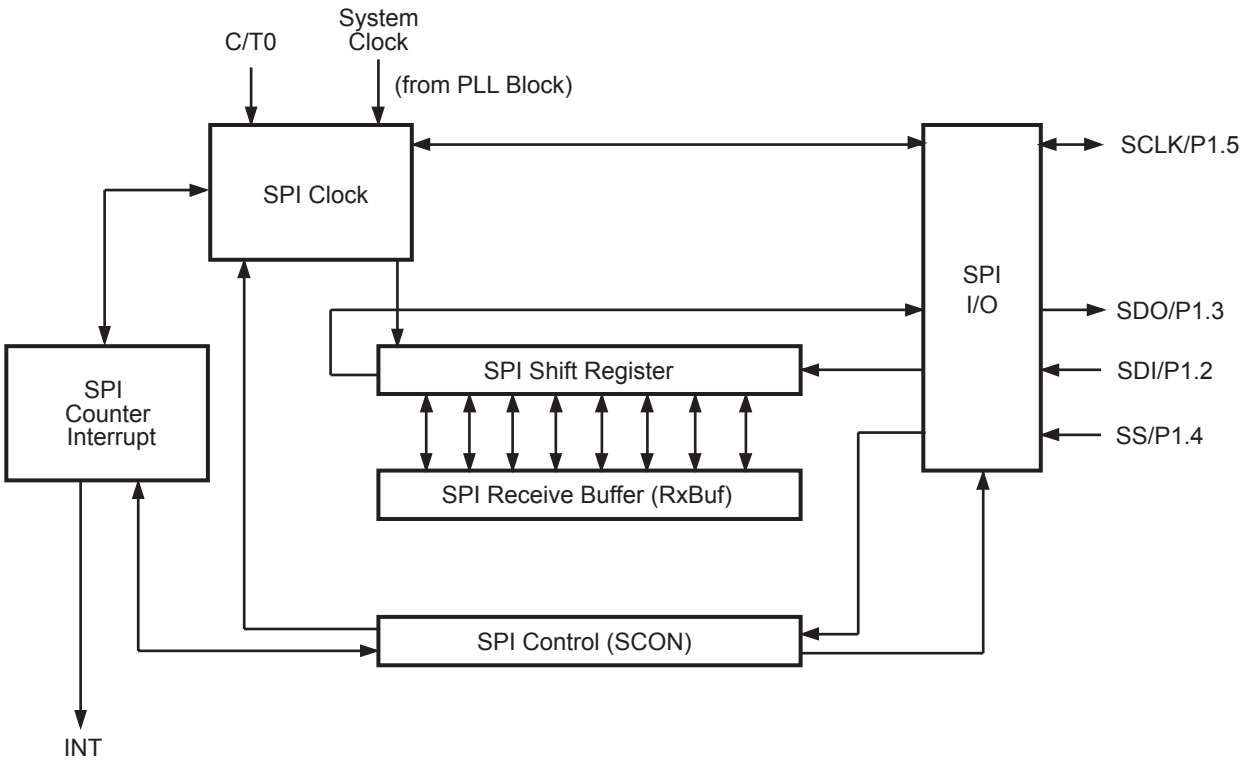


Figure 41. SPI Block Diagram

SYSTEM CLOCK GENERATOR

The System Clock can be generated from an external clock signal, or from the internal crystal oscillator. For the latter case, a 32-kHz crystal is used in conjunction with the internal crystal oscillator. The system clock generator includes a Phase-Locked Loop (PLL) circuit to derive a high-frequency System Clock from the low-frequency crystal oscillator. The benefits of using a low-frequency crystal are lower system cost, lower power consumption and lower EMI.

The Z893x3 supports several low-power clock modes to optimize power consumption. Total power consumption depends on System Clock frequency, and which oscillators and peripherals are enabled.

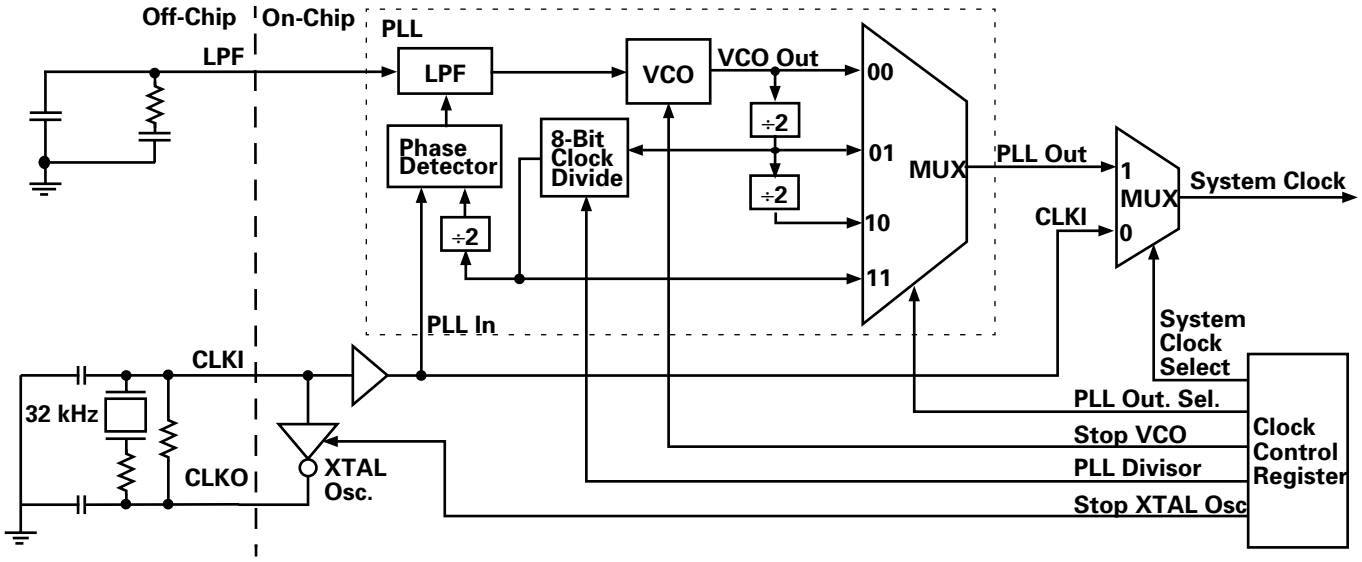


Figure 42. System Clock Generator

Modes of Operation

The various modes of clock operation are selected by writing to the appropriate bits and fields of the Clock Control Register, Bank15/EXT5. The mode of operation can be switched dynamically during program execution.

Power-up and Reset (Default)

At power-up, and following a reset or Sleep Mode Recovery, System Clock Select = 0, therefore system clock = CLKI. The XTAL Oscillator is running, so CLKI may be provided by a crystal, as depicted, or by an external clock (not shown). The VCO is running to minimize the time required to switch the system clock to PLL Out.

External Clock Direct

In this mode, an external clock on CLKI provides the System Clock. CLKO is not connected. System Clock Select = 0. The PLL is not used. The XTAL oscillator and VCO are both stopped to reduce power consumption.

Crystal Oscillator DIrect

In this mode of operation, the XTAL Oscillator is running, and an external crystal provides a 32-kHz (typical) clock at CLKI. System Clock Select = 0, so the System Clock is the frequency at CLKI (32 kHz). This mode requires less power than running at a high-frequency clock rate. The VCO may be stopped to conserve even more power, or left running for rapid switching (wake up) to a high-frequency PLL generated clock. Whenever the PLL circuit is enabled, Stop VCO = 0, and a software delay of 10 ms must be observed before switching System Clock from CLKI to PLL Out. As a result, the PLL has time to stabilize.

PLL Clock

An external 32-kHz crystal, together with the on-chip XTAL oscillator, provides the PLL input. The VCO generates the System Clock. A low-pass filter must be connected to LPF as depicted. The XTAL oscillator and VCO are both running, and System Clock = PLL Out (System Clock Select = 1). The frequency generated by the PLL is deter-

SYSTEM CLOCK GENERATOR (Continued)

mined by the PLL Divisor value in the MSB of the Clock Control Register, Bank15/EXT5:

VCO Frequency = 4 x PLL Divisor x PLL In Frequency.

The PLL Divisor value should be between 1 and156 to obtain a VCO Frequency between 128 kHz and 20 MHz from a 32-kHz input.

There are four options for PLL Out: VCO Out, VCO Out divided by 2, VCO Out divided by four, or twice the crystal frequency. This selection is determined by the PLL Out Select bits in the Clock Control Register.

Note: The PLL is designed and tested to operate with an input frequency of approximately 32 kHz. It is possible to drive the input with a crystal or user-generated clock at some other frequency, but the results are not guaranteed.

Sleep Modes

The Z893x3 supports various Clock Modes to minimize device power consumption. The lowest power mode is Deep Sleep in which the System Clock is stopped, and the VCO and XTAL Oscillator are both turned off.

Table 23. Standard Clock Mode Summary

Mode	CLKI Src	Stop XTAL Osc.	Stop VCO	Sys Clk Sel
Power-up/Reset (default)	XTAL, User	0	0	0
PLL Clock	XTAL	0	0	1
Crystal Oscillator Direct	XTAL	0	1	0
External Clock Direct	User	1	1	0
Deep Sleep (lowest power)	XTAL, User	1	1	1

Wake-Up From Sleep Modes

The Wake-up Trigger Source is specified by bits 5 and 6 of the Clock Control Register. The polarity of the Wake-up signal is defined by bit 7. Wake-up occurs when the wake-up signal is toggled to the specified wake-up polarity. Wake-up resumes operation starting from the reset vector address in the same way the chip responds to an external $\overline{\text{RESET}}$.

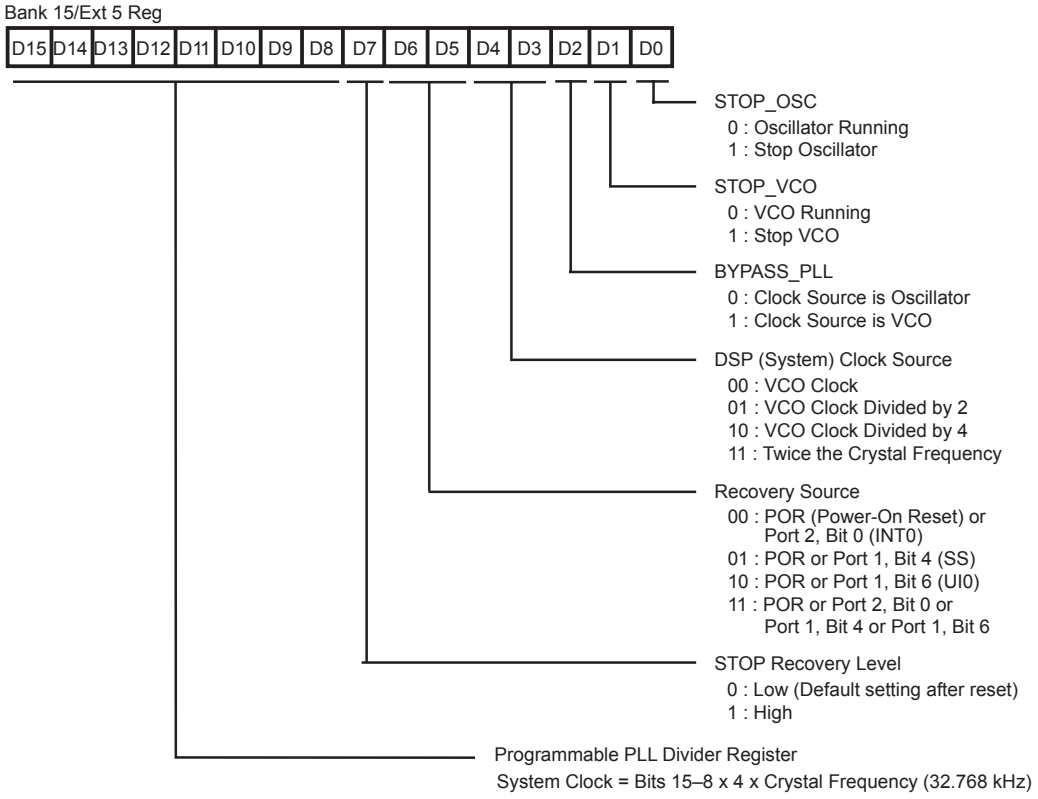


Figure 43. System Clock Control Register

INSTRUCTION SET

The addressing modes are:

<pregs>, <hwregs>. These modes are used for loads to and from registers within the chip, such as loading to the accumulator, or loading from a pointer register. The names of the registers are specified in the operand field (destination first, then source).

<dregs>. This mode is used for access to the lower 16 addresses in each bank of RAM. The 4-bit address comes from 2 bits of the status register and 2 bits of the operand field of the data pointer. Data registers can be used to access data in RAM, but typically are used as pointers to access data from the program memory.

<accind>. Similar to the previous mode, the address for the program memory read is stored in the Accumulator. Hence, @A in the second operand field loads the number in memory specified by the address in A.

<direct>. The direct mode allows read or write to data RAM from the Accumulator by specifying the absolute address of the RAM in the operand of the instruction. A number between 0 and 255 indicates a location in RAM bank 0, and a number between 256 and 511 indicates a location in RAM bank 1.

<limm>. This address mode indicates a long immediate operand. A 16-bit word can be loaded directly from the operand into the specified register or memory location.

<simm>. This address mode indicates a short immediate operand. It is used to load 8-bit data into the specified RAM pointer.

<regind>. This mode is used for indirect access to the data RAM. The address of the RAM location is stored in the pointer. The "@" symbol indicates "indirect" and precedes the pointer. For example, @P1:1 refers to the location in RAM bank 1 specified by the value in the pointer.

<memind>. This mode is used for indirect access to the program memory. The address of the memory is located in a RAM location, which is specified by the value in a pointer. Therefore, @@P1:1 instructs the processor to read from a location in memory, which is specified by a value in RAM, and the location of the RAM is in turn specified by the value in the pointer.

Note: the data pointer can also be used for a memory access in this manner, but only one "@" precedes the pointer. In both cases, each time the addressing mode is used, the memory address stored in RAM is incremented by one to allow easy transfer of sequential data from program memory.

Table 24. Instruction Set Addressing Modes

Symbolic Name	Syntax	Description
<pregs>	Pn:b	Pointer Registers
<dregs> (points to RAM)	Dn:b	Data Registers
<hwregs>	X, Y, PC, SR, P, EDn, A, BUS	Hardware Registers
<accind> (points to Program Memory)	@A	Accumulator Memory Indirect
<direct>	<expression>	Direct Address Expression
<limm>	#<const exp>	Long (16-bit) Immediate Value
<simm>	#<const exp>	Short (8-bit) Immediate Value
<regind> (points to RAM)	@Pn:b	Pointer Register Indirect
	@Pn:b+	Pointer Register Indirect with Increment
	@Pn:b–LOOP	Pointer Register Indirect with Loop Decrement
	@Pn:b+LOOP	Pointer register Indirect with Loop Increment
<memind> (points to Program Memory)	@@Pn:b	Pointer Register Memory Indirect
	@Dn:b	Data Register Memory Indirect
	@@Pn:b–LOOP	Pointer Register Memory Indirect with Loop Decrement
	@@Pn:b+LOOP	Pointer Register Memory Indirect with Loop Increment
	@@Pn:b+	Pointer Register Memory Indirect with Increment

CONDITION CODES

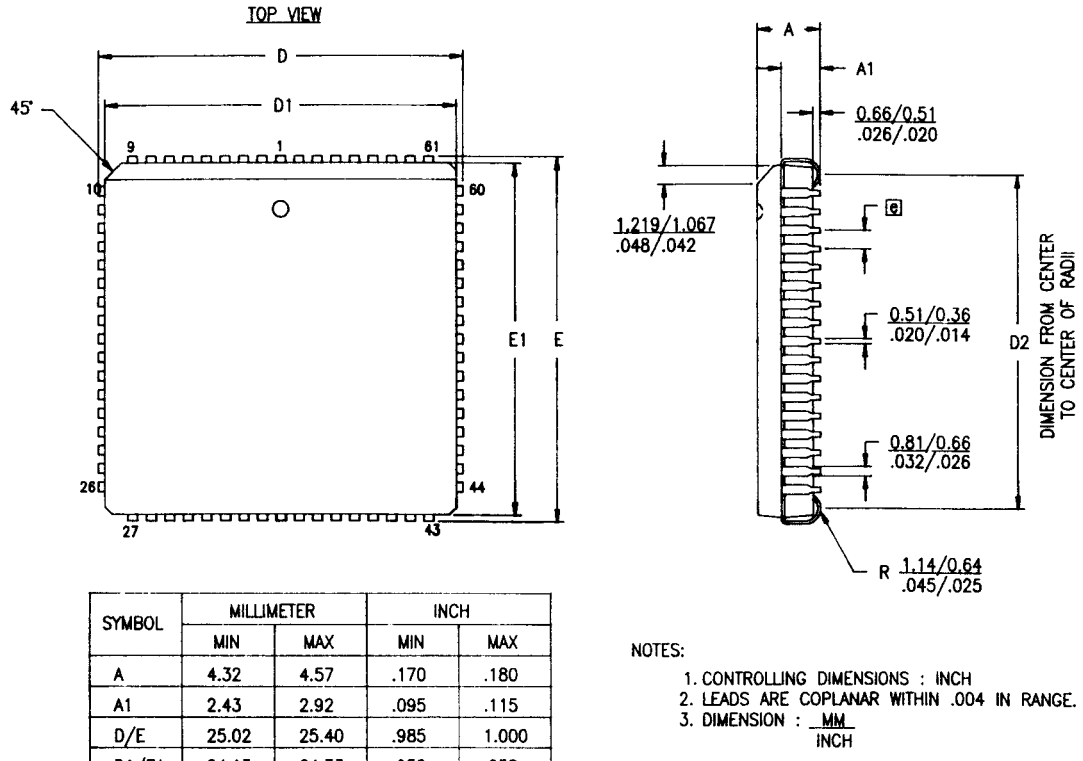
The following Instruction Description defines the condition codes supported by the DSP assembler. If the instruction description refers to the <cc> (condition code) symbol in one of its addressing modes, the instruction only executes if the condition is true.

Code	Description
C	Carry
EQ	Equal (same as Z)
F	False
IE	Interrupts Enabled
MI	Minus
NC	No Carry
NE	Not Equal (same as NZ)
NIE	Not Interrupts Enabled
NOV	Not Overflow
NU0	Not User Zero
NU1	Not User One
NZ	Not zero
OV	Overflow
PL	Plus (Positive)
U0	User Zero
U1	User One
UGE	Unsigned Greater Than or Equal (Same as NC)
ULT	Unsigned Less Than (Same as C)
Z	Zero

INSTRUCTION DESCRIPTIONS (Continued)

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
XOR	Bitwise exclusive OR	XOR <dest>,<src>	A,<pregs>	1	1	XOR A,P2:0
			A,<dregs>	1	1	XOR A,D0:1
			A,<limm>	2	2	XOR A,#13933
			A,<memind>	1	3	XOR A,@@P2:1+
			A,<direct>	1	1	XOR A,%2F
			A,<regind>	1	1	XOR A,@P2:0
			A,<hwregs>	1	1	XOR A,BUS
			A,<simm>	1	1	XOR A, #%12

Bank Switch Operand. The third (optional) operand of the MLD, MPYA and MPYS instructions represents whether the bank switch is set to ON or OFF. To illustrate, the keywords ON and OFF are used to state the direction of the switch. These keywords are referenced in the instruction descriptions through the <bank switch> symbol. The most notable capability is that a source operand can be multiplied by itself (squared).



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.32	4.57	.170	.180
A1	2.43	2.92	.095	.115
D/E	25.02	25.40	.985	1.000
D1/E1	24.13	24.33	.950	.958
D2	22.86	23.62	.900	.930
e	1.27 TYP		.050 TYP	

NOTES:

1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN RANGE.
3. DIMENSION : MM / INCH

Figure 47. 68-Pin PLCC Package Diagram

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