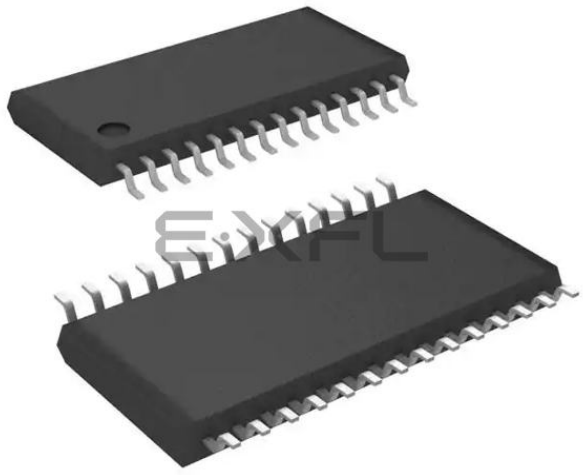

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8052
Core Size	8-Bit
Speed	16.78MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PSM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 6x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	28-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc814aru

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REVISION HISTORY

12/03 – Data Sheet Changed from REV. 0 to REV. A

Added detailed description of product .... Universal

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[1]Temperature range –40ºC to +125ºC.
[2]ADC linearity is guaranteed when operating in nonpipelined mode, i.e., ADC conversion followed sequentially by a read of the ADC result. ADC linearity is also guaranteed during normal MicroConverter core operation.
[3]ADC LSB size = V_{REF} /2^{12}, i.e., for internal V_{REF} = 2.5 V, 1 LSB = 610 µV, and for external V_{REF} = 1 V, 1 LSB = 244 µV.
[4]Offset and gain error and offset and gain error match are measured after factory calibration.
[5]Based on external ADC system components the user may need to execute a system calibration to remove additional external channel errors and achieve these specifications.
[6]Measured with coherent sampling system using external 16.77 MHz clock via P3.5 (Pin 22).
[7]SNR calculation includes distortion and noise components.
[8]Channel-to-channel crosstalk is measured on adjacent channels.
[9]The temperature monitor gives a measure of the die temperature directly; air temperature can be inferred from this result.
[10]DAC linearity is calculated using a reduced code range of 48 to 4095, 0 V to V_{REF} range; a reduced code range of 48 to 3950, 0 V to V_{DD} range. DAC output load = 10 kΩ and 100 pF.
[11]DAC differential nonlinearity specified on 0 V to V_{REF} and 0 to V_{DD} ranges.
[12]Measured with V_{REF} and C_{REF} pins decoupled with 0.1 µF capacitors to ground. Power-up time for the internal reference is determined by the value of the decoupling capacitor chosen for both the V_{REF} and C_{REF} pins.
[13]When using an external reference device, the internal band gap reference input can be bypassed by setting the ADCCON1.6 bit. In this mode, the V_{REF} and C_{REF} pins need to be shorted together for correct operation.
[14]These numbers are not production tested but are guaranteed by design and/or characterization data on production release.
[15]Pins configured in I^2C compatible mode or SPI mode; pins configured as digital inputs during this test.
[16]These typical specifications assume no loading on the XTAL2 pin. Any additional loading on the XTAL2 pin increases the power-on times.
[17]Flash/EE memory reliability characteristics apply to both the Flash/EE program memory and the Flash/EE data memory.
[18]Endurance is qualified to 100 kcycles as per JEDEC Std. 22, Method A117 and measured at –40ºC, +25°C, and +125°C; typical endurance at +25°C is 700 kcycles.
[19]Retention lifetime equivalent at junction temperature (T_J) = 55°C as per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature as shown in Figure 33 in the Flash/EE memory description section.
[20]Power supply current consumption is measured in normal, idle, and power-down modes under the following conditions:
Normal Mode: Reset and all digital I/O pins = open circuit, core Clk changed via CD bits in PLLCON, core executing internal software loop.
Idle Mode: Reset and all digital I/O pins = open circuit, core Clk changed via CD bits in PLLCON, PCON.0 = 1, core execution suspended in idle mode.
Power-Down Mode: Reset and all P1.2–P1.7 pins = 0.4 V; all other digital I/O pins are open circuit, Core Clk changed via CD bits in PLLCON, PCON.1 = 1, Core execution suspended in power-down mode, OSC turned on or off via OSC_PD bit (PLLCON.7) in PLLCON SFR.
[21]DV_{DD} power supply current increases typically by 3 mA (3 V operation) and 10 mA (5 V operation) during a Flash/EE memory program or erase cycle.

ABSOLUTE MAXIMUM RATINGS

Table 2. Temperature = 25°C, unless otherwise noted

Parameter	Rating
AV_{DD} to AGND	–0.3 V to +7 V
DV_{DD} to AGND	–0.3 V to +7 V
AV_{DD} to DV_{DD}	–0.3 V to +0.3 V
AGND to DGND[1]	–0.3 V to +0.3 V
Analog Input Voltage to AGND[2]	–0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND	–0.3 V to AV_{DD} + 0.3 V
Analog Input Current (Indefinite)	30 mA
Reference Input Current (Indefinite)	30 mA
Digital Input Voltage to DGND	–0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND	–0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	97.9°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] AGND and DGND are shorted internally on the ADuC814.
[2] Applies to Pins P1.2 to P1.7 operating in analog or digital input mode.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

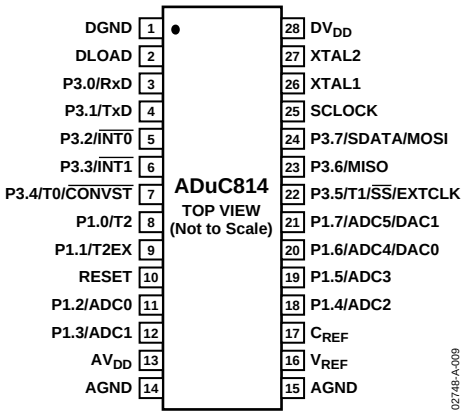

Figure 2. Pin Configuration

Table 3. Pin Descriptions

Pin No.	Mnemonic	Type	Function
1	DGND	S	Digital Ground. Ground reference point for the digital circuitry.
2	DLOAD	I	Debug/Serial Download Mode. Enables when pulled high through a resistor on power-on or RESET. In this mode, DLOAD may also be used as an external emulation I/O pin, therefore the voltage level at this pin must not be changed during this mode of operation because it may cause an emulation interrupt that halts code execution. User code is executed when this pin is pulled low on power-on or RESET.
3–7	P3.0 – P3.4	I/O	Bidirectional Port Pins with Internal Pull-Up Resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, with Port 3 pins being pulled low externally, they source current because of the internal pull-up resistors. When driving a 0-to-1 output transition, a strong pull-up is active during S1 of the instruction cycle. Port 3 pins also have various secondary functions which are described next.
3	P3.0/RxD	I/O	Receiver Data Input (asynchronous) or Data Input/Output (synchronous) in Serial (UART) Mode.
4	P3.1/TxD	I/O	Transmitter Data Output (asynchronous) or Clock Output (synchronous) in Serial (UART) Mode.
5	P3.2/$\overline{\text{INT0}}$	I/O	Interrupt 0, programmable edge or level-triggered interrupt input, which can be programmed to one of two priority levels. This pin can also be used as agate control input to Timer 0.
6	P3.3/$\overline{\text{INT1}}$	I/O	Interrupt 1, programmable edge or level-triggered interrupt input, which can be programmed to one of two priority levels. This pin can also be used as agate control input to Timer 1.
7	P3.4/T0/ $\overline{\text{CONVST}}$	I/O	Timer/Counter 0 Input and External Trigger Input for ADC Conversion Start.
8–9	P1.0–P1.1	I/O	Bidirectional Port Pins with Internal Pull-Up Resistors. Port 1 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs ,with Port 1 pins being pulled low externally, they source current because of the internal pull-up resistors When driving a 0-to-1 output transition a strong pull-up is active during S1 of the instruction cycle. Port 1 pins also have various secondary functions which are described as follows.
8	P1.0/T2	I/O	Timer 2 Digital Input. Input to Timer/Counter 2. When enabled, Counter 2 is incremented in response to a 1 to 0 transition of the T2 input.
9	P1.1/T2EX	I/O	Digital Input. Capture/Reload trigger for Counter 2.
10	RESET	I	Reset Input. A high level on this pin while the oscillator is running resets the device. There is an internal weak pull-down and a Schmitt-trigger input stage on this pin.
11–12	P1.2–P1.3	I	Port 1.2 to P1.3. These pins have no digital output drivers, i.e., they can only function as digital inputs, for which 0 must be written to the port bit. These port pins also have the following analog functionality:
11	P1.2/ADC0	I	ADC Input Channel 0. Selected via ADCCON2 SFR.
12	P1.3/ADC1	I	ADC Input Channel 1. Selected via ADCCON2 SFR.
13	AV_{DD}	S	Analog Positive Supply Voltage, 3 V or 5 V.
14–15	AGND	G	Analog Ground. Ground reference point for the analog circuitry.
16	V_{REF}	I/O	Reference Input/Output. This pin is connected to the internal reference through a switch and is the reference source for the analog to digital converter. The nominal internal reference voltage is 2.5 V and this appears at the pin. This pin can be used to connect an external reference to the analog to digital converter by setting ADCCON1.6 to 1. Connect 0.1 µF between this pin and AGND.

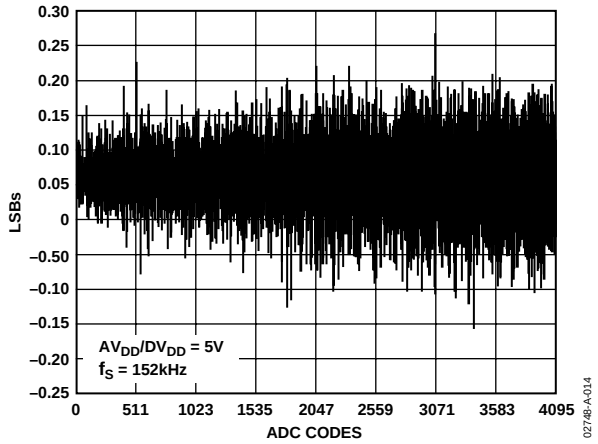

Figure 7. Typical DNL Error, V_{DD} = 5 V

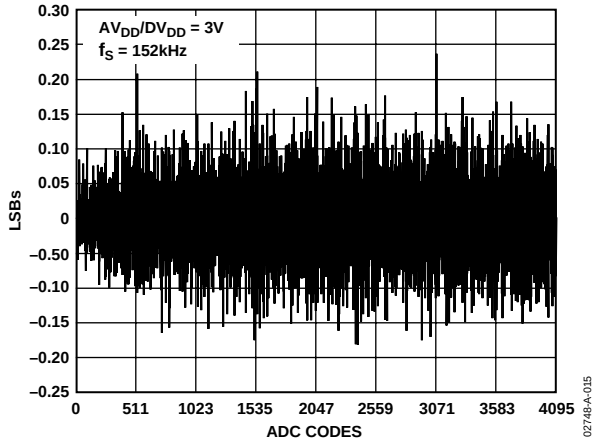

Figure 8. Typical DNL Error, V_{DD} = 3 V

Figure 9 and Figure 10 show the variation in worst-case positive (WCP) DNL and worst-case negative (WCN) DNL versus external reference input voltage.

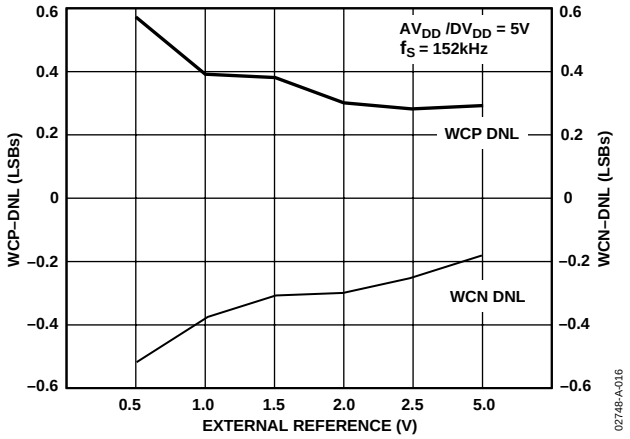

Figure 9. Typical Worst-Case DNL Error vs. V_{REF}, V_{DD} = 5 V

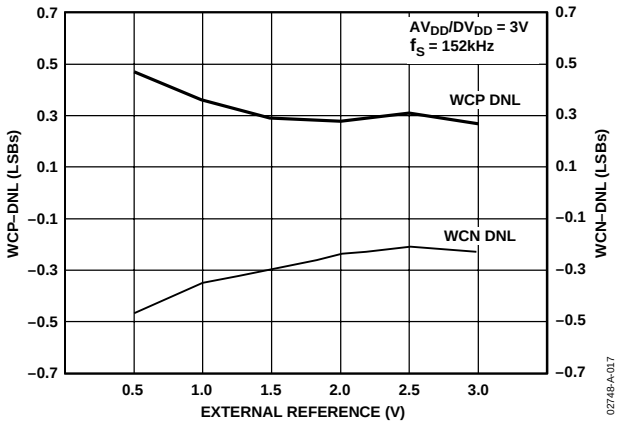

Figure 10. Typical Worst-Case DNL Error vs. V_{REF}, V_{DD} = 3 V

Figure 11 shows a histogram plot of 10,000 ADC conversion results on a dc input with V_{DD} = 5 V. The plot illustrates an excellent code distribution pointing to the low noise performance of the on-chip precision ADC.

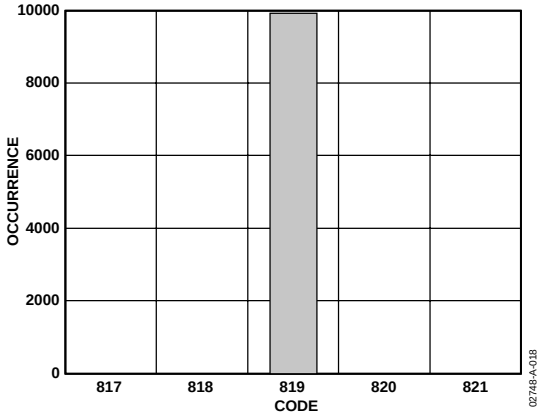

Figure 11. Code Histogram plot, V_{DD} = 5 V

Figure 12 shows a histogram plot of 10,000 ADC conversion results on a dc input for V_{DD} = 3 V. The plot again illustrates a very tight code distribution of 1 LSB with the majority of codes appearing in one output bin.

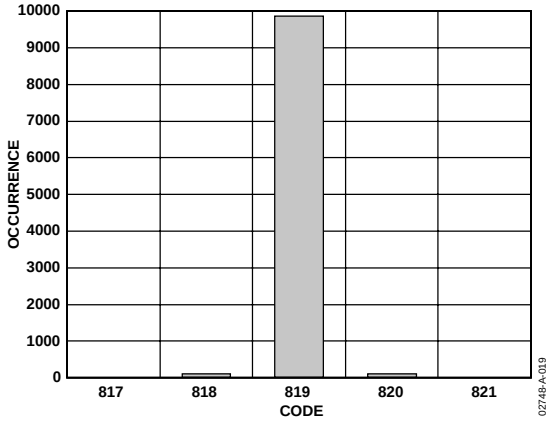

Figure 12. Code Histogram Plot, V_{DD} = 3 V

Figure 13 and Figure 14 show typical FFT plots for the ADuC814. These plots were generated using an external clock input via P3.5 to achieve coherent sampling. The ADC is using its internal reference (2.5 V) sampling a full-scale, 10 kHz sine wave test tone input at a sampling rate of 149.79 kHz. The resultant FFTs shown at 5 V and 3 V supplies illustrate an excellent 100 dB noise floor, a 71 dB signal-to-noise ratio (SNR), and a THD greater than −80 dB.

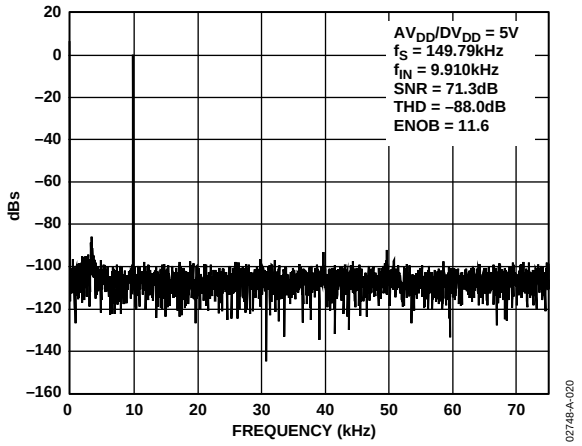

Figure 13. ADuC814 Dynamic Performance at V_{DD} = 5 V

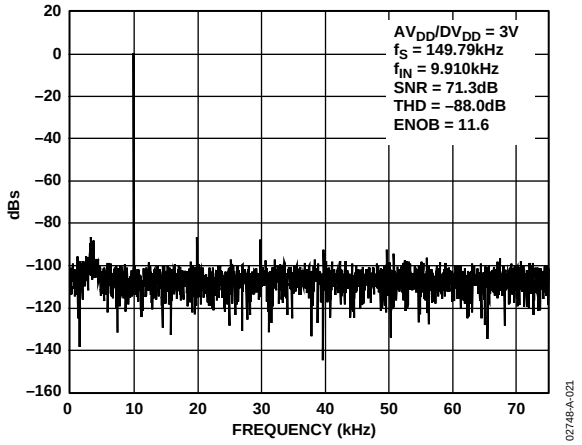

Figure 14. ADuC814 Dynamic Performance at V_{DD} = 3 V

Figure 15 and Figure 16 show typical dynamic performance versus external reference voltages. Again excellent ac performance can be observed in both plots with some roll-off being observed as V_{REF} falls below 1 V.

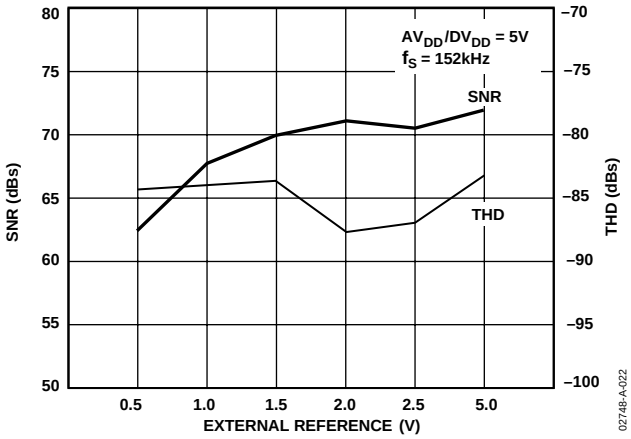

Figure 15. Typical Dynamic Performance vs. V_{REF}, V_{DD} = 5 V

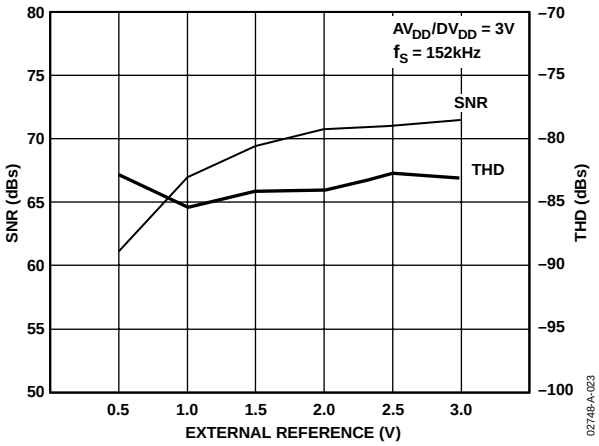

Figure 16. Typical Dynamic Performance vs. V_{REF}, V_{DD} = 3 V

ADC CIRCUIT INFORMATION

GENERAL OVERVIEW

The ADC block incorporates a 4.05 msec, 6-channel, 12-bit resolution, single-supply ADC. This block provides the user with a multichannel multiplexer, track-and-hold amplifier, on-chip reference, offset calibration features and ADC. All components in this block are easily configured via a 3-register SFR interface.

The ADC consists of a conventional successive-approximation converter based around a capacitor DAC. The converter accepts an analog input range of 0 V to V_{REF}. A precision, factory calibrated 2.5 V reference is provided on-chip. An external reference may also be used via the external V_{REF} pin. This external reference can be in the range 1.0 V to AV_{DD}.

Single or continuous conversion modes can be initiated in software. In hardware, a convert signal can be applied to an external pin (CONVST), or alternatively Timer 2 can be configured to generate a repetitive trigger for ADC conversions.

The ADuC814 has a high speed ADC to SPI interface data capture logic implemented on-chip. Once configured, this logic transfers the ADC data to the SPI interface without the need for CPU intervention.

The ADC has six external input channels. Two of the ADC channels are multiplexed with the DAC outputs, ADC4 with DAC0, and ADC5 with DAC1. When the DAC outputs are in use, any ADC conversion on these channels represents the DAC output voltage. Due care must be taken to ensure that no external signal is trying to drive these ADC/DAC channels while the DAC outputs are enabled.

In addition to the six external channels of the ADC, five internal signals are also routed through the front end multiplexer. These signals include a temperature monitor, DAC0, DAC1, V_{REF}, and AGND. The temperature monitor is a voltage output from an on-chip band gap reference, which is proportional to absolute temperature. These internal channels can be selected similarly to the external channels via CS3–CS0 bits in the ADCCON2 SFR.

The ADuC814 is shipped with factory programmed offset and gain calibration coefficients that are automatically downloaded to the ADC on a power-on or RESET event, ensuring optimum ADC performance. The ADC core contains automatic endpoint self-calibration and system calibration options that allow the user to overwrite the factory programmed coefficients if desired and tailor the ADC transfer function to the system in which it is being used.

ADC TRANSFER FUNCTION

The analog input range for the ADC is 0 V to V_{REF}. For this range, the designed code transitions occur midway between successive integer LSB values, i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS –3/2 LSBs. The output coding is straight binary with 1 LSB = FS/4096 or 2.5 V/4096 = 0.61 mV when V_{REF} = 2.5 V. The ideal input/output transfer characteristic for the 0 V to V_{REF} range is shown in Figure 23.

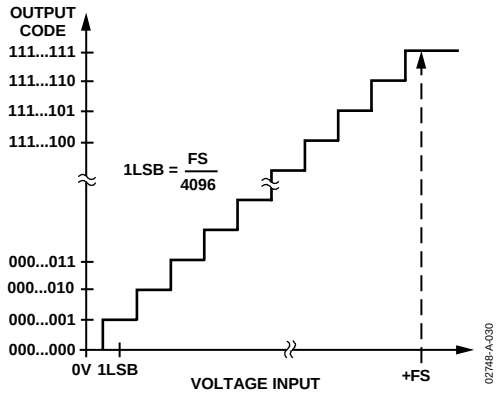

Figure 23. ADuC814 ADC Transfer Function

ADC Data Output Format

Once configured via the ADCCON1–3 SFRs, the ADC converts the analog input and provides an ADC 12-bit result word in the ADCDATAH/L SFRs. The ADCDATAL SFR contains the bottom 8 bits of the 12-bit result. The bottom nibble of the ADCDATAH SFR contains the top 4 bits of the result, while the top nibble contains the channel ID of the ADC channel which has been converted on. This ID corresponds to the channel selection bits CD3–CD0 in the ADCCON2 SFR. The format of the ADC 12-bit result word is shown in Figure 24.

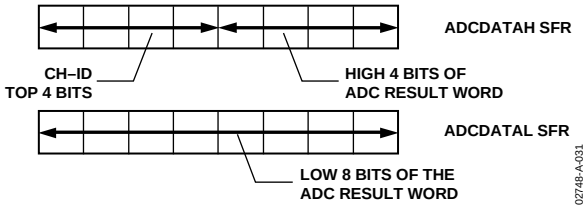

Figure 24. ADC Result Format

ADCCON3 (ADC CONTROL SFR 3)

The ADCCON3 register controls the operation of various calibration modes as well as giving an indication of ADC busy status.

SFR Address F5H
SFR Power-On Default 00H

BUSY	GNCLD	AVGS1	AVGS0	OFCLD	MODCAL	TYPECAL	SCAL

Table 8. ADCCON3 SFR Bit Designations

Bit No.	Name	Description
7	BUSY	ADC Busy Status Bit. BUSY is a read-only status bit that is set during a valid ADC conversion or calibration cycle. Busy is automatically cleared by the core at the end of a conversion or calibration cycle.
6	GNCLD	Gain Calibration Disable Bit. This bit enables/disables the gain calibration coefficients from affecting the ADC results. Set to 0 to enable gain calibration coefficient Set to 1 to disable gain calibration coefficient.
5	AVGS1	Number of Averages Selection Bits.
4	AVGS0	This bit selects the number of ADC readings averaged for each bit decision during a calibration cycle. AVGS1 AVGS0 Number of Averages 0 0 15 0 1 1 1 0 31 1 1 63
3	OFCLD	Offset Calibration Disable Bit. This bit enables/disables the offset calibration coefficients from affecting the ADC results. Set to 0 to enable offset calibration coefficient. Set to 1 to disable the offset calibration coefficient
2	MODCAL	Calibration Mode Select Bit. This bit should be set to 1 for all calibration cycles.
1	TYPECAL	Calibration Type Select Bit. This bit selects between offset (zero-scale) and gain (full-scale) calibration. Set to 0 for offset calibration. Set to 1 for gain calibration.
0	SCAL	Start Calibration Cycle Bit. When set, this bit starts the selected calibration cycle. It is automatically cleared when the calibration cycle is completed.

Table 10. Some Single-Supply Op Amps

Op Amp Model	Characteristics
OP281/OP481	Micropower
OP191/OP291/OP491	I/O good up to V_{DD}, low cost
OP196/OP296/OP496	I/O to V_{DD}, micropower, low cost
OP183/OP283	High gain-bandwidth product
OP162/OP262/OP462	High GBP, micropackage
AD820/OP822/OP824	FET input, low cost
AD823	FET input, high GBP

Keep in mind that the ADC's transfer function is 0 V to V_{REF}, and any signal range lost to amplifier saturation near ground impacts dynamic range. Though the op amps in Table 10 are capable of delivering output signals very closely approaching ground, no amplifier can deliver signals all the way to ground when powered by a single supply. Therefore, if a negative supply is available, one could consider using it to power the front end amplifiers. If you do, however, be sure to include the Schottky diodes shown in Figure 26 (or at least the lower of the two diodes) to protect the analog input from undervoltage conditions.

VOLTAGE REFERENCE CONNECTIONS

The on-chip 2.5 V band gap voltage reference can be used as the reference source for the ADC and DACs. To ensure the accuracy of the voltage reference, decouple the V_{REF} and the C_{REF} pin to ground with 0.1 µF capacitors as shown in Figure 27.

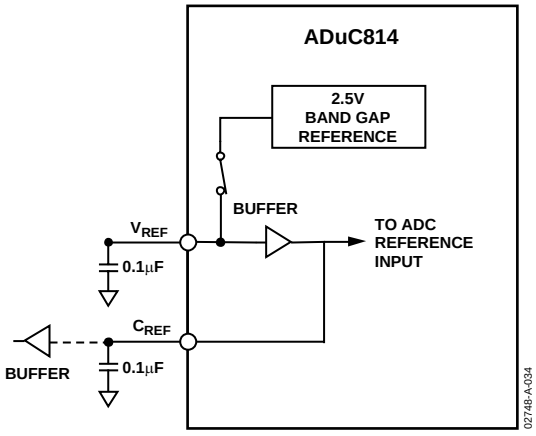

Figure 27. Decoupling V_{REF} and C_{REF}

If the internal voltage reference is to be used as a reference for external circuitry, the C_{REF} output should be used. However, a buffer must be used in this case to ensure that no current is drawn from the C_{REF} pin itself. The voltage on the C_{REF} pin is that of an internal node within the buffer block, and its voltage is critical to ADC and DAC accuracy. As outlined in the Reference Input/Output section of the Specifications table, the internal band gap reference takes typically 80 msecs to power on and settle to its final value. To ensure accurate ADC operation, one should wait for the ADC to settle after power-on.

If an external voltage reference is preferred, it should be connected to the V_{REF} and C_{REF} pins as shown in Figure 28. Bit 6 of the ADCCON1 SFR must be set to 1 to switch in the external reference voltage. To ensure accurate ADC operation, the voltage applied to V_{REF} must be between 1.0 V and AV_{DD}. In situations where analog input signals are proportional to the power supply (such as some strain gage applications) it can be desirable to connect the V_{REF} pin directly to AV_{DD}.

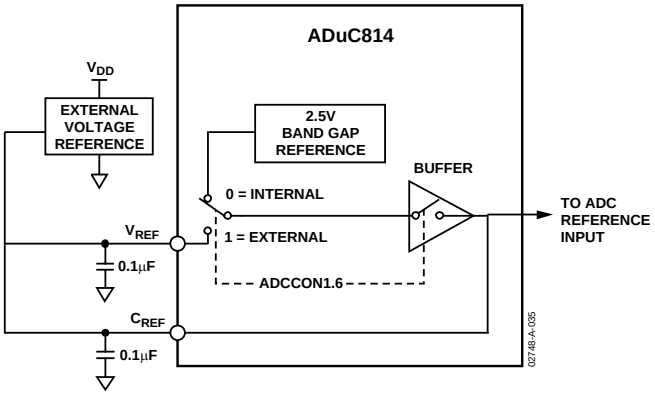

Figure 28. Using an External Voltage Reference

Operation of the ADC with a reference voltage below 1.0 V, however, may incur loss of accuracy eventually resulting in missing codes or non-monotonicity. For that reason, do not use a reference voltage less than 1.0 V.

CONFIGURING THE ADC

In configuring the ADC a number of parameters need to be set up. These parameters can be configured using the three SFRs: ADCCON1, ADCCON2, and ADCCON3, which are detailed in the following sections.

The ADCCLK determines the speed at which the ADC logic runs while performing an ADC conversion. All ADC timing parameters are calculated from the ADCCLK frequency. On the ADuC814, the ADCCLK is derived from the maximum core frequency (F_{CORE}), 16.777216 MHz. The ADCCLK frequency is selected via ADCCON1 Bits 5 and 4, which provide four core clock divide ratios of 8, 4, 16, and 32, generating ADCCLK values of 2 MHz, 4 MHz, 1 MHz, and 500 kHz, respectively.

The acquisition time (T_{ACQ}) is the number of ADCCLKs that the ADC input circuitry uses to sample the input signal. In most cases, an acquisition time of one ADCCLK provides more than adequate time for the ADuC814 to acquire its signal before switching the internal track-and-hold amplifier into hold mode. The only exception is a high source impedance analog input, but this should be buffered first anyway because high source impedances can cause significant dc errors (see Table 6). ADCCON1 Bits 3 and 2 are used to select acquisition times of 1, 2, 3, and 4 ADCCLKs.

USING FLASH/EE DATA MEMORY

The user Flash/EE data memory array consists of 640 bytes that are configured into 160 (00H to 9FH) 4-byte pages as shown in Figure 36.

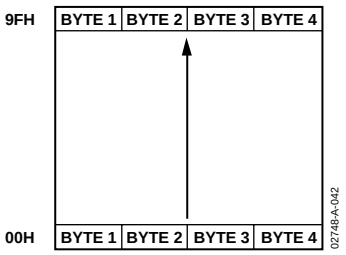

Figure 36. Flash/EE Data Memory Configuration

As with other ADuC814 user-peripheral circuits, the interface to this memory space is via a group of registers mapped in the SFR space. EADRL is used to hold the 8-bit address of the page to be accessed. A group of four data registers (EDATA1–4) is used to hold 4-byte page data just accessed. Finally, ECON is an 8-bit control register that may be written with one of five Flash/EE memory access commands to trigger various read, write, erase, and verify functions. These registers can be summarized as follows:

ECON

SFR Address	B9H
Function	Controls access to 640 bytes Flash/EE data space.
Default	00H

EADRL

SFR Address	C6H
Function	Holds the Flash/EE data page address. (640 bytes = > 160 page addresses)
Default	00H

EDATA1–4

SFR Address	BCH to BFH, respectively
Function	Holds Flash/EE data memory page write or page read data bytes.
Default	EDATA1–4 > 00H

A block diagram of the SFR interface to the Flash/EE data memory array is shown in Figure 37.

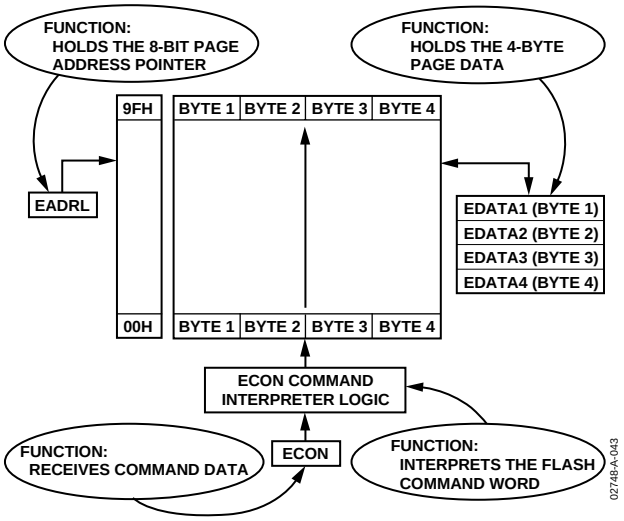

Figure 37. Flash/EE Data Memory Control and Configuration

ECON—Flash/EE Memory Control SFR

This SFR acts as a command interpreter and may be written with one of five command modes to enable various read, program, and erase cycles as detailed in Table 11.

Table 11. ECON–Flash/EE Memory Control Register Command Modes

Command Byte	Command Mode	Description
01H	READ	Results in 4 bytes being read into EDATA1–4 from memory page address contained in EADRL.
02H	PROGRAM	Results in 4 bytes (EDATA1–4) being written to memory page address in EADRL. This write command assumes the designated write page has been erased.
03H	Reserved	For internal use. 03H should not be written to the ECON SFR.
04H	VERIFY	Allows the user to verify if data in EDATA1–4 is contained in page address designated by EADRL. A subsequent read of the ECON SFR results in a zero being read if the verification is valid, a nonzero value is read to indicate an invalid verification.
05H	ERASE	Results in an erase of the 4-byte page designated in EADRL.
06H	ERASE-ALL	Results in an erase of the full Flash/EE aata memory, 160-page (640 bytes) array.
07H to FFH	Reserved	For future use.

FLASH/EE MEMORY TIMING

The typical program/erase times for the Flash/EE data memory are

Erase Full Array (640 bytes)	2 ms
Erase Single Page (4 bytes)	2 ms
Program Page (4 bytes)	250 µs
Read Page (4 bytes)	Within single instruction cycle

Using the Flash/EE Memory Interface

As with all Flash/EE memory architectures, the array can be programmed in-system at a byte level, although it must be erased first, the erasure being performed in page blocks (4-byte pages in this case).

A typical access to the Flash/EE data array involves setting up the page address to be accessed in the EADRL SFR, configuring the EDATA1–4 with data to be programmed to the array (the EDATA SFRs are not written to for read accesses), and finally, writing the ECON command word, which initiates one of the modes shown Table 11.

Note that a given mode of operation is initiated as soon as the command word is written to the ECON SFR. The core microcontroller operation on the ADuC814 is idled until the requested program/read or erase mode is completed. In practice, this means that even though the Flash/EE memory mode of operation is typically initiated with a two-machine cycle MOV instruction (to write to the ECON SFR), the next instruction cannot be executed until the Flash/EE operation is complete (250 µs or 2 ms later). This means that the core does not respond to interrupt requests until the Flash/EE operation is complete, though the core peripheral functions like counter/timers continue to count and time as configured throughout this period. Although the 640-byte user Flash/EE array is shipped from the factory pre-erased, i.e., byte locations set to FFH, it is nonetheless good programming practice to include an ERASE-ALL routine as part of any configuration/setup code running on the ADuC814. An ERASE-ALL command consists of writing 06H to the ECON SFR, which initiates an erasure of all 640 byte locations in the Flash/EE array. This command coded in 8051 assembly appears as

```
MOV ECON, #06H            ; Erase all Command
                          ; 2 ms Duration
```

Programming a Byte

In general terms, a byte in the Flash/EE array can be programmed only if it has been erased previously. To be more specific, a byte can only be programmed if it already holds the value FFH. Because of the Flash/EE architecture, this erasure must happen at a page level; therefore, a minimum of four bytes (1 page) are erased when an ERASE command is initiated.

A more specific example of the program-byte process is shown below. In this example the user writes F3H into the second byte on Page 03H of the Flash/EE data memory space while preserving the other three bytes already in this page. Because the user is required to modify only one of the page bytes, the full page must be first read so that this page can then be erased without the existing data being lost. This example, coded in 8051 assembly, appears as

```
MOV EADRL,#03H          ; Set Page Address
                        ; Pointer
MOV ECON,#01H           ; Read Page
MOV EDATA2,#0F3H        ; Write New Byte
MOV ECON,#05H           ; Erase Page
MOV ECON,#02H           ; Write Page
                        ; Program Flash/EE)
```

TIME INTERVAL COUNTER (TIC)

A time interval counter is provided on-chip for counting longer intervals than the standard 8051 compatible timers are capable of. The TIC is capable of time-out intervals ranging from 1/128th second to 255 hours. Furthermore, this counter is clocked by the crystal oscillator rather than by the PLL and thus has the ability to remain active in power-down mode and to time long power-down intervals. This has obvious applications for remote battery-powered sensors where regular, widely spaced readings are required.

Six SFRs are associated with the time interval counter, TIMECON being its control register. Depending on the configuration of the IT0 and IT1 bits in TIMECON, the selected time counter register overflow clocks the interval counter. When this counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) is set and generates an interrupt if enabled. (See IEIP2 SFR description under the Interrupt System section.) If the ADuC814 is in power-down mode, again with TIC interrupt enabled, the TII bit wakes up the device and resumes code execution by vectoring directly to the TIC interrupt service vector address at 0053H. The TIC-related SFRs are described in Table 14. Note that the time based SFRs can be written initially with the current time; the TIC can then be controlled and accessed by the user software. In effect, this facilitates the implementation of a real-time clock. A block diagram of the TIC is shown in Figure 43.

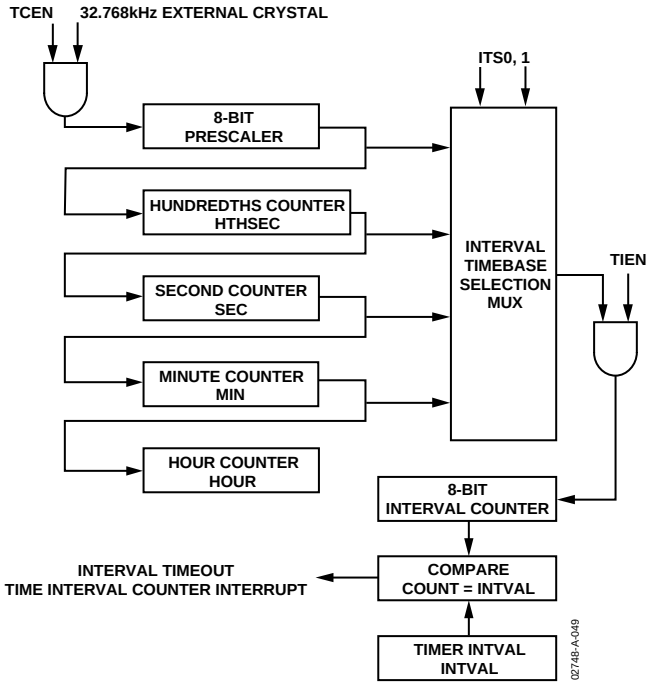

Figure 43. Time Interval Counter, Simplified Block Diagram

INTVAL	**User Time Interval Select Register**
Function	User code writes the required time interval to this register. When the 8-bit interval counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) is set and generates an interrupt if enabled. (See the IEIP2 SFR description in the Interrupt System section.)
SFR Address	A6H
Power-On Default	00H
Bit Addressable	No
Valid Value	0 to 255 decimal

HTHSEC	**Hundredths Seconds Time Register**
Function	This register is incremented in 1/128 second intervals once TCEN in TIMECON is active. The HTHSEC SFR counts from 0 to 127 before rolling over to increment the SEC time register.
SFR Address	A2H
Power-On Default	00H
Bit Addressable	No
Valid Value	0 to 127 decimal

SEC	**Seconds Time Register**
Function	This register is incremented in 1-second intervals once TCEN in TIMECON is active. The SEC SFR counts from 0 to 59 before rolling over to increment the MIN time register.
SFR Address	A3H
Power-On Default	00H
Bit Addressable	No
Valid Value	0 to 59 decimal

MIN	**Minutes Time Register**
Function	This register is incremented in 1-minute intervals once TCEN in TIMECON is active. The MIN SFR counts from 0 to 59 before rolling over to increment the HOUR time register.
SFR Address	A4H
Power-On Default	00H
Bit Addressable	No
Valid Value	0 to 59 decimal

HOUR	**Hours Time Register**
Function	This register is incremented in 1-hour intervals once TCEN in TIMECON is active. If the TFH bit (TIMECON.6) is set to 1 the HOUR SFR counts from 0 to 23 before rolling over to 0. If the TFH bit is set to 0, the HOUR SFR counts from 0 to 255 before rolling over to 0.
SFR Address	A5H
Power-On Default	00H
Bit Addressable	No
Valid Value	0 to 23 decimal

ADuC814 CONFIGURATION REGISTER (CFG814)

The ADuC814 is housed in a 28-lead TSSOP package. To maintain as much functional compatibility with other MicroConverter products, some pins share multiple I/O functionality. Switching between these functions is controlled via the ADuC814 configuration SFR, CFG814, located at SFR address 9CH. A summary of these functions is described and a detailed bit designation for the CFG814 SFR is given in Table 17.

Serial Peripheral Interface

The SPI interface on the ADuC814 shares the same pins as digital outputs P3.5, P3.6, and P3.7. The SPE bit in SPICON is used to select which interface is active at any one time. This is described in greater detail in the next section. By default, these pins operate as standard Port 3 pins. Bit 0 of the CFG814 SFR must be set to 1 to enable the SPI interface on these Port 3 pins.

External Clock

The ADuC814 is intended for use with a 32.768 kHz watch crystal. The on-chip PLL locks onto a multiple of this to provide a stable 16.777216 MHz clock for the device. On the ADuC814, P3.5 alternate functions include T1 input and slave select in SPI master mode. P3.5 also functions as external clock input, EXTCLK, selected via Bit 1 of the CFG814 SFR. When selected, this external clock bypasses the PLL and is used as the clock for the device, therefore allowing the ADuC814 to be synchronized to the rest of the application system. The maximum input frequency of this external clock is 16.777216 MHz. If selected, the EXTCLK signal affects the timing of the majority of peripherals on the ADuC814 including the ADC, EEPROM controller, watchdog timer, SPI interface clock, and the MicroConverter core clock.

CFG814	**ADuC814 Configuration Register**
SFR Address	9CH
Power-On Default	04H
Bit Addressable	No

						EXTCLK	SER_EN

Table 17. CFG814 SFR Bit Designations

Bit No.	Name	Description
1	EXTCLK	External Clock Selection Bit. Set to 1 to enable EXTCLK as MCU core clock. Cleared to 0 to enable XTAL and PLL as the MCU core clock.
0	SER_EN	Serial Interface Enable Bit. Set to 1 by the user to enable the SPI interface onto the P3.5, P3.6, and P3.7 pins. Cleared to 0 by the user to enable standard Port 3 functionality on the P3.5, P3.6, and P3.7 pins.

UART SERIAL INTERFACE

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can begin receiving a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, the first byte is lost. The physical interface to the serial data network is via Pins RxD (P3.0) and TxD (P3.1), while the SFR interface to the UART is comprised of the following registers.

SBUF

The serial port receive and transmit registers are both accessed through the SBUF SFR (SFR address = 99H). Writing to SBUF loads the transmit register and reading SBUF accesses a physically separate receive register.

SCON	**UART Serial Port Control Register**
SFR Address	98H
Power-On Default	00H
Bit Addressable	Yes

SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Table 26. SCON SFR Bit Designations

Bit No.	Name	Description
7	SM0	UART Serial Mode Select Bits.
6	SM1	These bits select the serial port operating mode as follows: SM0 SM1 Selected Operating Mode 0 0 Mode 0: Shift Register, fixed baud rate (Core_Clk/2) 0 1 Mode 1: 8-bit UART, variable baud rate 1 0 Mode 2: 9-bit UART, fixed baud rate (Core_Clk/64) or (Core_Clk/32) 1 1 Mode 3: 9-bit UART, variable baud rate
5	SM2	Multiprocessor Communication Enable Bit. Enables multiprocessor communication in Modes 2 and 3. In Mode 0, SM2 should be cleared. In Mode 1, if SM2 is set, RI is not activated if a valid stop bit is not received. If SM2 is cleared, RI is set as soon as the byte of data is received. In Mode 2 or 3, if SM2 is set, RI is not activated if the received ninth data bit in RB8 is 0. If SM2 is cleared, RI is set as soon as the byte of data is received.
4	REN	Serial Port Receive Enable Bit. Set by the user software to enable serial port reception. Cleared by the user software to disable serial port reception.
3	TB8	Serial Port Transmit (Bit 9). The data loaded into TB8 is the ninth data bit that is transmitted in Modes 2 and 3.
2	RB8	Serial port Receiver Bit 9. The ninth data bit received in Modes 2 and 3 is latched into RB8. For Mode 1, the stop bit is latched into RB8.
1	TI	Set by hardware at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in Modes 1, 2, and 3. Cleared by the user software.
0	RI	Serial Port Receive Interrupt Flag. Set by hardware at the end of the eighth bit in Mode 0, or halfway through the stop bit in Modes 1, 2, and 3. Cleared by user software.

Timer 2 Generated Baud Rates

Baud rates can also be generated using Timer 2. Using Timer 2 is similar to using Timer 1 in that the timer must overflow 16 times before a bit is transmitted/received. Because Timer 2 has a 16-bit autoreload mode, a wide range of baud rates is possible using Timer 2.

Modes 1 and 3 Baud Rate = (1/16) × (*Timer 2 Overflow Rate*)

Therefore, when Timer 2 is used to generate baud rates, the timer increments every two clock cycles and not every core machine cycle as before. Therefore, it increments six times faster than Timer 1, and therefore baud rates six times faster are possible. Because Timer 2 has 16-bit autoreload capability, very low baud rates are still possible. Timer 2 is selected as the baud rate generator by setting the CLK and/or RCLK in T2CON. The baud rates for transmit and receive can be simultaneously different. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode as shown in Figure 53.

In this case, the baud rate is given by the formula

Modes 1 and 3 Baud Rate = (*Core Clk*)/
(32 × [65536 – (*RCAP2H*, *RCAP2L*)])

Table 28 shows some commonly used baud rates and how they could be calculated from a core clock frequency of 2.0971 MHz and 16.7772 MHz.

Table 28. Commonly Used Baud Rates, Timer 2

Ideal Baud	Core CLK	RCAP2H Value	RCAP2L Value	Actual Baud	% Error
19200	16.78	–1 (FFH)	–27 (E5H)	19418	1.14
9600	16.78	–1 (FFH)	–55 (C9H)	9532	0.7
2400	16.78	–1 (FFH)	–218 (26H)	2405	0.21
1200	16.78	–2 (FEH)	–181 (4BH)	1199	0.02
9600	2.10	–1 (FFH)	–7 (FBH)	9362	2.4
2400	2.10	–1 (FFH)	–27 (ECH)	2427	1.14
1200	2.10	–1 (FFH)	–55 (D7H)	1191	0.7

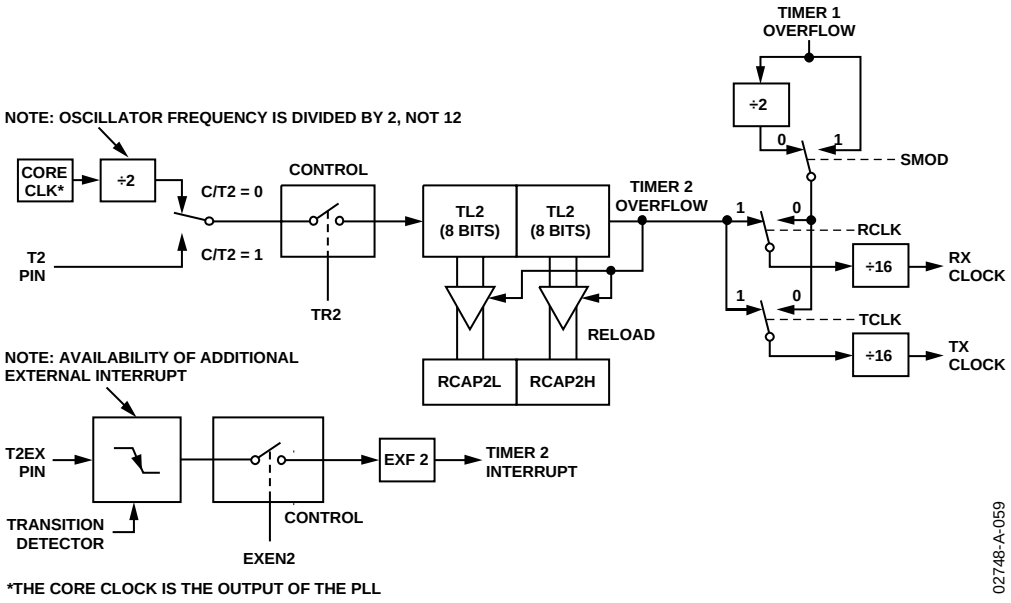

Figure 53. Timer 2, UART Baud Rates

INTERRUPT SYSTEM

The ADuC814 provides a total of twelve interrupt sources with two priority levels. The control and configuration of the interrupt system is carried out through three interrupt-related SFRs.

IE	Interrupt Enable Register
IP	Interrupt Priority Register
IEIP2	Secondary Interrupt Enable and Priority Register

IE	**Interrupt Enable Register**
SFR Address	A8H
Power-On Default	00H
Bit Addressable	Yes

EA	EADC	ET2	ES	ET1	EX1	ET0	EX0

Table 29. IE SFR Bit Designations

Bit No.	Name	Description
7	EA	Global Interrupt Enable. Set by the user to enable all interrupt sources. Cleared by the user to disable all interrupt sources.
6	EADC	ADC Interrupt. Set by the user to enable the ADC interrupt. Cleared by the user to disable the ADC interrupt.
5	ET2	Timer 2 Interrupt. Set by the user to enable the Timer 2 interrupt. Cleared by the user to disable the Timer 2 interrupt.
4	ES	UART Serial Port Interrupt. Set by the user to enable the UART serial port interrupt. Cleared by the user to disable the UART serial port interrupt.
3	ET1	Timer 1 Interrupt. Set by the user to enable the Timer 1 interrupt. Cleared by the user to disable the Timer 1 interrupt.
2	EX1	INT1 Interrupt. Set by the user to enable the External Interrupt 1. Cleared by the user to disable the External Interrupt 1.
1	ET0	Timer 0 Interrupt. Set by the user to enable the Timer 0 interrupt. Cleared by the user to disable the Timer 0 interrupt.
0	EX0	INT0 Interrupt. Set by the user to enable the External Interrupt 0. Cleared by the user to disable the External Interrupt 0.

TIMING SPECIFICATIONS[1,2,3]

Table 34. Clock Input (External Clock Driven XTAL1)

AV_{DD} = 2.7 V to 3.3 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.3 V or 4.75 V to 5.25 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted

		32.768 kHz External Crystal			
Parameter		**Min**	**Typ**	**Max**	**Unit**
t_{CK}	XTAL1 Period		30.52		µs
t_{CKL}	XTAL1 Width Low		15.16		µs
t_{CKH}	XTAL1 Width High		15.16		µs
t_{CKR}	XTAL1 Rise Time		20		ns
t_{CKF}	XTAL1 Fall Time		20		ns
$1/t_{CORE}$	ADuC814 Core Clock Frequency[4]	0.131		16.78	MHz
t_{CORE}	ADuC814 Core Clock Period[5]		0.476		µs
t_{CYC}	ADuC814 Machine Cycle Time[6]	0.72	5.7	91.55	µs

[1] AC inputs during testing are driven at DV_{DD} – 0.5 V for a Logic 1, and at 0.45 V for a Logic 0. Timing measurements are made at V_{IH} min for a Logic 1, and at V_{IL} max for a Logic 0 as shown in Figure 61.
[2] For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs as shown in Figure 61.
[3] C_{LOAD} for all outputs = 80 pF, unless otherwise noted.
[4] ADuC814 internal PLL locks onto a multiple (512 times) the external crystal frequency of 32.768 kHz to provide a stable 16.777216 MHz internal clock for the system. The core can operate at this frequency or at a binary submultiple called Core_Clk, selected via the PLLCON SFR.
[5] This number is measured at the default Core_Clk operating frequency of 2.09 MHz.
[6] ADuC814 Machine Cycle Time is nominally defined as 12/Core_CLK.

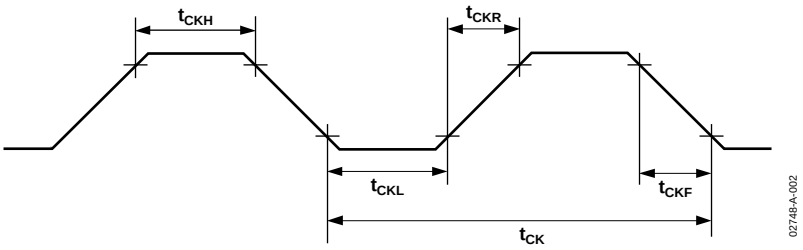

Figure 60. XTAL1 Input

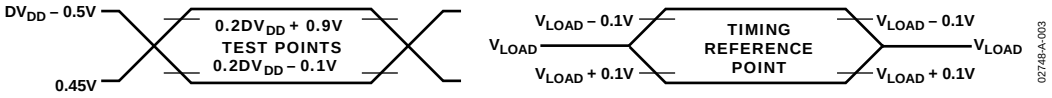

Figure 61. Timing Waveform Characteristics

Table 35. UART Timing (Shift Register Mode)

Parameter		16.78 MHz Core_Clk			Variable Core_Clk			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{XLXL}	Serial Port Clock Cycle Time		715			12 t_{CORE}		µs
t_{QVXH}	Output Data Setup to Clock	463			10 t_{CORE}	−133		ns
t_{DVXH}	Input Data Setup to Clock	252			2 t_{CORE}	+133		ns
t_{XHDX}	Input Data Hold after Clock	0			0			ns
t_{XHQX}	Output Data Hold after Clock	22			2 t_{CORE}	−117		ns

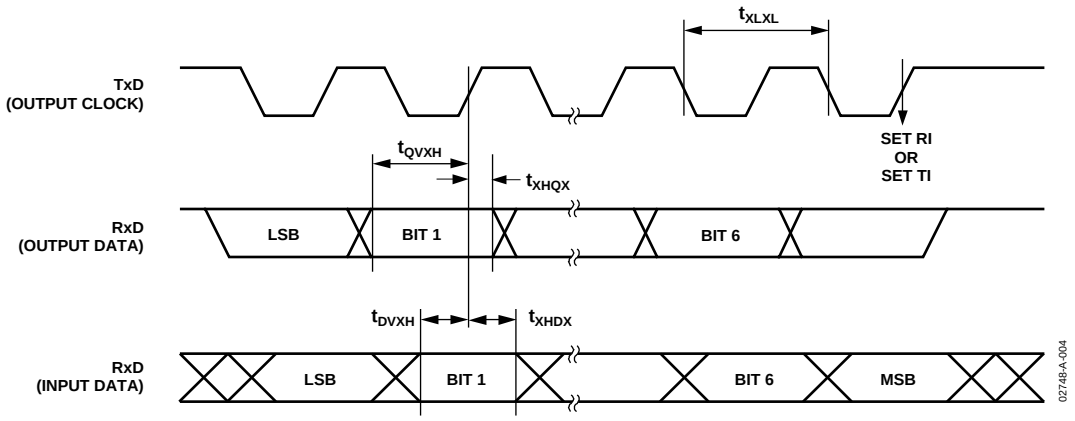

Figure 62. UART Timing in Shift Register Mode