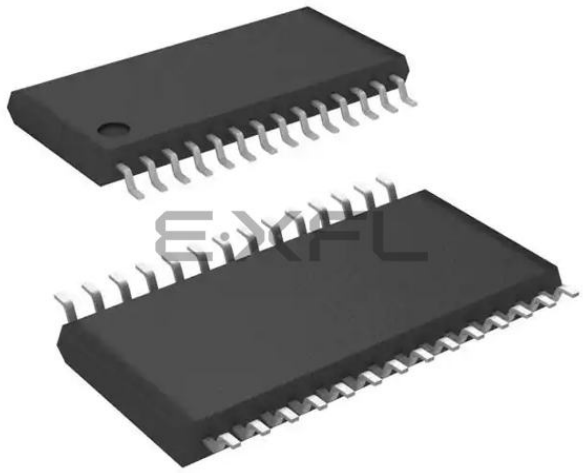

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	16.78MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PSM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 6x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	28-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc814aruz-reel

PIN CONFIGURATION AND FUNCTION DESCRIPTION

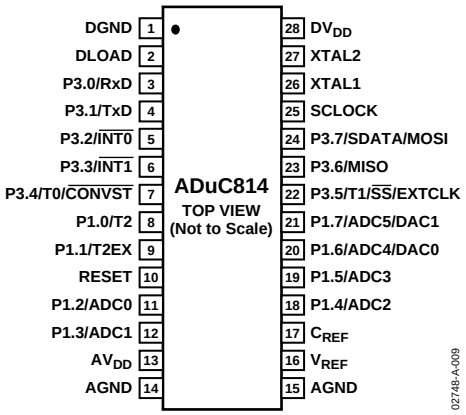

Figure 2. Pin Configuration

Table 3. Pin Descriptions

Pin No.	Mnemonic	Type	Function
1	DGND	S	Digital Ground. Ground reference point for the digital circuitry.
2	DLOAD	I	Debug/Serial Download Mode. Enables when pulled high through a resistor on power-on or RESET. In this mode, DLOAD may also be used as an external emulation I/O pin, therefore the voltage level at this pin must not be changed during this mode of operation because it may cause an emulation interrupt that halts code execution. User code is executed when this pin is pulled low on power-on or RESET.
3–7	P3.0 – P3.4	I/O	Bidirectional Port Pins with Internal Pull-Up Resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, with Port 3 pins being pulled low externally, they source current because of the internal pull-up resistors. When driving a 0-to-1 output transition, a strong pull-up is active during S1 of the instruction cycle. Port 3 pins also have various secondary functions which are described next.
3	P3.0/RxD	I/O	Receiver Data Input (asynchronous) or Data Input/Output (synchronous) in Serial (UART) Mode.
4	P3.1/TxD	I/O	Transmitter Data Output (asynchronous) or Clock Output (synchronous) in Serial (UART) Mode.
5	P3.2/$\overline{\text{INT0}}$	I/O	Interrupt 0, programmable edge or level-triggered interrupt input, which can be programmed to one of two priority levels. This pin can also be used as agate control input to Timer 0.
6	P3.3/$\overline{\text{INT1}}$	I/O	Interrupt 1, programmable edge or level-triggered interrupt input, which can be programmed to one of two priority levels. This pin can also be used as agate control input to Timer 1.
7	P3.4/T0/ $\overline{\text{CONVST}}$	I/O	Timer/Counter 0 Input and External Trigger Input for ADC Conversion Start.
8–9	P1.0–P1.1	I/O	Bidirectional Port Pins with Internal Pull-Up Resistors. Port 1 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs ,with Port 1 pins being pulled low externally, they source current because of the internal pull-up resistors When driving a 0-to-1 output transition a strong pull-up is active during S1 of the instruction cycle. Port 1 pins also have various secondary functions which are described as follows.
8	P1.0/T2	I/O	Timer 2 Digital Input. Input to Timer/Counter 2. When enabled, Counter 2 is incremented in response to a 1 to 0 transition of the T2 input.
9	P1.1/T2EX	I/O	Digital Input. Capture/Reload trigger for Counter 2.
10	RESET	I	Reset Input. A high level on this pin while the oscillator is running resets the device. There is an internal weak pull-down and a Schmitt-trigger input stage on this pin.
11–12	P1.2–P1.3	I	Port 1.2 to P1.3. These pins have no digital output drivers, i.e., they can only function as digital inputs, for which 0 must be written to the port bit. These port pins also have the following analog functionality:
11	P1.2/ADC0	I	ADC Input Channel 0. Selected via ADCCON2 SFR.
12	P1.3/ADC1	I	ADC Input Channel 1. Selected via ADCCON2 SFR.
13	AV_{DD}	S	Analog Positive Supply Voltage, 3 V or 5 V.
14–15	AGND	G	Analog Ground. Ground reference point for the analog circuitry.
16	V_{REF}	I/O	Reference Input/Output. This pin is connected to the internal reference through a switch and is the reference source for the analog to digital converter. The nominal internal reference voltage is 2.5 V and this appears at the pin. This pin can be used to connect an external reference to the analog to digital converter by setting ADCCON1.6 to 1. Connect 0.1 µF between this pin and AGND.

TYPICAL PERFORMANCE CURVES

The typical performance plots presented in this section illustrate typical performance of the ADuC814 under various operating conditions. Note that all typical plots in this section were generated using the ADuC814BRU, i.e., the B-grade part.

Figure 3 and Figure 4 show typical ADC integral nonlinearity (INL) errors from ADC Code 0 to Code 4095 at 5 V and 3 V supplies, respectively. The ADC is using its internal reference (2.5 V) and operating at a sampling rate of 152 kHz. The typical worst-case errors in both plots are just less than 0.3 LSBs.

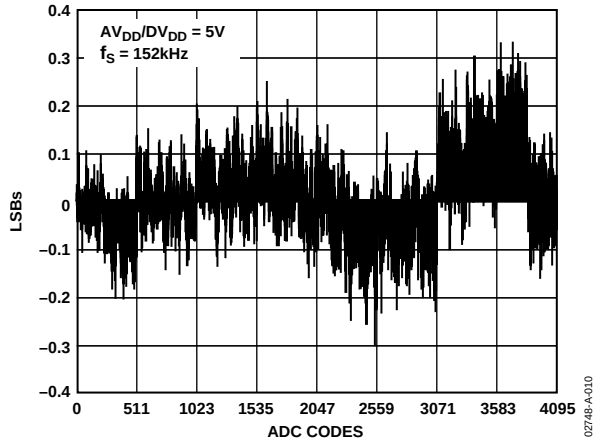

Figure 3. Typical INL Error, V_{DD} = 5 V

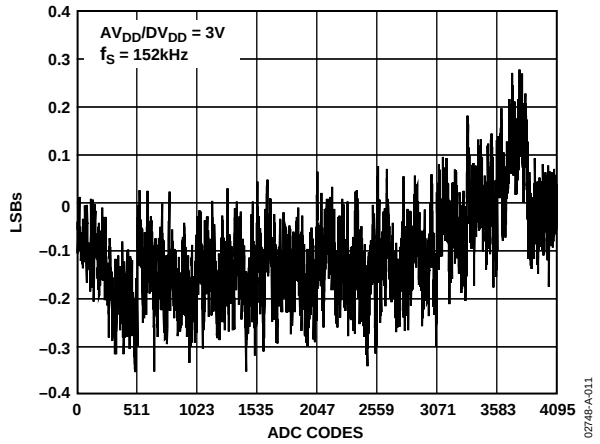

Figure 4. Typical INL Error, V_{DD} = 3 V

Figure 5 and Figure 6 show the variation in worst-case positive (WCP) INL and worst-case negative (WCN) INL versus external reference input voltage.

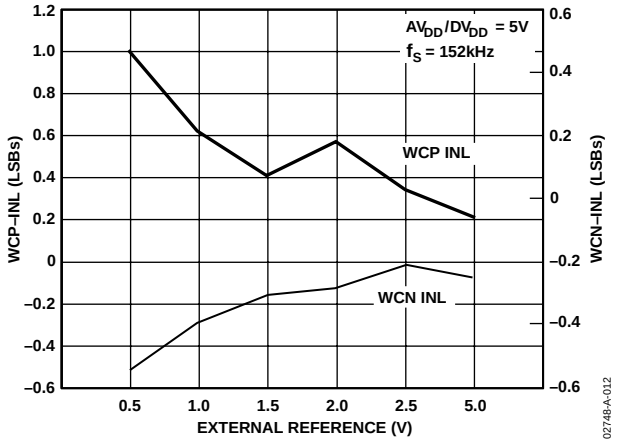

Figure 5. Typical Worst-Case INL Error vs. V_{REF}, V_{DD} = 5 V

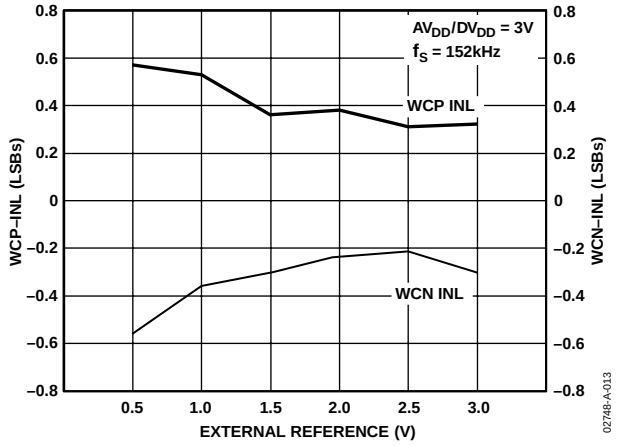

Figure 6. Typical Worst-Case INL Error vs. V_{REF}, V_{DD} = 3 V

Figure 7 and Figure 8 show typical ADC differential nonlinearity (DNL) errors from ADC Code 0 to Code 4095 at 5 V and 3 V supplies, respectively. The ADC is using its internal reference (2.5 V) and operating at a sampling rate of 152 kHz. The typical worst-case errors in both plots are just less than 0.2 LSBs.

Figure 13 and Figure 14 show typical FFT plots for the ADuC814. These plots were generated using an external clock input via P3.5 to achieve coherent sampling. The ADC is using its internal reference (2.5 V) sampling a full-scale, 10 kHz sine wave test tone input at a sampling rate of 149.79 kHz. The resultant FFTs shown at 5 V and 3 V supplies illustrate an excellent 100 dB noise floor, a 71 dB signal-to-noise ratio (SNR), and a THD greater than −80 dB.

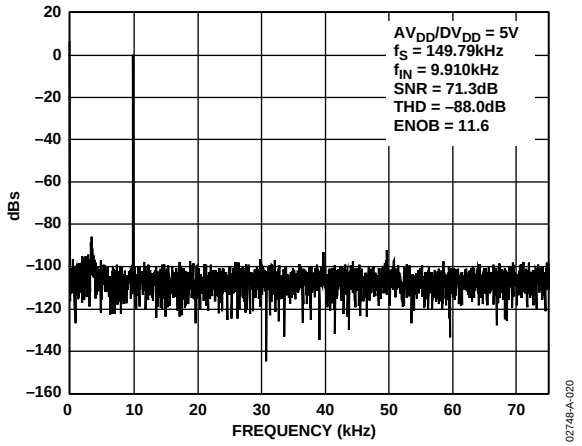

Figure 13. ADuC814 Dynamic Performance at V_{DD} = 5 V

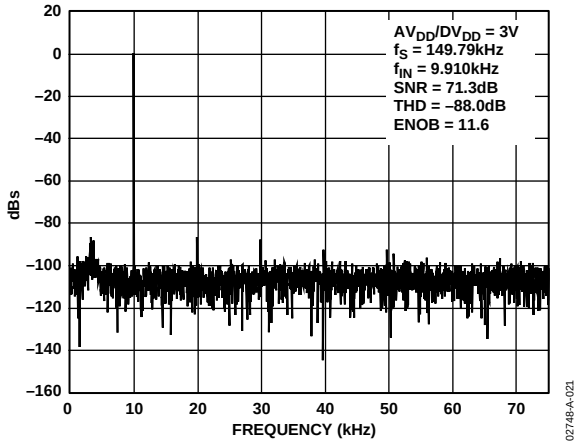

Figure 14. ADuC814 Dynamic Performance at V_{DD} = 3 V

Figure 15 and Figure 16 show typical dynamic performance versus external reference voltages. Again excellent ac performance can be observed in both plots with some roll-off being observed as V_{REF} falls below 1 V.

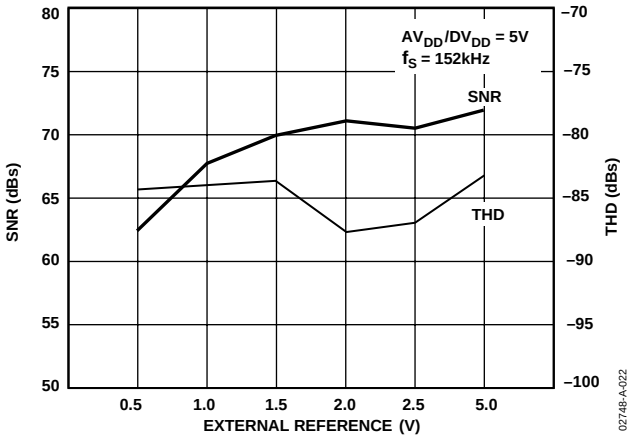

Figure 15. Typical Dynamic Performance vs. V_{REF}, V_{DD} = 5 V

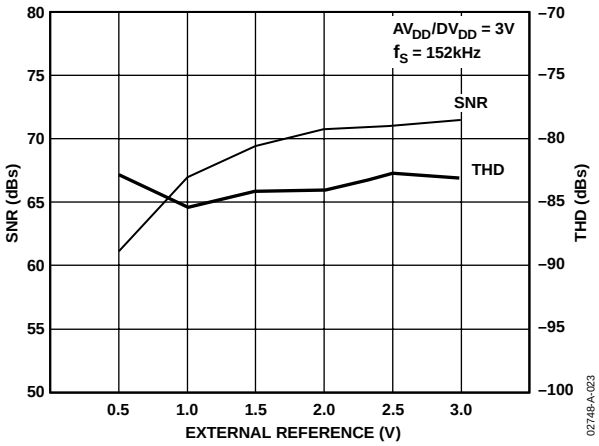

Figure 16. Typical Dynamic Performance vs. V_{REF}, V_{DD} = 3 V

ADC CIRCUIT INFORMATION

GENERAL OVERVIEW

The ADC block incorporates a 4.05 msec, 6-channel, 12-bit resolution, single-supply ADC. This block provides the user with a multichannel multiplexer, track-and-hold amplifier, on-chip reference, offset calibration features and ADC. All components in this block are easily configured via a 3-register SFR interface.

The ADC consists of a conventional successive-approximation converter based around a capacitor DAC. The converter accepts an analog input range of 0 V to V_{REF}. A precision, factory calibrated 2.5 V reference is provided on-chip. An external reference may also be used via the external V_{REF} pin. This external reference can be in the range 1.0 V to AV_{DD}.

Single or continuous conversion modes can be initiated in software. In hardware, a convert signal can be applied to an external pin (CONVST), or alternatively Timer 2 can be configured to generate a repetitive trigger for ADC conversions.

The ADuC814 has a high speed ADC to SPI interface data capture logic implemented on-chip. Once configured, this logic transfers the ADC data to the SPI interface without the need for CPU intervention.

The ADC has six external input channels. Two of the ADC channels are multiplexed with the DAC outputs, ADC4 with DAC0, and ADC5 with DAC1. When the DAC outputs are in use, any ADC conversion on these channels represents the DAC output voltage. Due care must be taken to ensure that no external signal is trying to drive these ADC/DAC channels while the DAC outputs are enabled.

In addition to the six external channels of the ADC, five internal signals are also routed through the front end multiplexer. These signals include a temperature monitor, DAC0, DAC1, V_{REF}, and AGND. The temperature monitor is a voltage output from an on-chip band gap reference, which is proportional to absolute temperature. These internal channels can be selected similarly to the external channels via CS3–CS0 bits in the ADCCON2 SFR.

The ADuC814 is shipped with factory programmed offset and gain calibration coefficients that are automatically downloaded to the ADC on a power-on or RESET event, ensuring optimum ADC performance. The ADC core contains automatic endpoint self-calibration and system calibration options that allow the user to overwrite the factory programmed coefficients if desired and tailor the ADC transfer function to the system in which it is being used.

ADC TRANSFER FUNCTION

The analog input range for the ADC is 0 V to V_{REF}. For this range, the designed code transitions occur midway between successive integer LSB values, i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS –3/2 LSBs. The output coding is straight binary with 1 LSB = FS/4096 or 2.5 V/4096 = 0.61 mV when V_{REF} = 2.5 V. The ideal input/output transfer characteristic for the 0 V to V_{REF} range is shown in Figure 23.

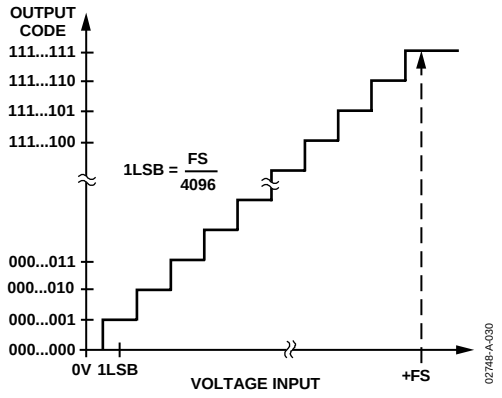

Figure 23. ADuC814 ADC Transfer Function

ADC Data Output Format

Once configured via the ADCCON1–3 SFRs, the ADC converts the analog input and provides an ADC 12-bit result word in the ADCDATAH/L SFRs. The ADCDATAL SFR contains the bottom 8 bits of the 12-bit result. The bottom nibble of the ADCDATAH SFR contains the top 4 bits of the result, while the top nibble contains the channel ID of the ADC channel which has been converted on. This ID corresponds to the channel selection bits CD3–CD0 in the ADCCON2 SFR. The format of the ADC 12-bit result word is shown in Figure 24.

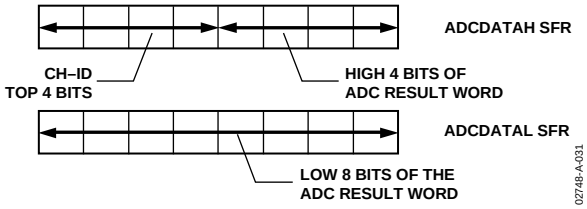

Figure 24. ADC Result Format

DACxH/L	DAC0 and DAC1 Data Registers
Function	DAC Data Registers, written by the user to update the DAC outputs.
SFR Address	DAC0L (DAC0 data low byte) –> F9H DAC0H (DAC0 data high byte) –> FAH; DAC1L (DAC1 data low byte) –> FBH DAC1H (DAC1 data high byte) –> FCH
Power-On Default	00H –> Both DAC0 and DAC1 data registers.
Bit Addressable	No –> Both DAC0 and DAC1 data registers.

The 12-bit DAC data should be written into DACxH/L right-justified such that DACL contains the lower eight bits, and the lower nibble of DACH contains the upper four bits.

Using the DACs

The on-chip DAC architecture consists of a resistor string DAC followed by an output buffer amplifier, the functional equivalent of which is illustrated in Figure 38. Features of this architecture include inherent guaranteed monotonicity and excellent differential linearity.

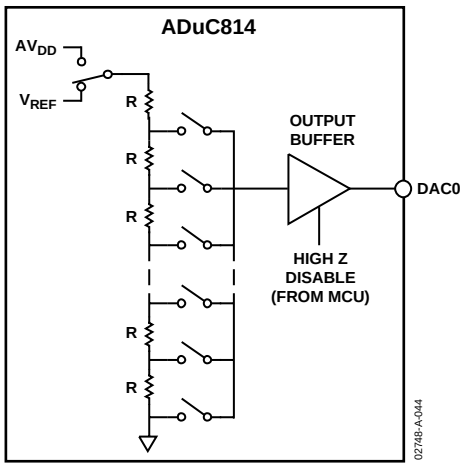

Figure 38. Resistor String DAC Functional Equivalent

As illustrated in Figure 38, the reference source for each DAC is user selectable in software. It can be either AV_{DD} or V_{REF}. In 0 V-to-AV_{DD} mode, the DAC output transfer function spans from 0 V to the voltage at the AV_{DD} pin. In 0 V-to-V_{REF} mode, the DAC output transfer function spans from 0 V to the internal V_{REF}, or if an external reference is applied, the voltage at the V_{REF} pin. The DAC output buffer features a true rail-to-rail output stage implementation. This means that, unloaded, each output is capable of swinging to within less than 100 mV of both AV_{DD} and ground. Moreover, the DAC's linearity specification (when driving a 10 kΩ resistive load to ground) is guaranteed through the full transfer function except Codes 0 to 48, and, in 0 V-to-AV_{DD} mode only, Codes 3945 to 4095. Linearity degradation near ground and V_{DD} is caused by saturation of the output buffer, and a general representation of its effects (neglecting offset and gain error) is illustrated in Figure 39. The dotted line in Figure 39 indicates the ideal transfer function, and the solid line represents what the transfer function might look like with endpoint nonlinearities due to saturation of the output buffer. Note that Figure 39 represents a transfer function in 0 V-to-V_{DD} mode only. In 0 V-to-V_{REF} mode (with $V_{REF} < V_{DD}$), the lower nonlinearity would be similar, but the upper portion of the transfer function would follow the ideal line right to the end (V_{REF} in this case, not V_{DD}), showing no signs of upper endpoint linearity error.

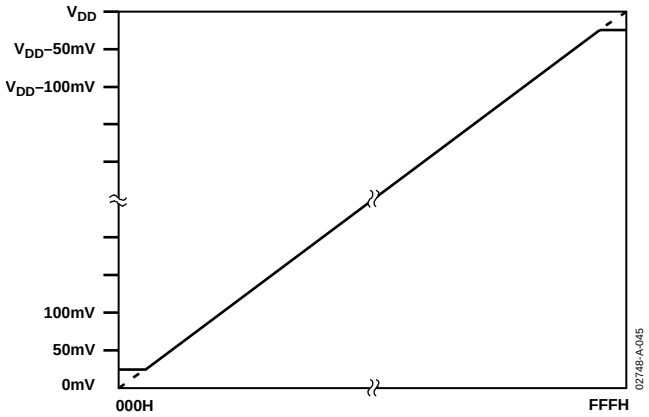

Figure 39. Endpoint Nonlinearities Due to Amplifier Saturation

The endpoint nonlinearities conceptually illustrated in Figure 39 get worse as a function of output loading. Most ADuC814 specifications assume a 10 kΩ resistive load to ground at the DAC output. As the output is forced to source or sink more current, the nonlinear regions at the top or bottom (respectively) of Figure 39 become larger. With larger current demands, this can significantly limit output voltage swing. Figure 40 and Figure 41 illustrate this behavior. Note that the upper trace in each of these figures is valid only for an output range selection of 0 V-to-AV_{DD}. In 0 V-to-V_{REF} mode, DAC loading does not cause high-side voltage drops as long as the reference voltage remains below the upper trace in the corresponding figure. For example, if AV_{DD} = 3 V and V_{REF} = 2.5 V, the high-side voltage is not affected by loads less than 5 mA. But around 7 mA, the upper curve in Figure 41 drops below 2.5 V (V_{REF}), indicating that at these higher currents the output cannot reach V_{REF}.

ON-CHIP PLL

The ADuC814 is intended for use with a 32.768 kHz watch crystal. An on-board PLL locks onto a multiple (512) of this 32.768kHz frequency to provide a stable 16.777216 MHz clock for the system. The core can operate at this frequency or at binary submultiples of it to allow power saving in cases where maximum core performance is not required. The default core clock is the PLL clock divided by 8 ($2^{CD} = 2^3$) or 2.097152 MHz. The PLL is controlled via the PLLCON special function register.

PLLCON	**PLL Control Register**
SFR Address	D7H
Power-On Default	03H
Bit Addressable	No

OSC_PD	LOCK	---	---	FINT	CD2	CD1	CD0

Table 13. PLLCON SFR Bit Designations

Bit No.	Name	Description			
7	OSC_PD	Oscillator Power-Down Bit.			
		Set by the user to halt the 32 kHz oscillator in power-down mode.			
		Cleared by the user to enable the 32 kHz oscillator in power-down mode. This feature allows the oscillator to continue clocking the TIC even in power-down mode.			
6	LOCK	PLL Lock Bit. This is a read-only bit.			
		Set automatically at power-on to indicate that the PLL loop is correctly tracking the crystal clock. If the external crystal becomes subsequently disconnected, the PLL rails and the core halts.			
		Cleared automatically at power-on to indicate that the PLL is not correctly tracking the crystal clock. This may be due to the absence of a crystal clock or an external crystal at power-on. In this mode, the PLL output is 16.78 MHz ± 20%.			
5	---	Reserved. Should be written with 0.			
4	---	Reserved. Should be written with 0.			
3	FINT	Fast Interrupt Response Bit.			
		Set by the user to enable the response to any interrupt to be executed at the fastest core clock frequency, regardless of the configuration of the CD2–CD0 bits (see below). Once user code has returned from an interrupt, the core resumes code execution at the core clock selected by the CD2–CD0 bits.			
		Cleared by the user to disable the fast interrupt response feature.			
2	CD2	CPU (Core Clock) Divider Bits.			
1	CD1	This number determines the frequency at which the microcontroller core operates.			
0	CD0	CD2	CD1	CD0	Core Clock Frequency (MHz)
		0	0	0	16.777216
		0	0	1	8.388608
		0	1	0	4.194304
		0	1	1	2.097152 (Default Core Clock Frequency)
		1	0	0	1.048576
		1	0	1	0.524288
		1	1	0	0.262144
		1	1	1	0.131072

TIME INTERVAL COUNTER (TIC)

A time interval counter is provided on-chip for counting longer intervals than the standard 8051 compatible timers are capable of. The TIC is capable of time-out intervals ranging from 1/128th second to 255 hours. Furthermore, this counter is clocked by the crystal oscillator rather than by the PLL and thus has the ability to remain active in power-down mode and to time long power-down intervals. This has obvious applications for remote battery-powered sensors where regular, widely spaced readings are required.

Six SFRs are associated with the time interval counter, TIMECON being its control register. Depending on the configuration of the IT0 and IT1 bits in TIMECON, the selected time counter register overflow clocks the interval counter. When this counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) is set and generates an interrupt if enabled. (See IEIP2 SFR description under the Interrupt System section.) If the ADuC814 is in power-down mode, again with TIC interrupt enabled, the TII bit wakes up the device and resumes code execution by vectoring directly to the TIC interrupt service vector address at 0053H. The TIC-related SFRs are described in Table 14. Note that the time based SFRs can be written initially with the current time; the TIC can then be controlled and accessed by the user software. In effect, this facilitates the implementation of a real-time clock. A block diagram of the TIC is shown in Figure 43.

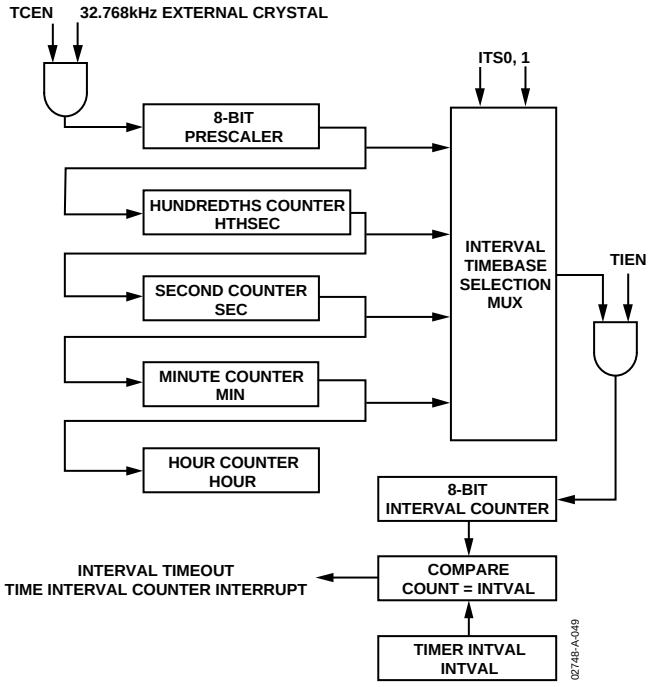

Figure 43. Time Interval Counter, Simplified Block Diagram

TIMECON **TIC CONTROL REGISTER**

SFR Address A1H
Power-On Default 00H
Bit Addressable No

---	TFH	ITS1	ITS0	STI	TII	TIEN	TCEN

Table 14. TIMECON SFR Bit Designations

Bit No.	Name	Description
7	---	Reserved.

6	TFH	Twenty-Four Hour Select Bit.
		Set by the user to enable the HOUR counter to count from 0 to 23.
		Cleared by the user to enable the HOUR counter to count from 0 to 255.
		The time interval counter continues to count after a reset when in hours/min/sec mode. If the part is in 24 hour mode though, this bit is reset and the part now counts in 255 hour mode. The following code segment can be used to set the TIC back into 24 hour mode after a RESET event.
		`MOV A,TIMECON ;Move contents of TIMECON into ACC`
		`RRC A ;Rotate ACC right by 1 place into Carry`
		`JNC NOTSET ;If CARRY bit is ! = 1 jump to NOTSET, else continue with next line`
		`ORL TIMECON,#01000000B`
		`;If CARRY bit = 1 for last line, then logical OR TIMECON with 40H`
		`NOTSE: ;continuation of normal code from here`

	ITS1	Interval Timebase Selection Bits.
4	ITS0	Written by the user to determine the interval counter update rate. ITS1 ITS0 Interval Timebase 0 0 1/128 Second 0 1 Seconds 1 0 Minutes 1 1 Hours
3	STI	Single Time Interval Bit. Set by the user to generate a single interval timeout. If set, a timeout clears the TIEN bit. Cleared by the user to allow the interval counter to be automatically reloaded and start counting again at each interval timeout.
2	TII	TIC Interrupt Bit. Set when the 8-bit interval counter matches the value in the INTVAL SFR. Cleared by the user software.
1	TIEN	Time Interval Enable Bit. Set by the user to enable the 8-bit time interval counter. Cleared by the user to disable and clear the contents of the interval counter.
0	TCEN	Time Clock Enable Bit. Set by the user to enable the time clock to the time interval counters. Cleared by the user to disable the clock to the time interval counters and clear the time interval SFRs. The time registers (HTHSEC, SEC, MIN and HOUR) can be written while TCEN is low.

WATCHDOG TIMER

The purpose of the watchdog timer is to generate a device reset or interrupt within a reasonable amount of time if the ADuC814 enters an erroneous state, possibly due to a programming error, electrical noise, or RFI. The watchdog function can be disabled by clearing the WDE (watchdog enable) bit in the watchdog control (WDCON) SFR. When enabled, the watchdog circuit generates a system reset or interrupt (WDS) if the user program fails to set the watchdog (WDE) bit within a predetermined amount of time (see PRE3–0 bits in WDCON). The watchdog timer itself is a 16-bit counter that is clocked at 32.768 kHz. The watchdog timeout interval can be adjusted via the PRE3–0 bits in WDCON. Full control and status of the watchdog timer function can be controlled via the watchdog timer control SFR (WDCON). The WDCON SFR can be written only by the user software if the double write sequence (WDWR) described in Table 15 is initiated on every write access to the WDCON SFR.

WDCON	**Watchdog Timer Control Register**
SFR Address	C0H
Power-On Default	10H
Bit Addressable	Yes

PRE3	PRE2	PRE1	PRE0	WDIR	WDS	WDE	WDWR

Table 15. WDCON SFR Bit Designation

Bit No.	Name	Description
7	PRE3	Watchdog Timer Prescale Bits.
6	PRE2	The watchdog timeout period is given by the equation
5	PRE1	$t_{WD} = (2^{PRE} \times (2^9/f_{PLL}))$
		where f_{PLL} = 32.768 kHz and PRE is defined as follows:
4	PRE0	PRE3 PRE2 PRE1 PRE0 Timeout Period (ms) Action
		0 0 0 0 15.6 Reset or Interrupt
		0 0 0 1 31.2 Reset or Interrupt
		0 0 1 0 62.5 Reset or Interrupt
		0 0 1 1 125 Reset or Interrupt
		0 1 0 0 250 Reset or Interrupt
		0 1 0 1 500 Reset or Interrupt
		0 1 1 0 1000 Reset or Interrupt
		0 1 1 1 2000 Reset or Interrupt
		1 0 0 0 0.0 Immediate Reset
		PRE3–0 > 1001 Reserved
3	WDIR	Watchdog Interrupt Request.
		If this bit is set by the user, the watchdog generates an interrupt response instead of a system reset when the watchdog timeout period has expired. This interrupt is not disabled by the CLR EA instruction and it is also a fixed, high-priority interrupt.
		If the watchdog is not being used to monitor the system, it can alternatively be used as a timer. The prescaler is used to set the timeout period in which an interrupt is generated. (See Table 33, Note 1, in the Interrupt System section.)
2	WDS	Watchdog Status Bit.
		Set by the watchdog controller to indicate that a watchdog timeout has occurred.
		Cleared by writing a 0 or by an external hardware reset. It is not cleared by a watchdog reset.
1	WDE	Watchdog Enable Bit.
		Set by the user to enable the watchdog and clear its counters. If this bit is not set by the user within the watchdog timeout period, the watchdog generates a reset or interrupt, depending on WDIR.
		Cleared under the following conditions: User writes 0, Watchdog Reset (WDIR = 0); Hardware Reset; PSM Interrupt.
0	WDWR	Watchdog Write Enable Bit.
		To write data into the WDCON SFR involves a double instruction sequence. The WDWR bit must be set and followed immediately by a write instruction to the WDCON SFR. For example:

```
CLR EA           ; disable interrupts while writing to WDT
SETB WDWR        ; allow write to WDCON
MOV WDCON, #72H  ; enable WDT for 2.0s timeout
SET B EA         ; enable interrupts again (if rqd)
```

POWER SUPPLY MONITOR

As its name suggests, the power supply monitor, once enabled, monitors the supply (DV_{DD}) on the ADuC814. It indicates when any of the supply pins drop below one of four user-selectable voltage trip points from 2.63 V to 4.63 V. For correct operation of the power supply monitor function, DV_{DD} must be equal to or greater than 2.7 V. Monitor function is controlled via the PSMCON SFR. If enabled via the IEIP2 SFR, the monitor interrupts the core using the PSMI bit in the PSMCON SFR. This bit is not cleared until the failing power supply has returned above the trip point for at least 250 ms. This monitor function allows the user to save working registers to avoid possible data loss due to the low supply condition, and also ensures that normal code execution does not resume until a safe supply level is well established. The supply monitor is also protected against spurious glitches triggering the interrupt circuit.

PSMCON	**Power Supply Monitor Control Register**
SFR Address	DFH
Power-On Default	DEH
Bit Addressable	No

----	CMPD	PSMI	TPD1	TPD0	----	----	PSMEN

Table 16. PSMCON SFR Bit Designations

Bit No.	Name	Description		
7	PSMCON.7	Reserved.		
6	CMPD	DV_{DD} Comparator Bit.		
		This is a read-only bit and directly reflects the state of the DV_{DD} comparator.		
		Read 1 indicates that the DV_{DD} supply is above its selected trip point.		
		Read 0 indicates that the DV_{DD} supply is below its selected trip point.		
5	PSMI	Power Supply Monitor Interrupt Bit.		
		This bit is set high by the MicroConverter if CMPD is low, indicating low digital supply. The PSMI bit can be used to interrupt the processor. Once CMPD returns and remains high, a 250 ms counter is started. When this counter times out, the PSMI interrupt is cleared. PSMI can also be written by the user; however, if the comparator output is low, it is not possible for the user to clear PSMI.		
4	TPD1	DV_{DD} Trip Point Selection Bits.		
3	TPD0	These bits select the DV_{DD} trip-point voltage as follows:		
		TPD1	TPD0	Selected DV_{DD} Trip Point (V)
		0	0	4.63
		0	1	3.08
		1	0	2.93
		1	1	2.63
2	PSMCON.2	Reserved.		
1	PSMCON.1	Reserved.		
0	PSMEN	Power Supply Monitor Enable Bit.		
		Set to 1 by the user to enable the power supply monitor circuit.		
		Cleared to 0 by the user to disable the power supply monitor circuit.		

Bit No.	Name	Description		
2	CPHA[1]	Clock Phase Select Bit.		
		Set by the user if the leading SCLOCK edge is to transmit data.		
		Cleared by the user if the trailing SCLOCK edge is to transmit data.		
1	SPR1	SPI Bit Rate Select Bits.		
0	SPR0	These bits select the SCLOCK rate (bit rate) in master mode as follows:		
		SPR1	SPR0	Selected Bit Rate
		0	0	$f_{CORE}/2$
		0	1	$f_{CORE}/4$
		1	0	$f_{CORE}/8$
		1	1	fcore/16
		In SPI slave mode,where SPIM = 0, the logic level on the external $\overline{SS}$ pin (Pin 22), can be read via the SPR0 bit.		

[1]The CPOL and CPHA bits should both contain the same values for master and slave devices.

SPIDAT	**SPI Data Register**
Function	The SPIDAT SFR is written by the user to transmit data over the SPI interface or read by the user code to read data just received by the SPI interface.
SFR Address	F7H
Power-On Default	00H
Bit Addressable	No

Using the SPI Interface

Depending on the configuration of the bits in the SPICON SFR shown in Table 18, the ADuC814 SPI interface transmits or receives data in a number of possible modes. Figure 44 shows all possible ADuC814 SPI configurations and the timing relationships and synchronization between the signals involved.

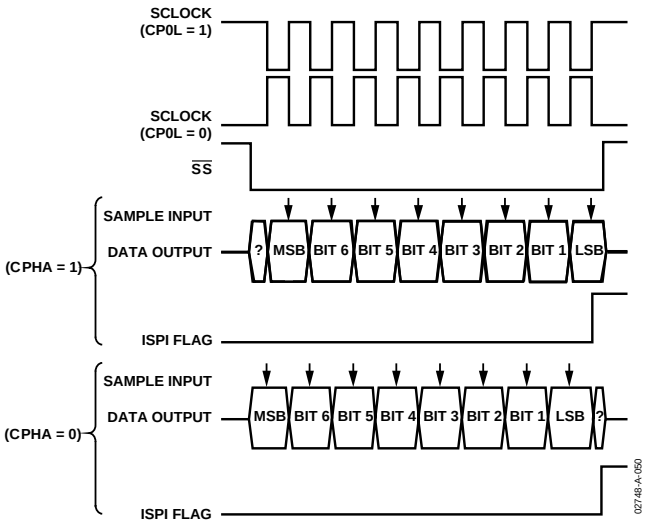

Figure 44. ADuC814, SPI Timing, All Modes

SPI Interface—Master Mode

In master mode, the SCLOCK pin is always an output and generates a burst of eight clocks whenever user code writes to the SPIDAT register. The SCLOCK bit rate is determined by SPR0 and SPR1 in SPICON. It should also be noted that the $\overline{SS}$ pin is not used in master mode. If the ADuC814 needs to assert the $\overline{SS}$ pin on an external slave device, a port digital output pin should be used. In master mode, a byte transmission or reception is initiated by a write to SPIDAT. Eight clock periods are generated via the SCLOCK pin and the SPIDAT byte being transmitted via MOSI. With each SCLOCK period, a data bit is also sampled via MISO. After eight clocks, the byte is completely transmitted, and the input byte is waiting in the input shift register. The ISPI flag is set automatically and an interrupt occurs if enabled. The value in the shift register is latched into SPIDAT.

SPI Interface—Slave Mode

In slave mode, the SCLOCK is an input. The $\overline{SS}$ pin must also be driven low externally during the byte communication. Transmission is also initiated by a write to SPIDAT. In slave mode, a data bit is transmitted via MISO, and a data bit is received via MOSI on each input SCLOCK. After eight clocks, the byte is completely transmitted and the input byte is waiting in the input shift register. The ISPI flag is set automatically and an interrupt occurs if enabled. The value in the shift register is latched into SPIDAT only when the transmission/reception of a byte is complete. The end of transmission occurs after the eighth clock is received, if CPHA = 1, or when $\overline{SS}$ returns high if CPHA = 0.

T2CON **Timer/Counter 2 Control Register**
SFR Address C8H
Power-On Default 00H
Bit Addressable Yes

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CNT2	CAP2

Table 24. T2CON SFR Bit Designations

Bit No.	Name	Description
7	TF2	Timer 2 Overflow Flag. Set by hardware on a Timer 2 overflow. TF2 is not set when either RCLK or TCLK = 1. Cleared by the user software.
6	EXF2	Timer 2 External Flag. Set by hardware when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. Cleared by the user software.
5	RCLK	Receive Clock Enable. Set by the user to enable the serial port to use Timer 2 overflow pulses for its receive clock in serial port in Modes 1 and 3. Cleared by the user to enable Timer 1 overflow to be used for the receive clock.
4	TCLK	Transmit Clock Enable Bit. Set by the user to enable the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. Cleared by the user to enable Timer 1 overflow to be used for the transmit clock.
3	EXEN2	Timer 2 External Enable Flag. Set by the user to enable a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. Cleared by the user for Timer 2 to ignore events at T2EX.
2	TR2	Timer 2 Start/Stop Control Bit. Set by the user to start Timer 2. Cleared by the user to stop Timer 2.
1	CNT2	Timer 2 timer or counter function select bit. Set by the user to select counter function (input from external T2 pin). Cleared by the user to select timer function (input from on-chip core clock).
0	CAP2	Timer 2 Capture/Reload Select Bit. Set by the user to enable captures on negative transitions at T2EX if EXEN2 = 1. Cleared by the user to enable autoreloads with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to autoreload on Timer 2 overflow.

Timer/Counter 2 Data Registers

Timer/Counter 2 also has two pairs of 8-bit data registers associated with it. These are used as both timer data registers and timer capture/reload registers.

TH2 and TL2 Timer 2, data high byte and low byte.
SFR Address CDH, CCH, respectively

RCAP2H and RCAP2L Timer 2, Capture/Reload byte and low byte.
SFR Address CBH, CAH, respectively

TIMER/COUNTER 2 OPERATING MODES

This section describes the operating modes for Timer/Counter 2. The operating modes are selected by bits in the T2CON SFR as shown in Table 27.

Table 25. Mode Selection in T2CON

RCLK (or) TCLK	CAP2	TR2	MODE
0	0	1	16-Bit Autoreload
0	1	1	16-Bit Capture
1	X	1	Baud Rate
X	X	0	OFF

16-Bit Autoreload Mode

In autoreload mode, there are two options that are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then when Timer 2 rolls over, it not only sets TF2 but also causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1, then Timer 2 still performs the above, but with the added feature that a 1-to-0 transition at external input T2EX also triggers the 16-bit reload and sets EXF2. The autoreload mode is illustrated in Figure 49.

16-Bit Capture Mode

In the capture mode, there are again two options that are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which, upon overflowing, sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, then Timer 2 still performs the above, but a 1-to-0 transition on external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt. Capture mode is illustrated in Figure 50.

The baud rate generator mode is selected by RCLK = 1 and/or TCLK = 1. In either case, if Timer 2 is being used to generate the baud rate, the TF2 interrupt flag does not occur. Therefore Timer 2 interrupts do not occur so they do not have to be disabled. In this mode, the EXF2 flag, however, can still cause interrupts; this can be used as a third external interrupt. Baud rate generation is described as part of the UART Serial Interface section that follows.

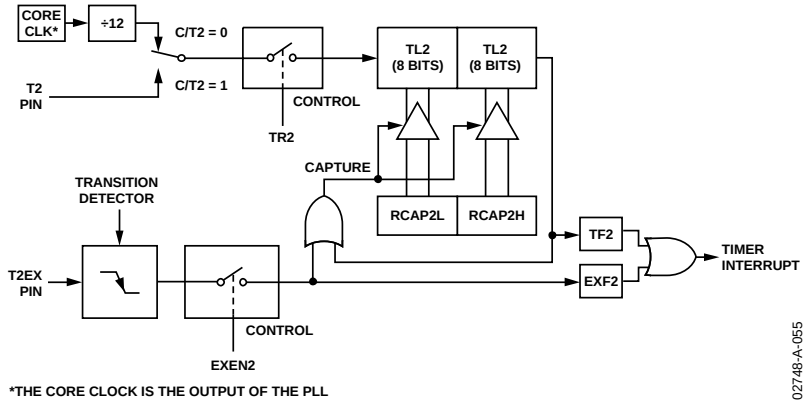

Figure 49. Timer/Counter 2, 16-Bit Autoreload Mode

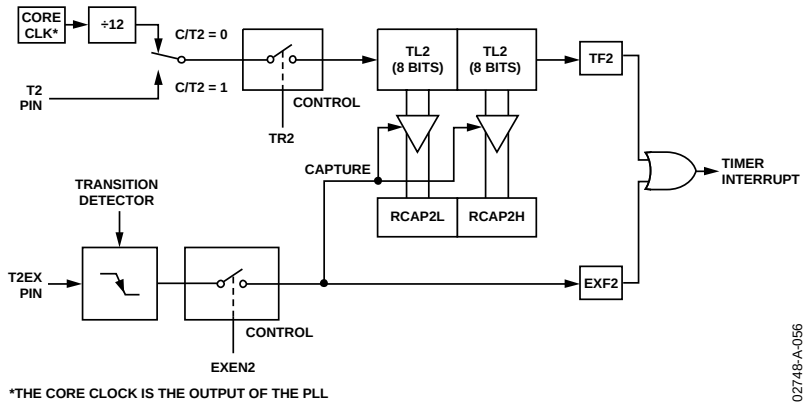

Figure 50. Timer/Counter 2, 16-Bit Capture Mode

UART SERIAL INTERFACE

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can begin receiving a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, the first byte is lost. The physical interface to the serial data network is via Pins RxD (P3.0) and TxD (P3.1), while the SFR interface to the UART is comprised of the following registers.

SBUF

The serial port receive and transmit registers are both accessed through the SBUF SFR (SFR address = 99H). Writing to SBUF loads the transmit register and reading SBUF accesses a physically separate receive register.

SCON	**UART Serial Port Control Register**
SFR Address	98H
Power-On Default	00H
Bit Addressable	Yes

SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Table 26. SCON SFR Bit Designations

Bit No.	Name	Description
7	SM0	UART Serial Mode Select Bits.
6	SM1	These bits select the serial port operating mode as follows: SM0 SM1 Selected Operating Mode 0 0 Mode 0: Shift Register, fixed baud rate (Core_Clk/2) 0 1 Mode 1: 8-bit UART, variable baud rate 1 0 Mode 2: 9-bit UART, fixed baud rate (Core_Clk/64) or (Core_Clk/32) 1 1 Mode 3: 9-bit UART, variable baud rate
5	SM2	Multiprocessor Communication Enable Bit. Enables multiprocessor communication in Modes 2 and 3. In Mode 0, SM2 should be cleared. In Mode 1, if SM2 is set, RI is not activated if a valid stop bit is not received. If SM2 is cleared, RI is set as soon as the byte of data is received. In Mode 2 or 3, if SM2 is set, RI is not activated if the received ninth data bit in RB8 is 0. If SM2 is cleared, RI is set as soon as the byte of data is received.
4	REN	Serial Port Receive Enable Bit. Set by the user software to enable serial port reception. Cleared by the user software to disable serial port reception.
3	TB8	Serial Port Transmit (Bit 9). The data loaded into TB8 is the ninth data bit that is transmitted in Modes 2 and 3.
2	RB8	Serial port Receiver Bit 9. The ninth data bit received in Modes 2 and 3 is latched into RB8. For Mode 1, the stop bit is latched into RB8.
1	TI	Set by hardware at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in Modes 1, 2, and 3. Cleared by the user software.
0	RI	Serial Port Receive Interrupt Flag. Set by hardware at the end of the eighth bit in Mode 0, or halfway through the stop bit in Modes 1, 2, and 3. Cleared by user software.

IP **Interrupt Priority Register**
SFR Address B8H
Power-On Default 00H
Bit Addressable Yes

---	PADC	PT2	PS	PT1	PX1	PT0	PX0

Table 30. IP SFR Bit Designations

Bit No.	Name	Description
7	---	Reserved.
6	PADC	ADC Interrupt Priority. Written to by user to set interrupt priority level (1 = High; 0 = Low).
5	PT2	Timer 2 Interrupt Priority. Written to by the user to set interrupt priority level (1 = High; 0 = Low).
4	PS	UART Serial Port Interrupt Priority. Written to by the user to set interrupt priority level (1 = High; 0 = Low).
3	PT1	Timer 1 Interrupt Priority. Written to by the user to set interrupt priority level (1 = High; 0 = Low).
2	PX1	External Interrupt 1 Priority (INT1). Written to by the user to set interrupt priority level (1 = High; 0 = Low).
1	PT0	Timer 0 Interrupt Priority. Written to by the user to set interrupt priority level (1 = High; 0 = Low).
0	PX0	External Interrupt 0 Priority (INT0). Written to by the user to set interrupt priority level (1 = High; 0 = Low).

IEIP2 **Secondary Interrupt Enable and Priority Register**
SFR Address A9H
Power-On Default A0H
Bit Addressable No

---	PT1	PPSM	PSI	---	ETI	EPSM	ESI

Table 31. IEIP2 SFR Bit Designations

Bit No.	Name	Description
7	---	Reserved.
6	PTI	Time Interval Counter Interrupt Priority. Written to by the user to set TIC interrupt priority (1 = High; 0 = Low).
5	PPSM	PSM Interrupt Priority. Written to by the user to select power supply monitor interrupt priority (1 = High; 0 = Low).
4	PSI	SPI Serial Port Interrupt Priority. Written to by the user to select SPI serial port interrupt priority (1 = High; 0 = Low).
3	---	Reserved. This bit must be 0.
2	ETI	TIC Interrupt. Set by the user to enable the TIC interrupt. Cleared by the user to disable the TIC interrupt.
1	EPSM	Power Supply Monitor Interrupt. Set by the user to enable the power supply monitor interrupt. Cleared by the user to disable the power supply monitor interrupt.
0	ESI	SPI Serial Port Interrupt. Set by the user to enable the SPI serial port interrupt. Cleared by the user to disable the SPI serial port interrupt.

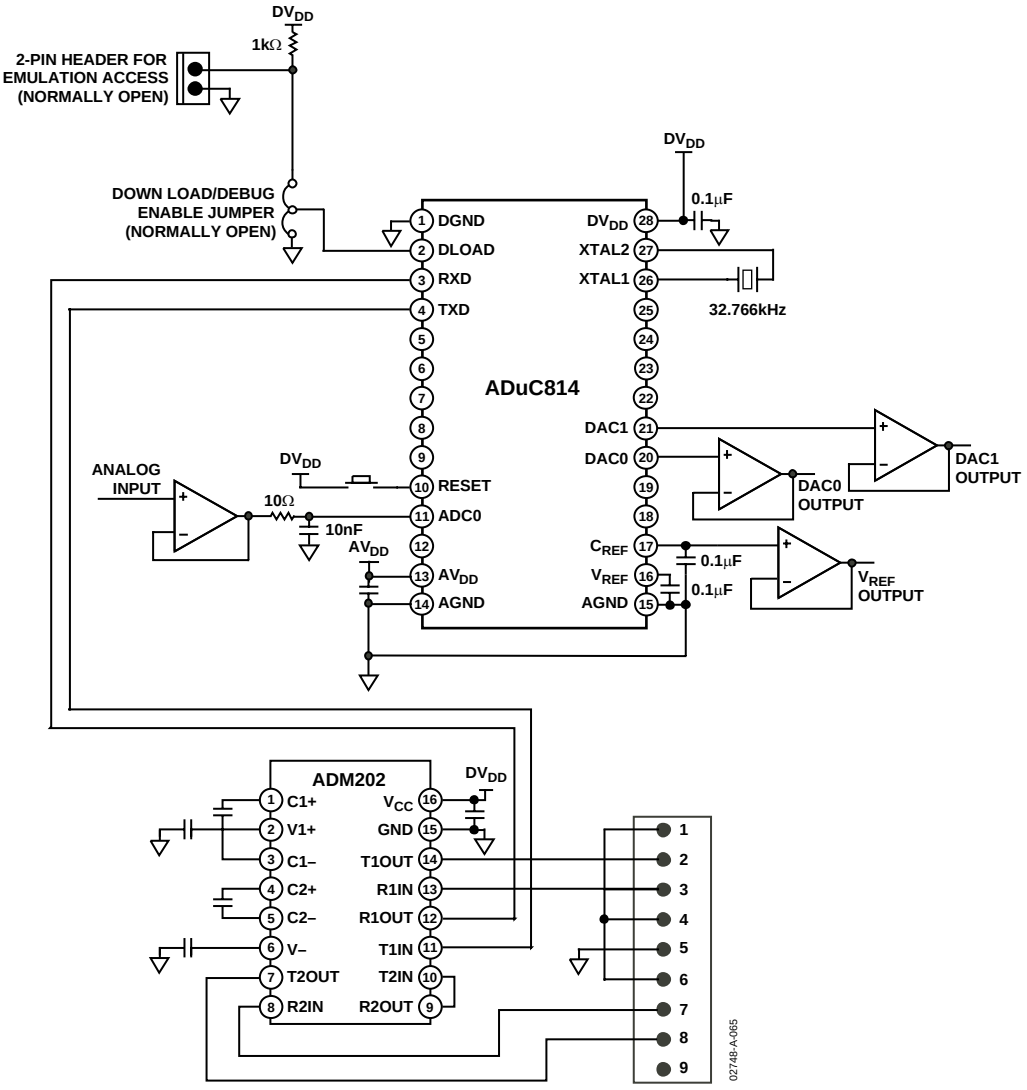

Figure 59. Typical ADuC814 System Connection Diagram

Single-Pin Emulation Mode

Also built into the ADuC814 is a dedicated controller for single-pin in-circuit emulation (ICE) using standard production ADuC814 devices. In this mode, emulation access is gained by connection to a single pin, again the DLOAD pin is used for this function. As described previously, this pin is either high to enable entry into serial download and serial debug modes or low to select normal code execution. To enable single-pin emulation mode, however, users need to pull the DLOAD pin high through a 1 kΩ resistor. The emulator then connects to the 2-pin header. To be compatible with the standard connector that comes with the single-pin emulator available from Accutron Limited (www.accutron.com), use a 2-pin 0.1-inch pitch friction lock header from Molex (www.molex.com) such as their part number 22-27-2021. Be sure to observe the polarity of this header. When the friction lock tab is at the right, the ground pin should be the lower of the two pins (when viewed from the top).

TIMING SPECIFICATIONS[1,2,3]

Table 34. Clock Input (External Clock Driven XTAL1)

AV_{DD} = 2.7 V to 3.3 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.3 V or 4.75 V to 5.25 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted

		32.768 kHz External Crystal			
Parameter		**Min**	**Typ**	**Max**	**Unit**
t_{CK}	XTAL1 Period		30.52		µs
t_{CKL}	XTAL1 Width Low		15.16		µs
t_{CKH}	XTAL1 Width High		15.16		µs
t_{CKR}	XTAL1 Rise Time		20		ns
t_{CKF}	XTAL1 Fall Time		20		ns
$1/t_{CORE}$	ADuC814 Core Clock Frequency[4]	0.131		16.78	MHz
t_{CORE}	ADuC814 Core Clock Period[5]		0.476		µs
t_{CYC}	ADuC814 Machine Cycle Time[6]	0.72	5.7	91.55	µs

[1] AC inputs during testing are driven at DV_{DD} – 0.5 V for a Logic 1, and at 0.45 V for a Logic 0. Timing measurements are made at V_{IH} min for a Logic 1, and at V_{IL} max for a Logic 0 as shown in Figure 61.
[2] For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs as shown in Figure 61.
[3] C_{LOAD} for all outputs = 80 pF, unless otherwise noted.
[4] ADuC814 internal PLL locks onto a multiple (512 times) the external crystal frequency of 32.768 kHz to provide a stable 16.777216 MHz internal clock for the system. The core can operate at this frequency or at a binary submultiple called Core_Clk, selected via the PLLCON SFR.
[5] This number is measured at the default Core_Clk operating frequency of 2.09 MHz.
[6] ADuC814 Machine Cycle Time is nominally defined as 12/Core_CLK.

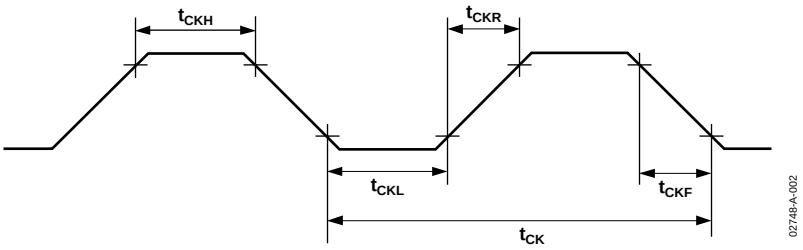

Figure 60. XTAL1 Input

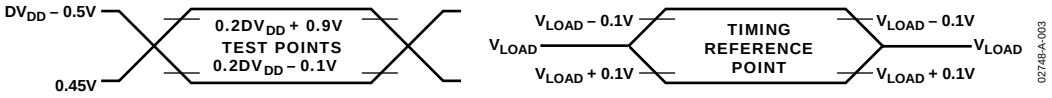

Figure 61. Timing Waveform Characteristics

Table 38. SPI Slave Mode Timing (CPHA = 1)

Parameter		Min	Typ	Max	Unit
t_{SS}	$\overline{SS}$ to SCLOCK Edge	0			ns
t_{SL}	SCLOCK Low Pulse Width		330		ns
t_{SH}	SCLOCK High Pulse Width		330		ns
t_{DAV}	Data Output Valid after SCLOCK Edge			50	ns
t_{DSU}	Data Input Setup Time before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time after SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns
t_{SFS}	$\overline{SS}$ High after SCLOCK Edge	0			ns

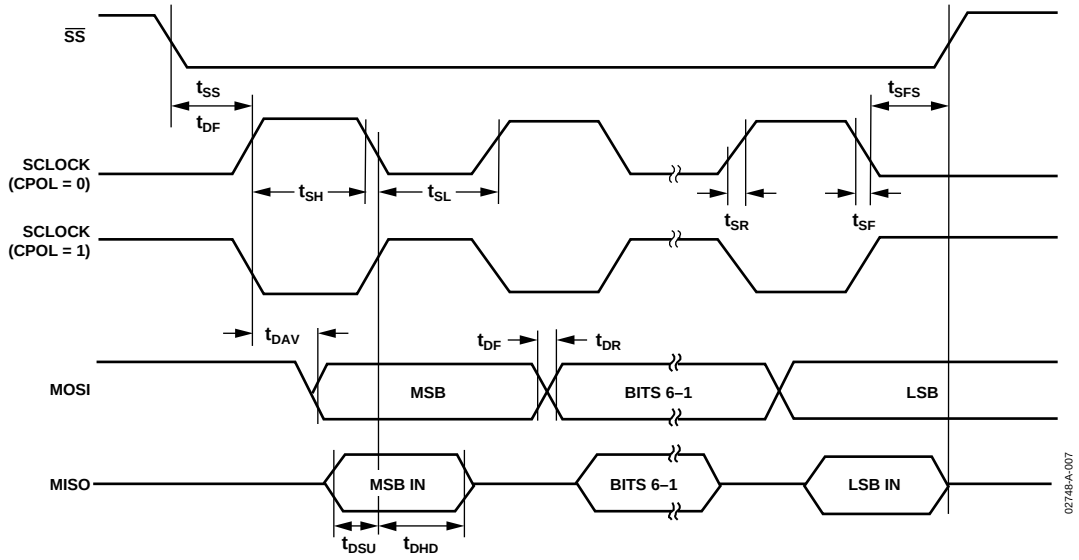

Figure 65. SPI Slave Mode Timing (CPHA = 1)

OUTLINE DIMENSIONS

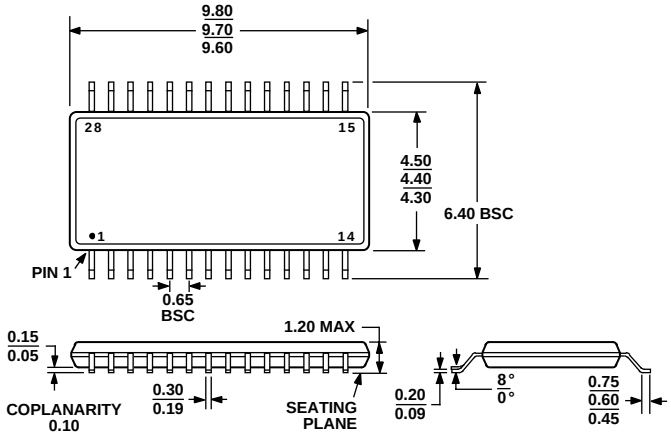

Figure 67. 28-Lead Thin Shrink Small Outline Package (TSSOP) (RU-28)
Dimensions shown in mm

NOTES

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