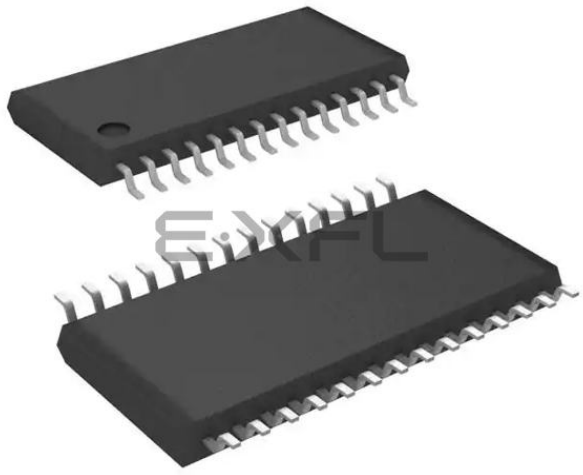

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8052
Core Size	8-Bit
Speed	16.78MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PSM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 6x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	28-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc814bru

ADUC814* PRODUCT PAGE QUICK LINKS

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- ADuC814 QuickStart Development System

DOCUMENTATION

Application Notes

- AN-1074: Understanding the Serial Download Protocol (Formerly uC004)
- AN-282: Fundamentals of Sampled Data Systems
- AN-660: XY-Matrix Keypad Interface to MicroConverter®
- AN-661: ADuC814 to ADM1032 via I²C® Interface
- AN-709: RTD Interfacing and Linearization Using an ADuC8xx MicroConverter®
- AN-759: Expanding the Number of DAC Outputs on the ADuC8xx and ADuC702x Families (uC012)
- UC-001: MicroConverter® I2C® Compatible Interface
- UC-006: A 4-wire UART-to-PC Interface
- UC-009: Addressing 16MB of External Data Memory
- UC-018: Uses of the Time Interval Counter

Data Sheet

- ADuC814: MicroConverter® , Small Package, 12-Bit ADC with Embedded Flash MCU Data Sheet
- ADuC814: Errata Sheet

User Guides

- ADuC814 Quick Reference Guide
- UG-041: ADuC8xx Evaluation Kit Getting Started User Guide

REFERENCE MATERIALS

Technical Articles

- Integrated Route Taken to Pulse Oximetry

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ABSOLUTE MAXIMUM RATINGS

Table 2. Temperature = 25°C, unless otherwise noted

Parameter	Rating
AV_{DD} to AGND	–0.3 V to +7 V
DV_{DD} to AGND	–0.3 V to +7 V
AV_{DD} to DV_{DD}	–0.3 V to +0.3 V
AGND to DGND[1]	–0.3 V to +0.3 V
Analog Input Voltage to AGND[2]	–0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND	–0.3 V to AV_{DD} + 0.3 V
Analog Input Current (Indefinite)	30 mA
Reference Input Current (Indefinite)	30 mA
Digital Input Voltage to DGND	–0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND	–0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	97.9°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] AGND and DGND are shorted internally on the ADuC814.
[2] Applies to Pins P1.2 to P1.7 operating in analog or digital input mode.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

ADC SPECIFICATIONS

Integral Nonlinearity

This is the maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point1/2 LSB below the first code transition and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

This is the deviation of the first code transition (0000 … 000) to (0000 … 001) from the ideal, i.e., +1/2 LSB.

Full-Scale Error

This is the deviation of the last code transition from the ideal AIN voltage (full-scale error has been adjusted out).

Signal-to-(Noise + Distortion) Ratio

This is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$\textit{Signal-to =- (Noise + Distortion)} = (6.02N + 1.76)$$

Thus, for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion (THD)

Total harmonic distortion is the ratio of the rms sum of the harmonics to the fundamental.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and including dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is the noise peak.

DAC SPECIFICATIONS

Relative Accuracy

Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero-scale error and full-scale error.

Voltage Output Settling Time

This is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

Digital-to-Analog Glitch Impulse

This is the amount of charge injected into the analog output when the inputs change state. It is specified as the area of the glitch in nV-sec.

TYPICAL PERFORMANCE CURVES

The typical performance plots presented in this section illustrate typical performance of the ADuC814 under various operating conditions. Note that all typical plots in this section were generated using the ADuC814BRU, i.e., the B-grade part.

Figure 3 and Figure 4 show typical ADC integral nonlinearity (INL) errors from ADC Code 0 to Code 4095 at 5 V and 3 V supplies, respectively. The ADC is using its internal reference (2.5 V) and operating at a sampling rate of 152 kHz. The typical worst-case errors in both plots are just less than 0.3 LSBs.

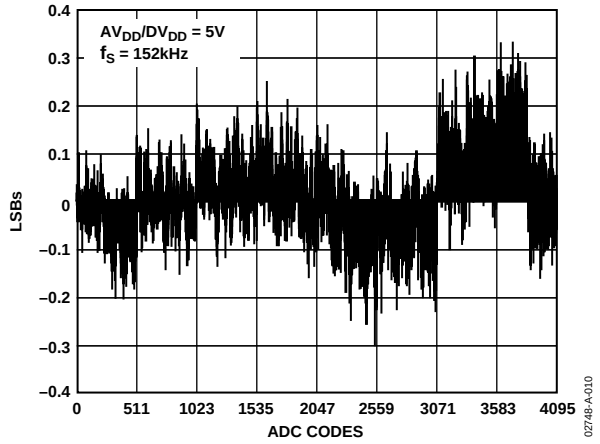

Figure 3. Typical INL Error, V_{DD} = 5 V

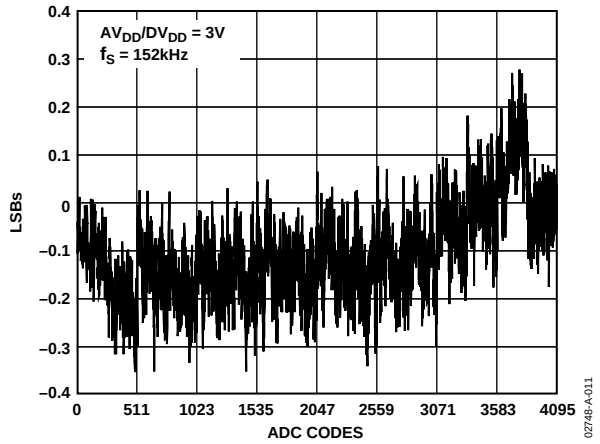

Figure 4. Typical INL Error, V_{DD} = 3 V

Figure 5 and Figure 6 show the variation in worst-case positive (WCP) INL and worst-case negative (WCN) INL versus external reference input voltage.

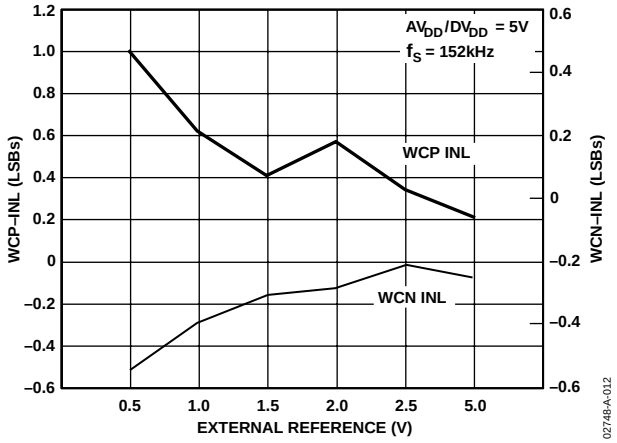

Figure 5. Typical Worst-Case INL Error vs. V_{REF}, V_{DD} = 5 V

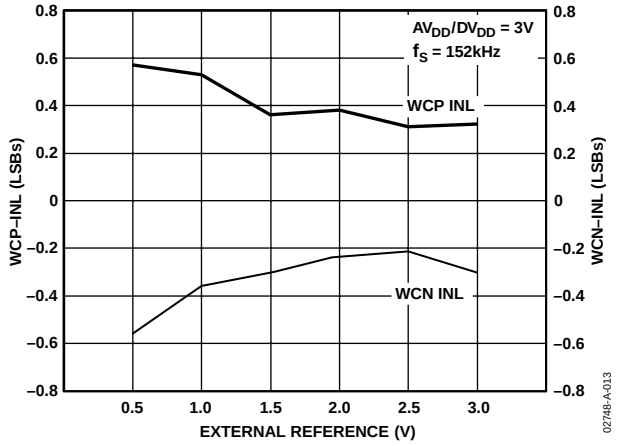

Figure 6. Typical Worst-Case INL Error vs. V_{REF}, V_{DD} = 3 V

Figure 7 and Figure 8 show typical ADC differential nonlinearity (DNL) errors from ADC Code 0 to Code 4095 at 5 V and 3 V supplies, respectively. The ADC is using its internal reference (2.5 V) and operating at a sampling rate of 152 kHz. The typical worst-case errors in both plots are just less than 0.2 LSBs.

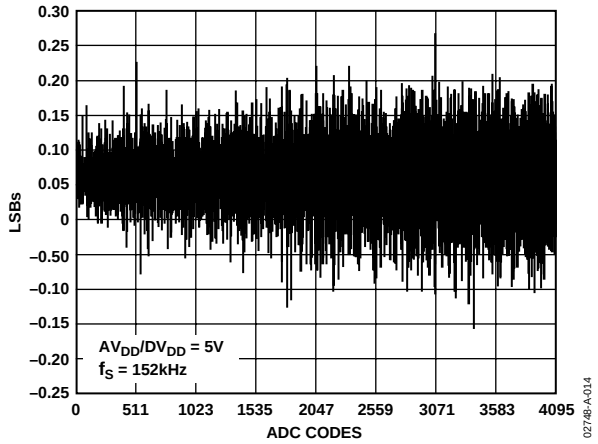

Figure 7. Typical DNL Error, V_{DD} = 5 V

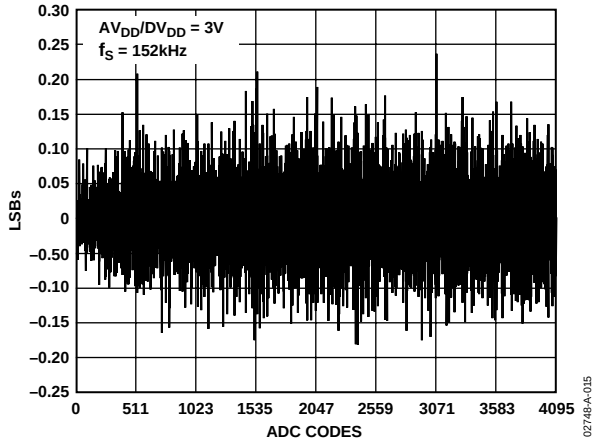

Figure 8. Typical DNL Error, V_{DD} = 3 V

Figure 9 and Figure 10 show the variation in worst-case positive (WCP) DNL and worst-case negative (WCN) DNL versus external reference input voltage.

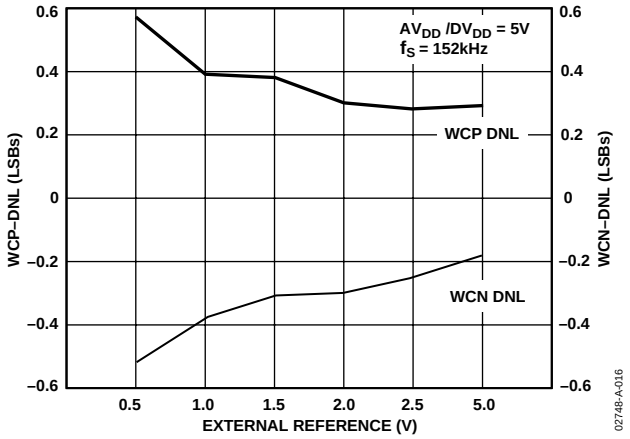

Figure 9. Typical Worst-Case DNL Error vs. V_{REF}, V_{DD} = 5 V

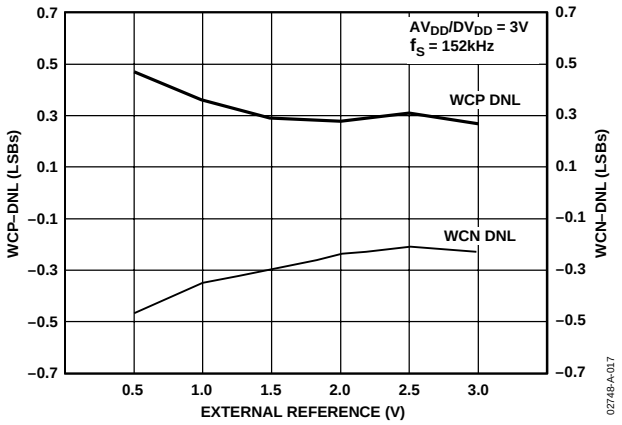

Figure 10. Typical Worst-Case DNL Error vs. V_{REF}, V_{DD} = 3 V

Figure 11 shows a histogram plot of 10,000 ADC conversion results on a dc input with V_{DD} = 5 V. The plot illustrates an excellent code distribution pointing to the low noise performance of the on-chip precision ADC.

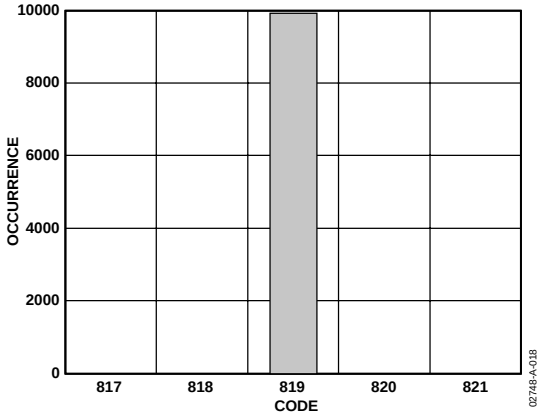

Figure 11. Code Histogram plot, V_{DD} = 5 V

Figure 12 shows a histogram plot of 10,000 ADC conversion results on a dc input for V_{DD} = 3 V. The plot again illustrates a very tight code distribution of 1 LSB with the majority of codes appearing in one output bin.

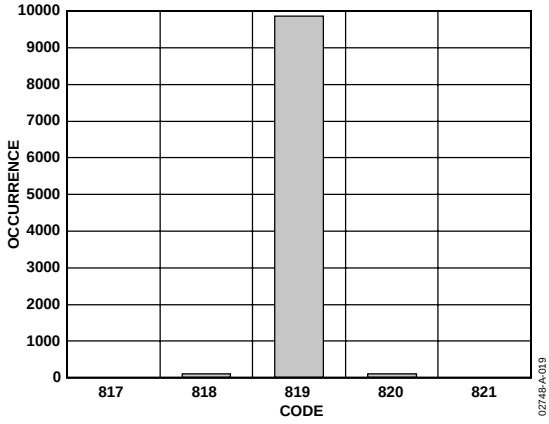

Figure 12. Code Histogram Plot, V_{DD} = 3 V

ADCCON2 (ADC CONTROL SFR 2)

The ADCCON2 (byte addressable) register controls ADC channel selection and conversion modes as detailed below.

SFR Address D8H
SFR Power-On Default 00H
Bit Addressable Yes

ADCI	ADCSPI	CCONV	SCOVC	CS3	CS2	CS1	CS0

Table 7. ADCCON2 SFR Bit Designations

Bit No.	Name	Description
7	ADCI	ADC Interrupt Bit. ADCI is set at the end of a single ADC conversion cycle. If the ADC interrupt is enabled, the ADCI bit is cleared when user code vectors to the ADC interrupt routine. Otherwise the ADCI bit should be cleared by the user code.
6	ADCSPI	ADCSPI Mode Enable Bit. ADCSPI is set to enable the ADC conversion results to be transferred directly to the SPI data buffer (SPIDAT) without intervention from the CPU.
5	CCONV	Continuous Conversion Bit. CCONV is set to initiate the ADC into a continuous mode of conversion. In this mode the ADC starts converting based on the timing and channel configuration already set up in the ADCCON SFRs. The ADC automatically starts another conversion once a previous conversion cycle has completed. When operating in this mode from 3 V supplies, the ADC should be configured for ADC clock divide of 16 using CK1 and CK0 bits in ADCCON1, and ADC acquisition time should be set to four ADC clocks using AQ1, AQ0 bits in ADCCON1 SFR.
4	SCONV	Single Conversion Bit. SCONV is set to initiate a single conversion cycle. The SCONV bit is automatically reset to 0 on completion of the single conversion cycle. When operating in this mode from 3 V supplies, the maximum ADC sampling rate should not exceed 147 kSPS.
3	CS3	Channel Selection Bits. CS3–CS0 allow the user to program the ADC channel selection under software control. Once a conversion is initiated, the channel converted is pointed to by these channel selection bits. The Channel Select bits operate as follows:
2	CS2	
1	CS1	
0	CS0	

CS3	CS2	CS1	CS0	CHANNEL	
0	0	0	0	0	
0	0	0	1	1	
0	0	1	0	2	
0	0	1	1	3	
0	1	0	0	4	
0	1	0	1	5	
0	1	1	0	X	Not a vaild selection. No ADC channel selected.
0	1	1	1	X	Not a valid selection. No ADC channel selected.
1	0	0	0	Temperature Sensor	
1	0	0	1	DAC0	
1	0	1	0	DAC1	
1	0	1	1	AGND	
1	1	0	0	V_{REF}	

NONVOLITILE FLASH/EE MEMORY

FLASH/EE MEMORY OVERVIEW

The ADuC814 incorporates Flash/EE memory technology on-chip to provide the user with nonvolatile, in-circuit reprogrammable code and data memory space.

Flash/EE memory takes the flexible in-circuit reprogrammable features of EEPROM and combines them with the space efficient/density features of EPROM (see Figure 32).

Because Flash/EE technology is based on a single transistor cell architecture, a Flash memory array such as EPROM can be implemented to achieve the space efficiencies or memory densities required by a given design.

Like EEPROM, flash memory can be programmed in-system at a byte level, although it must first be erased; the erase being performed in page blocks. Thus, flash memory is often and more correctly referred to as Flash/EE memory.

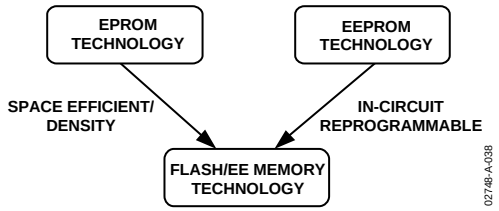

Figure 32. Flash/EE Memory Development

Incorporated in the ADuC814, Flash/EE memory technology allows the user to update program code space in-circuit without the need to replace one-time programmable (OTP) devices at remote operating nodes.

FLASH/EE MEMORY AND THE ADUC814

The ADuC814 provides two arrays of Flash/EE memory for user applications. There are 8 kbytes of Flash/EE program space provided on-chip to facilitate code execution, therefore removing the requirement for an external discrete ROM device. The program memory can be programmed using conventional third-party memory programmers. This array can also be programmed in-circuit, using the serial download mode provided.

A 640-byte Flash/EE data memory space is also provided on-chip. This may be used as a general-purpose nonvolatile scratchpad area. User access to this area is via a group of six SFRs. This space can be programmed at a byte level, although it must first be erased in 4-byte pages.

ADUC814 FLASH/EE MEMORY RELIABILITY

The Flash/EE program and data memory arrays on the ADuC814 are fully qualified for two key Flash/EE memory characteristics: Flash/EE memory cycling endurance and Flash/EE memory data retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many program, read, and erase cycles. In real terms, a single endurance cycle is composed of four independent, sequential events:

1. Initial page erase sequence
2. Read/verify sequence
3. Byte program sequence
4. Second read/verify sequence

In reliability qualification, every byte in both the program and data Flash/EE memory is cycled from 00H to FFH until a first fail is recorded signifying the endurance limit of the on-chip Flash/EE memory.

As indicated in the Specifications tables, the ADuC814 Flash/EE memory endurance qualification has been carried out in accordance with JEDEC Specification A117 over the industrial temperature range of –40°C to +125°C. The results allow the specification of a minimum endurance figure over supply and a temperature of 100,000 cycles, with an endurance figure of 700,000 cycles being typical of operation at 25°C.

Retention quantifies the ability of the Flash/EE memory to retain its programmed data over time. Again, the ADuC814 has been qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature (T_J = 55°C). As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit described above, before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its full specified retention lifetime every time the Flash/EE memory is reprogrammed. It should be noted that retention lifetime, based on an activation energy of 0.6 eV, derates with T_J as shown in Figure 33.

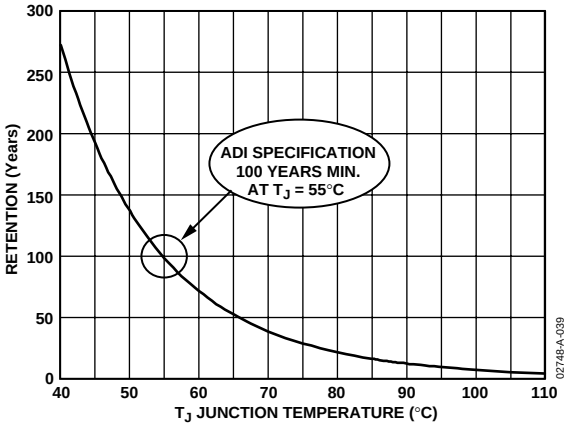

Figure 33. Flash/EE Memory Data Retention

USING FLASH/EE PROGRAM MEMORY

The Flash/EE program memory array can be programmed in one of two modes: serial downloading and parallel programming.

Serial Downloading (In-Circuit Programming)

As part of its factory boot code, the ADuC814 facilitates code download via the standard UART serial port. Serial download mode is automatically entered on power-up or during a hardware RESET operation if the external DLOAD pin is pulled high through an external resistor, as shown in Figure 34. Once in this mode, the user can download code to the program memory array while the device is sited in its target application hardware. A PC serial download executable is provided as part of the ADuC814 QuickStart development system. The Serial Download protocol is detailed in a MicroConverter Applications Note uC004 available from the ADI MicroConverter website at www.analog.com/microconverter.

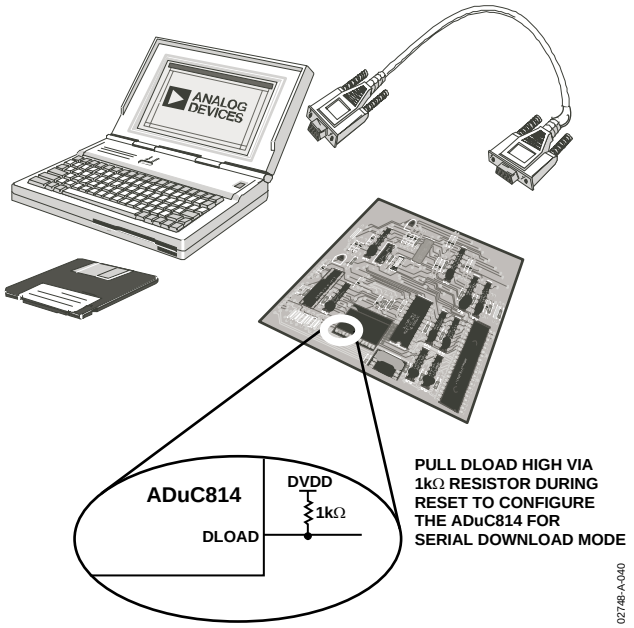

Figure 34. Flash/EE Memory Serial Download Mode Programming

Parallel Programming

The parallel programming mode is fully compatible with conventional third-party Flash or EEPROM device programmers. A block diagram of the external pin configuration required to support parallel programming is shown in Figure 35.

The high voltage (12 V) supply required for Flash/EE programming is generated using on-chip charge pumps to supply the high voltage program lines.

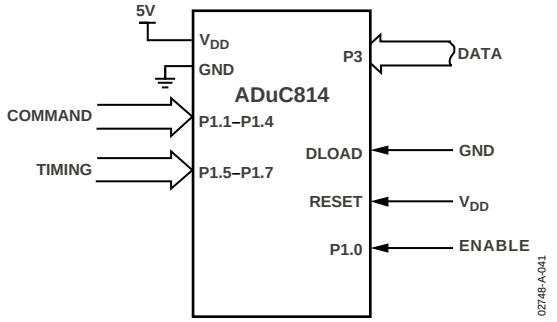

Figure 35. Flash/EE Memory Parallel Programming

FLASH/EE PROGRAM MEMORY SECURITY

The ADuC814 facilitates three modes of Flash/EE program memory security, which are described in the following sections. These modes can be independently activated, restricting access to the internal code space. These security modes can be enabled as part of the user interface available on all ADuC814 serial or parallel programming tools referenced on the MicroConverter website at www.analog.com/microconverter.

Lock Mode

This mode locks code in memory, disabling parallel programming of the program memory, although reading the memory in parallel mode is still allowed. This mode is deactivated by initiating a CODE-ERASE command in serial download or parallel programming modes.

Secure Mode

This mode locks code in memory, disabling parallel programming (program and VERIFY/READ commands). This mode is deactivated by initiating a CODE-ERASE command in serial download or parallel programming modes.

Serial Safe Mode

This mode disables serial download capability on the device. If serial safe mode is activated and an attempt is made to reset the part into serial download mode, i.e., RESET asserted and de-asserted with DLOAD high, the part interprets the serial download reset as a normal reset only. It therefore does not enter serial download mode but only executes a normal reset sequence. Serial safe mode can be disabled only by initiating a CODE-ERASE command in parallel programming mode.

FLASH/EE MEMORY TIMING

The typical program/erase times for the Flash/EE data memory are

Erase Full Array (640 bytes)	2 ms
Erase Single Page (4 bytes)	2 ms
Program Page (4 bytes)	250 µs
Read Page (4 bytes)	Within single instruction cycle

Using the Flash/EE Memory Interface

As with all Flash/EE memory architectures, the array can be programmed in-system at a byte level, although it must be erased first, the erasure being performed in page blocks (4-byte pages in this case).

A typical access to the Flash/EE data array involves setting up the page address to be accessed in the EADRL SFR, configuring the EDATA1–4 with data to be programmed to the array (the EDATA SFRs are not written to for read accesses), and finally, writing the ECON command word, which initiates one of the modes shown Table 11.

Note that a given mode of operation is initiated as soon as the command word is written to the ECON SFR. The core microcontroller operation on the ADuC814 is idled until the requested program/read or erase mode is completed. In practice, this means that even though the Flash/EE memory mode of operation is typically initiated with a two-machine cycle MOV instruction (to write to the ECON SFR), the next instruction cannot be executed until the Flash/EE operation is complete (250 µs or 2 ms later). This means that the core does not respond to interrupt requests until the Flash/EE operation is complete, though the core peripheral functions like counter/timers continue to count and time as configured throughout this period. Although the 640-byte user Flash/EE array is shipped from the factory pre-erased, i.e., byte locations set to FFH, it is nonetheless good programming practice to include an ERASE-ALL routine as part of any configuration/setup code running on the ADuC814. An ERASE-ALL command consists of writing 06H to the ECON SFR, which initiates an erasure of all 640 byte locations in the Flash/EE array. This command coded in 8051 assembly appears as

```
MOV ECON, #06H            ; Erase all Command
                          ; 2 ms Duration
```

Programming a Byte

In general terms, a byte in the Flash/EE array can be programmed only if it has been erased previously. To be more specific, a byte can only be programmed if it already holds the value FFH. Because of the Flash/EE architecture, this erasure must happen at a page level; therefore, a minimum of four bytes (1 page) are erased when an ERASE command is initiated.

A more specific example of the program-byte process is shown below. In this example the user writes F3H into the second byte on Page 03H of the Flash/EE data memory space while preserving the other three bytes already in this page. Because the user is required to modify only one of the page bytes, the full page must be first read so that this page can then be erased without the existing data being lost. This example, coded in 8051 assembly, appears as

```
MOV EADRL,#03H          ; Set Page Address
                        ; Pointer
MOV ECON,#01H           ; Read Page
MOV EDATA2,#0F3H        ; Write New Byte
MOV ECON,#05H           ; Erase Page
MOV ECON,#02H           ; Write Page
                        ; Program Flash/EE)
```

INTVAL	**User Time Interval Select Register**
Function	User code writes the required time interval to this register. When the 8-bit interval counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) is set and generates an interrupt if enabled. (See the IEIP2 SFR description in the Interrupt System section.)
SFR Address	A6H
Power-On Default	00H
Bit Addressable	No
Valid Value	0 to 255 decimal

HTHSEC	**Hundredths Seconds Time Register**
Function	This register is incremented in 1/128 second intervals once TCEN in TIMECON is active. The HTHSEC SFR counts from 0 to 127 before rolling over to increment the SEC time register.
SFR Address	A2H
Power-On Default	00H
Bit Addressable	No
Valid Value	0 to 127 decimal

SEC	**Seconds Time Register**
Function	This register is incremented in 1-second intervals once TCEN in TIMECON is active. The SEC SFR counts from 0 to 59 before rolling over to increment the MIN time register.
SFR Address	A3H
Power-On Default	00H
Bit Addressable	No
Valid Value	0 to 59 decimal

MIN	**Minutes Time Register**
Function	This register is incremented in 1-minute intervals once TCEN in TIMECON is active. The MIN SFR counts from 0 to 59 before rolling over to increment the HOUR time register.
SFR Address	A4H
Power-On Default	00H
Bit Addressable	No
Valid Value	0 to 59 decimal

HOUR	**Hours Time Register**
Function	This register is incremented in 1-hour intervals once TCEN in TIMECON is active. If the TFH bit (TIMECON.6) is set to 1 the HOUR SFR counts from 0 to 23 before rolling over to 0. If the TFH bit is set to 0, the HOUR SFR counts from 0 to 255 before rolling over to 0.
SFR Address	A5H
Power-On Default	00H
Bit Addressable	No
Valid Value	0 to 23 decimal

WATCHDOG TIMER

The purpose of the watchdog timer is to generate a device reset or interrupt within a reasonable amount of time if the ADuC814 enters an erroneous state, possibly due to a programming error, electrical noise, or RFI. The watchdog function can be disabled by clearing the WDE (watchdog enable) bit in the watchdog control (WDCON) SFR. When enabled, the watchdog circuit generates a system reset or interrupt (WDS) if the user program fails to set the watchdog (WDE) bit within a predetermined amount of time (see PRE3–0 bits in WDCON). The watchdog timer itself is a 16-bit counter that is clocked at 32.768 kHz. The watchdog timeout interval can be adjusted via the PRE3–0 bits in WDCON. Full control and status of the watchdog timer function can be controlled via the watchdog timer control SFR (WDCON). The WDCON SFR can be written only by the user software if the double write sequence (WDWR) described in Table 15 is initiated on every write access to the WDCON SFR.

WDCON	**Watchdog Timer Control Register**
SFR Address	C0H
Power-On Default	10H
Bit Addressable	Yes

PRE3	PRE2	PRE1	PRE0	WDIR	WDS	WDE	WDWR

Table 15. WDCON SFR Bit Designation

Bit No.	Name	Description
7	PRE3	Watchdog Timer Prescale Bits.
6	PRE2	The watchdog timeout period is given by the equation
5	PRE1	$t_{WD} = (2^{PRE} \times (2^9/f_{PLL}))$
		where f_{PLL} = 32.768 kHz and PRE is defined as follows:
4	PRE0	PRE3 PRE2 PRE1 PRE0 Timeout Period (ms) Action
		0 0 0 0 15.6 Reset or Interrupt
		0 0 0 1 31.2 Reset or Interrupt
		0 0 1 0 62.5 Reset or Interrupt
		0 0 1 1 125 Reset or Interrupt
		0 1 0 0 250 Reset or Interrupt
		0 1 0 1 500 Reset or Interrupt
		0 1 1 0 1000 Reset or Interrupt
		0 1 1 1 2000 Reset or Interrupt
		1 0 0 0 0.0 Immediate Reset
		PRE3–0 > 1001 Reserved
3	WDIR	Watchdog Interrupt Request.
		If this bit is set by the user, the watchdog generates an interrupt response instead of a system reset when the watchdog timeout period has expired. This interrupt is not disabled by the CLR EA instruction and it is also a fixed, high-priority interrupt.
		If the watchdog is not being used to monitor the system, it can alternatively be used as a timer. The prescaler is used to set the timeout period in which an interrupt is generated. (See Table 33, Note 1, in the Interrupt System section.)
2	WDS	Watchdog Status Bit.
		Set by the watchdog controller to indicate that a watchdog timeout has occurred.
		Cleared by writing a 0 or by an external hardware reset. It is not cleared by a watchdog reset.
1	WDE	Watchdog Enable Bit.
		Set by the user to enable the watchdog and clear its counters. If this bit is not set by the user within the watchdog timeout period, the watchdog generates a reset or interrupt, depending on WDIR.
		Cleared under the following conditions: User writes 0, Watchdog Reset (WDIR = 0); Hardware Reset; PSM Interrupt.
0	WDWR	Watchdog Write Enable Bit.
		To write data into the WDCON SFR involves a double instruction sequence. The WDWR bit must be set and followed immediately by a write instruction to the WDCON SFR. For example:

```
CLR EA           ; disable interrupts while writing to WDT
SETB WDWR        ; allow write to WDCON
MOV WDCON, #72H  ; enable WDT for 2.0s timeout
SET B EA         ; enable interrupts again (if rqd)
```

POWER SUPPLY MONITOR

As its name suggests, the power supply monitor, once enabled, monitors the supply (DV_{DD}) on the ADuC814. It indicates when any of the supply pins drop below one of four user-selectable voltage trip points from 2.63 V to 4.63 V. For correct operation of the power supply monitor function, DV_{DD} must be equal to or greater than 2.7 V. Monitor function is controlled via the PSMCON SFR. If enabled via the IEIP2 SFR, the monitor interrupts the core using the PSMI bit in the PSMCON SFR. This bit is not cleared until the failing power supply has returned above the trip point for at least 250 ms. This monitor function allows the user to save working registers to avoid possible data loss due to the low supply condition, and also ensures that normal code execution does not resume until a safe supply level is well established. The supply monitor is also protected against spurious glitches triggering the interrupt circuit.

PSMCON	**Power Supply Monitor Control Register**
SFR Address	DFH
Power-On Default	DEH
Bit Addressable	No

----	CMPD	PSMI	TPD1	TPD0	----	----	PSMEN

Table 16. PSMCON SFR Bit Designations

Bit No.	Name	Description		
7	PSMCON.7	Reserved.		
6	CMPD	DV_{DD} Comparator Bit.		
		This is a read-only bit and directly reflects the state of the DV_{DD} comparator.		
		Read 1 indicates that the DV_{DD} supply is above its selected trip point.		
		Read 0 indicates that the DV_{DD} supply is below its selected trip point.		
5	PSMI	Power Supply Monitor Interrupt Bit.		
		This bit is set high by the MicroConverter if CMPD is low, indicating low digital supply. The PSMI bit can be used to interrupt the processor. Once CMPD returns and remains high, a 250 ms counter is started. When this counter times out, the PSMI interrupt is cleared. PSMI can also be written by the user; however, if the comparator output is low, it is not possible for the user to clear PSMI.		
4	TPD1	DV_{DD} Trip Point Selection Bits.		
3	TPD0	These bits select the DV_{DD} trip-point voltage as follows:		
		TPD1	TPD0	Selected DV_{DD} Trip Point (V)
		0	0	4.63
		0	1	3.08
		1	0	2.93
		1	1	2.63
2	PSMCON.2	Reserved.		
1	PSMCON.1	Reserved.		
0	PSMEN	Power Supply Monitor Enable Bit.		
		Set to 1 by the user to enable the power supply monitor circuit.		
		Cleared to 0 by the user to disable the power supply monitor circuit.		

SERIAL PERIPHERAL INTERFACE

The ADuC814 integrates a complete hardware serial peripheral interface (SPI) on-chip. SPI is an industry-standard synchronous serial interface that allows eight bits of data to be synchronously transmitted and received simultaneously, i.e., full duplex. Note that the SPI pins MISO and MOSI are multiplexed with digital outputs P3.6 and P3.7. These pins are controlled via the CFG814.0 bit in the CFG814 SFR (Table 17), which configures the relevant Port 3 pins for normal operation or serial port operation. When the relevant Port 3 pins are configured for serial interface operation via the CFG814 SFR, the SPE bit in the SPICON SFR configures SPI or I^2C operation (see SPE bit description in Table 18). SPI can be configured for master or slave operation, and typically consists of four pins described next.

MISO (Master In, Slave Out Data I/O Pin)

The MISO pin (Pin 23) is configured as an input line in master mode and as an output line in slave mode. The MISO line on the master (data in) should be connected to the MISO line in the slave device (data out). The data is transferred as byte-wide (8-bit) serial data, MSB first.

MOSI (Master Out, Slave In Pin)

The MOSI pin (Pin 24) is configured as an output line in master mode and as an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte-wide (8-bit) serial data, MSB first.

SCLOCK (Serial Clock I/O Pin)

The SCLOCK pin (Pin 25) is used to synchronize the data being transmitted and received through the MOSI and MISO data lines. A single data bit is transmitted and received in each SCLOCK period. Therefore, a byte is transmitted/received after eight SCLOCK periods. The SCLOCK pin is configured as an output in master mode and as an input in slave mode.

In master mode, the bit rate, polarity, and phase of the clock are controlled by the CPOL, CPHA, SPR0, and SPR1 bits in the SPICON SFR (see Table 18). In slave mode, the SPICON register must be configured with the phase and polarity (CPHA and CPOL) of the expected input clock. In both master and slave modes, the data is transmitted on one edge of the SCLOCK signal and sampled on the other. It is important, therefore, that the CPHA and CPOL are configured the same for the master and slave devices.

$\overline{SS}$ (Slave Select Input Pin)

The $\overline{SS}$ input pin (Pin 22) is used only when the ADuC814 is configured in slave mode to enable the SPI peripheral. This line is active low. Data is received or transmitted in slave mode only when the $\overline{SS}$ pin is low, allowing the ADuC814 to be used in single master, multislave SPI configurations. If CPHA = 1, then the $\overline{SS}$ input may be permanently pulled low. With CPHA = 0, the $\overline{SS}$ input must be driven low before the first bit in a byte-wide transmission or reception and return high again after the last bit in that byte-wide transmission or reception. In SPI slave mode, the logic level on the external $\overline{SS}$ pin can be read via the SPR0 bit in the SPICON SFR.

The following SFR registers are used to control the SPI interface.

SPICON	**SPI Control Register**
SFR Address	F8H
Power-On Default	04H
Bit Addressable	Yes

ISPI	WCOL	SPE	SPM	CPOL	CPHA	SPR1	SPR0

Table 18. SPICON SFR Bit Designations

Bit No.	Name	Description
7	ISPI	SPI Interrupt Bit. Set by the MicroConverter at the end of each SPI transfer. Cleared directly by the user code or indirectly by reading the SPIDAT SFR.
6	WCOL	Write Collision Error Bit. Set by the MicroConverter if SPIDAT is written to while an SPI transfer is in progress. Cleared by the user.
5	SPE	SPI Interface Enable Bit. Set by the user to enable the SPI interface. Cleared by the user to enable the I^2C interface.
4	SPIM	SPI Master/Slave Mode Select Bit. Set by the user to enable master mode operation (SCLOCK is an output). Cleared by the user to enable slave mode operation (SCLOCK is an input).
3	CPOL[1]	Clock Polarity Select Bit. Set by the user if SCLOCK idles high. Cleared by the user if SCLOCK idles low.

I²C COMPATIBLE INTERFACE

The ADuC814 supports a 2-wire serial interface mode that is I²C compatible. The I²C compatible interface shares its pins with the on-chip SPI interface, and therefore the user can enable only one interface or the other at any given time (see the SPE bit in SPICON SFR, Table 18). Application Note uC001 describes the operation of this interface as implemented, and is available on the MicroConverter website at www.analog.com/microconverter. This interface can be configured as a software master or hardware slave, and uses two pins in the interface.

SDATA (Pin 24) Serial Data I/O

SCLOCK (Pin 25) Serial Clock

Three SFRs are used to control the I²C compatible interface.

I2CCON	**I²C Control Register**
SFR Address	E8H
Power-On Default	00H
Bit Addressable	Yes

MDO	MDE	MCO	MDI	I2CM	I2CRS	I2CTX	I2CI

Table 19. I2CCON SFR Bit Designations

Bit No.	Name	Description
7	MDO	I²C Software Master Data Output Bit (Master Mode Only). This data bit is used to implement a master I²C transmitter interface in software. Data written to this bit is output on the SDATA pin if the data output enable (MDE) bit is set.
6	MDE	I²C Software Master Data Output Enable Bit (Master Mode Only). Set by the user to enable the SDATA pin as an output (Tx). Cleared by the user to enable SDATA pin as an input (Rx).
5	MCO	I²C Software Master Clock Output Bit (Master Mode Only). This data bit is used to implement a master I²C transmitter interface in software. Data written to this bit is output on the SCLOCK pin.
4	MDI	I²C Software Master Data Input Bit (Master Mode Only). This data bit is used to implement a master I²C receiver interface in software. Data on the SDATA pin is latched into this bit on SCLOCK if the data output enable (MDE) bit is 0.
3	I2CM	I²C Master/Slave Mode Bit. Set by the user to enable I²C software master mode. Cleared by the user to enable I²C hardware slave mode.
2	I2CRS	I²C Reset Bit (Slave Mode Only). Set by the user to reset the I²C interface. Cleared by the user code for normal I²C operation.
1	I2CTX	I²C Direction Transfer Bit (Slave Mode Only). Set by the MicroConverter if the interface is transmitting. Cleared by the MicroConverter if the interface is receiving.
0	I2CI	I²C Interrupt Bit (Slave Mode Only). Set by the MicroConverter after a byte has been transmitted or received. Cleared automatically when user code reads the I2CDAT SFR (see the I2CDAT SFR description that follows).

I2CADD	**I²C Address Register**
Function	Holds the I²C peripheral address for the part. It may be overwritten by the user code. Application Note uC001 at www.analog.com/microconverter describes the format of the 7-bit address in detail.
SFR Address	9BH
Power-On Default	55H
Bit Addressable	No

I2CDAT	**I²C Data Register**
Function	The I2CDAT SFR is written to by the user code to transmit data over the I²C interface, or it is read by the user code to read data just received via the I²C interface. Accessing the I2CDAT register automatically clears any pending I²C interrupts and the I2CI bit in the I2CCON SFR.
SFR Address	9AH
Power-On Default	00H
Bit Addressable	No

UART SERIAL INTERFACE

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can begin receiving a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, the first byte is lost. The physical interface to the serial data network is via Pins RxD (P3.0) and TxD (P3.1), while the SFR interface to the UART is comprised of the following registers.

SBUF

The serial port receive and transmit registers are both accessed through the SBUF SFR (SFR address = 99H). Writing to SBUF loads the transmit register and reading SBUF accesses a physically separate receive register.

SCON	**UART Serial Port Control Register**
SFR Address	98H
Power-On Default	00H
Bit Addressable	Yes

SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Table 26. SCON SFR Bit Designations

Bit No.	Name	Description
7	SM0	UART Serial Mode Select Bits.
6	SM1	These bits select the serial port operating mode as follows: SM0 SM1 Selected Operating Mode 0 0 Mode 0: Shift Register, fixed baud rate (Core_Clk/2) 0 1 Mode 1: 8-bit UART, variable baud rate 1 0 Mode 2: 9-bit UART, fixed baud rate (Core_Clk/64) or (Core_Clk/32) 1 1 Mode 3: 9-bit UART, variable baud rate
5	SM2	Multiprocessor Communication Enable Bit. Enables multiprocessor communication in Modes 2 and 3. In Mode 0, SM2 should be cleared. In Mode 1, if SM2 is set, RI is not activated if a valid stop bit is not received. If SM2 is cleared, RI is set as soon as the byte of data is received. In Mode 2 or 3, if SM2 is set, RI is not activated if the received ninth data bit in RB8 is 0. If SM2 is cleared, RI is set as soon as the byte of data is received.
4	REN	Serial Port Receive Enable Bit. Set by the user software to enable serial port reception. Cleared by the user software to disable serial port reception.
3	TB8	Serial Port Transmit (Bit 9). The data loaded into TB8 is the ninth data bit that is transmitted in Modes 2 and 3.
2	RB8	Serial port Receiver Bit 9. The ninth data bit received in Modes 2 and 3 is latched into RB8. For Mode 1, the stop bit is latched into RB8.
1	TI	Set by hardware at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in Modes 1, 2, and 3. Cleared by the user software.
0	RI	Serial Port Receive Interrupt Flag. Set by hardware at the end of the eighth bit in Mode 0, or halfway through the stop bit in Modes 1, 2, and 3. Cleared by user software.

Timer 2 Generated Baud Rates

Baud rates can also be generated using Timer 2. Using Timer 2 is similar to using Timer 1 in that the timer must overflow 16 times before a bit is transmitted/received. Because Timer 2 has a 16-bit autoreload mode, a wide range of baud rates is possible using Timer 2.

Modes 1 and 3 Baud Rate = (1/16) × (*Timer 2 Overflow Rate*)

Therefore, when Timer 2 is used to generate baud rates, the timer increments every two clock cycles and not every core machine cycle as before. Therefore, it increments six times faster than Timer 1, and therefore baud rates six times faster are possible. Because Timer 2 has 16-bit autoreload capability, very low baud rates are still possible. Timer 2 is selected as the baud rate generator by setting the CLK and/or RCLK in T2CON. The baud rates for transmit and receive can be simultaneously different. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode as shown in Figure 53.

In this case, the baud rate is given by the formula

Modes 1 and 3 Baud Rate = (*Core Clk*)/
(32 × [65536 – (*RCAP2H*, *RCAP2L*)])

Table 28 shows some commonly used baud rates and how they could be calculated from a core clock frequency of 2.0971 MHz and 16.7772 MHz.

Table 28. Commonly Used Baud Rates, Timer 2

Ideal Baud	Core CLK	RCAP2H Value	RCAP2L Value	Actual Baud	% Error
19200	16.78	–1 (FFH)	–27 (E5H)	19418	1.14
9600	16.78	–1 (FFH)	–55 (C9H)	9532	0.7
2400	16.78	–1 (FFH)	–218 (26H)	2405	0.21
1200	16.78	–2 (FEH)	–181 (4BH)	1199	0.02
9600	2.10	–1 (FFH)	–7 (FBH)	9362	2.4
2400	2.10	–1 (FFH)	–27 (ECH)	2427	1.14
1200	2.10	–1 (FFH)	–55 (D7H)	1191	0.7

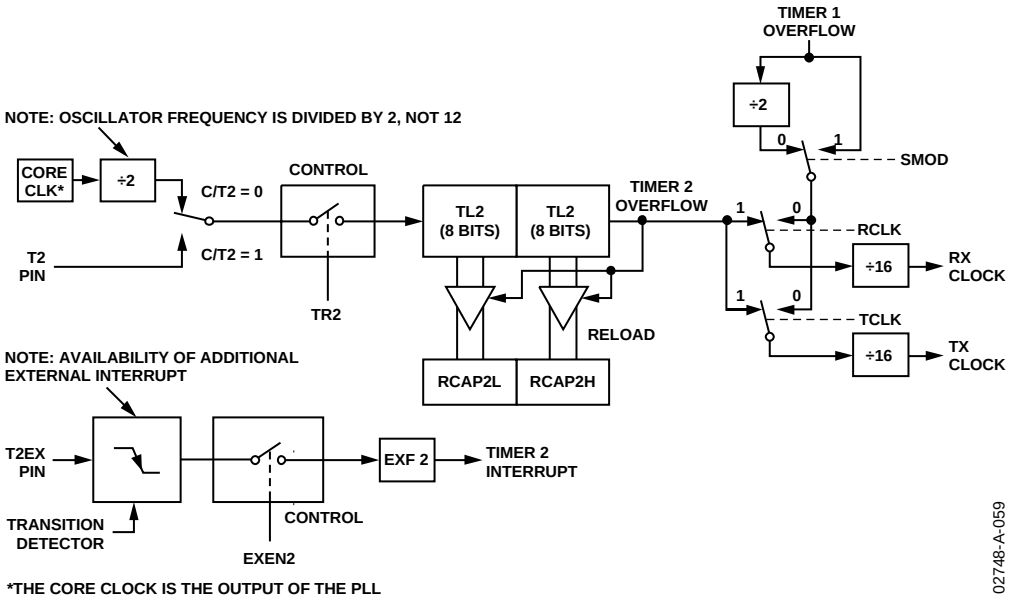

Figure 53. Timer 2, UART Baud Rates

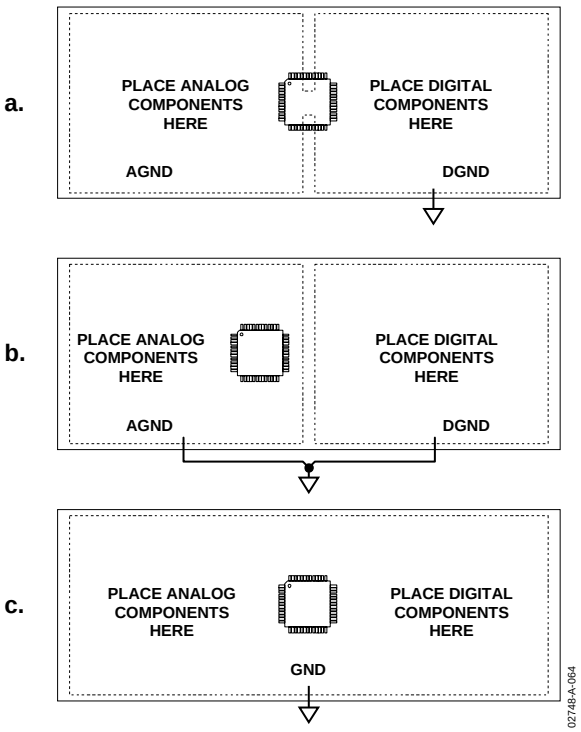

Figure 58. System Grounding Schemes

In all of these scenarios, and in more complicated real-life applications, keep in mind the flow of current from the supplies and back to ground. Make sure the return paths for all currents are as close as possible to the paths the currents took to reach their destinations. For example, do not put power components on the analog side of Figure 58b with DV_{DD} because that would force return currents from DV_{DD} to flow through AGND. Also, try to avoid digital currents flowing under analog circuitry, which could happen if a noisy digital chip is placed on the left half of the board in Figure 58c. Whenever possible, avoid large discontinuities in the ground plane(s) (such as are formed by a long trace on the same layer), because they force return signals to travel a longer path. And of course, make all connections to the ground plane directly, with little or no trace separating the pin from its via to ground.

If the user plans to connect fast logic signals (rise/fall time < 5 ns) to any of the ADuC814's digital inputs, add a series resistor to each relevant line to keep rise and fall times longer than 5 ns at the ADuC814 input pins. A value of 100 Ω or 200 Ω is usually sufficient to prevent high speed signals from coupling capacitively into the ADuC814 and affecting the accuracy of ADC conversions.

OTHER HARDWARE CONSIDERATIONS

To facilitate in-circuit programming, in-circuit debug, and emulation options, users should implement some simple connection points in their hardware. A typical ADuC814 connection diagram is shown in Figure 59.

In-Circuit Serial Download Access

Nearly all ADuC814 designs will want to take advantage of the in-circuit reprogrammability of the chip. This is accomplished by a connection from the ADuC814's UART to a PC, which requires an external RS-232 chip for level translation. If users would rather not design an RS-232 chip onto a board, refer to the Application Note uC006, *A 4-Wire UART-to-PC Interface* (available at www.analog.com/microconverter) for a simple (and zero-cost-per-board) method of gaining in-circuit serial download access to the ADuC814.

In addition to the basic UART connections, users also need a way to trigger the chip into download mode. This is accomplished via a 1 kΩ pull-up resistor that can be jumpered onto the DLOAD pin. To get the ADuC814 into download mode, simply connect this jumper and power-cycle the device (or manually reset the device, if a manual reset button is available), and it will be ready to receive a new program serially. To enable the device to enter normal mode (and run the program) whenever power is cycled or RESET is toggled, the DLOAD pin must be pulled low through a 1 kΩ resistor.

Embedded Serial Port Debugger

From a hardware perspective, entry to serial port debug mode is identical to the serial download entry sequence described in the preceding section. In fact, both serial download and serial port debug modes can be thought of as essentially one mode of operation used in two different ways. Note that the serial port debugger is fully contained on the ADuC814 device, unlike ROM monitor type debuggers.

Table 36. SPI Master Mode Timing (CPHA = 1)

Parameter		Min	Typ	Max	Unit
t_{SL}	SCLOCK Low Pulse Width[1]		630		ns
t_{SH}	SCLOCK High Pulse Width[1]		630		ns
t_{DAV}	Data Output Valid after SCLOCK Edge			50	ns
t_{DSU}	Data Input Setup Time before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time after SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns

[1] Characterized under the following conditions:
a. Core clock divider bits CD2, CD1, and CD0 in PLLCON SFR set to 0, 1, and 1, respectively, i.e., core clock frequency = 2.09 MHz.
b. SPI bit-rate selection bits SPR1 and SPR0 bits in SPICON SFR set to 0 and 0, respectively.

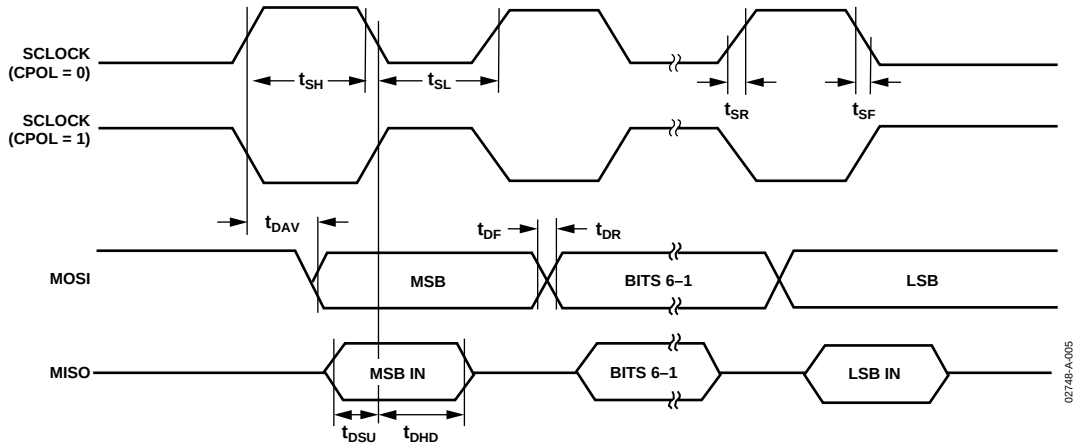

Figure 63. SPI Master Mode Timing (CPHA = 1)

Table 37. SPI Master Mode Timing (CPHA = 0)

Parameter		Min	Typ	Max	Unit
t_{SL}	SCLOCK Low Pulse Width[1]		630		ns
t_{SH}	SCLOCK High Pulse Width[1]		630		ns
t_{DAV}	Data Output Valid after SCLOCK Edge			50	ns
t_{DOSU}	Data Output Setup before SCLOCK Edge			150	ns
t_{DSU}	Data Input Setup Time before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time after SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns

[1] Characterized under the following conditions:
a. Core clock divider bits CD2, CD1, and CD0 bits in PLLCON SFR set to 0, 1, and 1, respectively, i.e., core clock frequency = 2.09 MHz.
b. SPI bit-rate selection bits SPR1 and SPR0 bits in SPICON SFR set to 0 and 0, respectively.

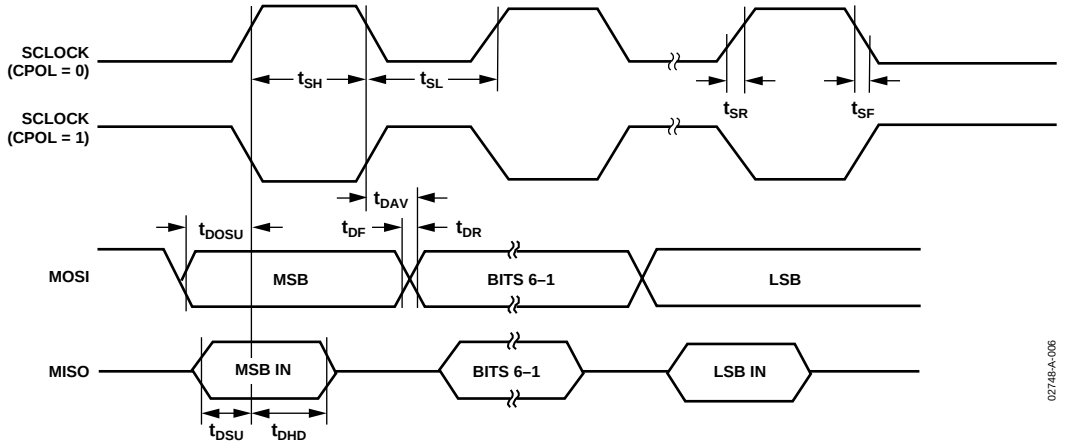

Figure 64. SPI Master Mode Timing (CPHA = 0)

OUTLINE DIMENSIONS

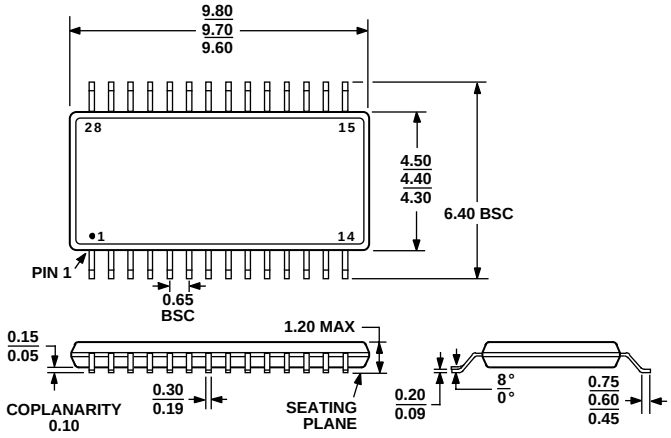

Figure 67. 28-Lead Thin Shrink Small Outline Package (TSSOP) (RU-28)
Dimensions shown in mm