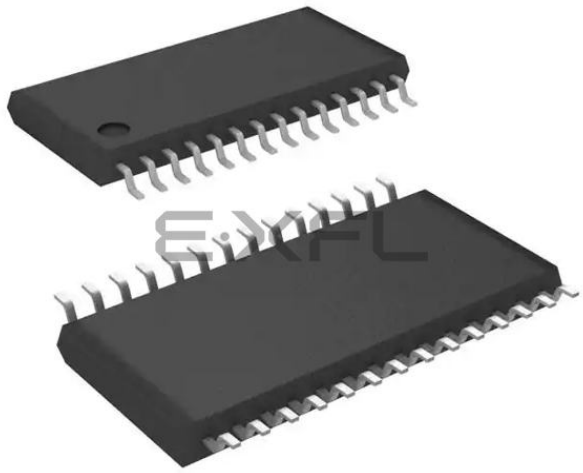

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	16.78MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PSM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 6x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	28-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc814bruz-reel7

SPECIFICATIONS

Table 1. AV_{DD} = DV_{DD} = 2.7 V to 3.3 V or 4.5 V to 5.5 V, V_{REF} = 2.5 V internal reference, XTAL1/XTAL2 = 32.768 kHz crystal. All specifications T_{MIN} to T_{MAX}, unless otherwise specified[1]

Parameter	V_{DD} = 5 V	V_{DD} = 3 V	Unit	Test Conditions
ADC CHANNEL SPECIFICATIONS				
A GRADE				
DC ACCURACY[2,3]				f_{SAMPLE} = 147 kHz
Resolution	12	12	Bits	
Integral Nonlinearity	2	2	LSB max	2.5 V internal reference
	1	1	LSB typ	
	2.5	2.5	LSB typ	1.0 V external reference
Differential Nonlinearity	4	4	LSB max	2.5 V internal reference
	2	2	LSB typ	
	5	5	LSB typ	1.0 V external reference
CALIBRATED ENDPOINT ERRORS[4, 5]				
Offset Error	5	5	LSB max	
Offset Error Match	1	1	LSB typ	
Gain Error	5	5	LSB max	
Gain Error Match	1	1	LSB typ	
DYNAMIC PERFORMANCE[6]				f_{IN} = 10 kHz sine wave f_{SAMPLE} = 147 kHz
Signal to Noise Ratio (SNR)[7]	62.5	62.5	dB typ	
Total Harmonic Distortion (THD)	–65	–65	dB typ	
Peak Harmonic or Spurious Noise	–65	–65	dB typ	
Channel-to-Channel Crosstalk[8]	–80	–80	dB typ	
B GRADE				
DC ACCURACY[2, 3]				f_{SAMPLE} = 147 kHz
Resolution	12	12	Bits	
Integral Nonlinearity	1	1	LSB max	2.5 V internal reference
	0.3	0.3	LSB typ	
	1.5	1.5	LSB max	1.0 V external reference[11]
Differential Nonlinearity	0.9	0.9	LSB max	2.5 V internal reference
	0.25	0.25	LSB typ	
	+1.5/–0.9	1.5/–0.9	LSB max	1.0 V external reference[11]
Code Distribution	1	1	LSB typ	ADC input is a dc voltage
CALIBRATED ENDPOINT ERRORS[4, 5]				
Offset Error	2	3	LSB max	
Offset Error Match	1	1	LSB typ	
Gain Error	2	3	LSB max	
Gain Error Match	1	1	LSB typ	
DYNAMIC PERFORMANCE[6]				f_{IN} = 10 kHz sine wave f_{SAMPLE} = 147 kHz
Signal to Noise Ratio (SNR)[7]	71	71	dB typ	
Total Harmonic Distortion (THD)	–85	–85	dB typ	
Peak Harmonic or Spurious Noise	–85	–85	dB typ	
Channel-to-Channel Crosstalk[8]	–80	–80	dB typ	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	V	
Leakage Current	1	1	µA max	
Input Capacitance	32	32	pF typ	

Parameter	V_{DD} = 5 V	V_{DD} = 3 V	Unit	Test Conditions
SCLOCK and RESET Only[14] (Schmitt-Triggered Inputs)				
V_{T+}	1.3	0.95	V min	
	3.0	2.5	V max	
V_{T-}	0.8	0.4	V min	
	1.4	1.1	V max	
$V_{T+} - V_{T-}$	0.3	0.3	V min	
	0.85	0.85	V max	
INPUT CURRENTS				
P1.2–P1.7, DLOAD	±10	±10	µA max	V_{IN} = 0 V or V_{DD}
SCLOCK[15]	–10	–3	µA min	V_{IN} = 0 V, internal pull-up
	–40	–15	µA max	V_{IN} = 0 V, internal pull-up
	±10	±10	µA max	V_{IN} = V_{DD}
RESET	±10	±10	µA max	V_{IN} = 0 V
	20	10	µA min	V_{IN} = 5 V, 3 V internal pull-down
	105	35	µA max	V_{IN} = 5 V, 3 V internal pull-down
P1.0, P1.1, Port 3[15]	±10	±10	µA max	V_{IN} = 5 V, 3 V
(includes MISO, MOSI/SDATA and $\overline{SS}$)	1	1	µA typ	
	–180	–70	µA min	V_{IN} = 2 V, V_{DD} = 5 V, 3 V
	–660	–200	µA max	
	–360	–100	µA typ	
	–20	–5	µA min	V_{IN} = 450 mV, V_{DD} = 5 V, 3 V
	–75	–25	µA max	
	–38	–12	µA typ	
INPUT CAPACITANCE	5	5	pF typ	All digital inputs
CRYSTAL OSCILLATOR (XTAL1 AND XTAL2)				
Logic Inputs, XTAL1 Only				
V_{INL}, Input Low Voltage	0.8	0.4	V typ	
V_{INH}, Input High Voltage	3.5	2.5	V typ	
XTAL1 Input Capacitance	18	18	pF typ	
XTAL2 Output Capacitance	18	18	pF typ	
DIGITAL OUTPUTS				
Output High Voltage (V_{OH})	2.4	2.4	V min	I_{SOURCE} = 80 mA
Output Low Voltage (V_{OL})				
Port 1.0 and Port 1.1	0.4	0.4	V max	I_{SINK} = 10 mA, T_{MAX} = 85°C
Port 1.0 and Port 1.1	0.4	0.4	V max	I_{SINK} = 10 mA, T_{MAX} = 125°C
SCLOCK, MISO/MOSI	0.4	0.4	V max	I_{SINK} = 4 mA
All Other Outputs	0.4	0.4	V max	I_{SINK} = 1.6 mA
MCU CORE CLOCK				
MCU Clock Rate	131.1	131.1	kHz min	Clock rate generated via on-chip PLL, programmable via CD2-0 in PLLCON
	16.78	16.78	MHz max	
START UP TIME				
At Power-On	500	500	ms typ	
From Idle Mode	100	100	µs typ	
From Power-Down Mode				
Oscillator Running				OSC_PD = 0 in PLLCON SFR
Wake-Up with $\overline{INT0}$ Interrupt	100	100	µs typ	
Wake-Up with SPI/I^2C Interrupt	100	100	µs typ	
Wake-Up with TIC Interrupt	100	100	µs typ	
Wake-Up with External RESET	3	3	ms typ	

PIN CONFIGURATION AND FUNCTION DESCRIPTION

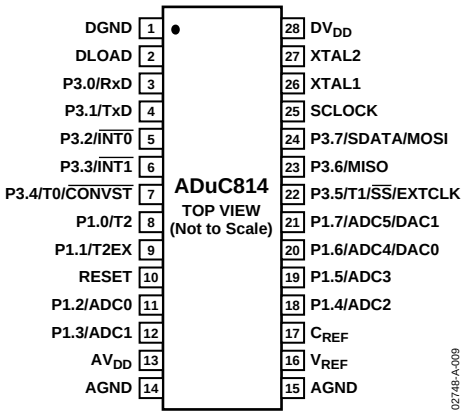

Figure 2. Pin Configuration

Table 3. Pin Descriptions

Pin No.	Mnemonic	Type	Function
1	DGND	S	Digital Ground. Ground reference point for the digital circuitry.
2	DLOAD	I	Debug/Serial Download Mode. Enables when pulled high through a resistor on power-on or RESET. In this mode, DLOAD may also be used as an external emulation I/O pin, therefore the voltage level at this pin must not be changed during this mode of operation because it may cause an emulation interrupt that halts code execution. User code is executed when this pin is pulled low on power-on or RESET.
3–7	P3.0 – P3.4	I/O	Bidirectional Port Pins with Internal Pull-Up Resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, with Port 3 pins being pulled low externally, they source current because of the internal pull-up resistors. When driving a 0-to-1 output transition, a strong pull-up is active during S1 of the instruction cycle. Port 3 pins also have various secondary functions which are described next.
3	P3.0/RxD	I/O	Receiver Data Input (asynchronous) or Data Input/Output (synchronous) in Serial (UART) Mode.
4	P3.1/TxD	I/O	Transmitter Data Output (asynchronous) or Clock Output (synchronous) in Serial (UART) Mode.
5	P3.2/$\overline{\text{INT0}}$	I/O	Interrupt 0, programmable edge or level-triggered interrupt input, which can be programmed to one of two priority levels. This pin can also be used as agate control input to Timer 0.
6	P3.3/$\overline{\text{INT1}}$	I/O	Interrupt 1, programmable edge or level-triggered interrupt input, which can be programmed to one of two priority levels. This pin can also be used as agate control input to Timer 1.
7	P3.4/T0/ $\overline{\text{CONVST}}$	I/O	Timer/Counter 0 Input and External Trigger Input for ADC Conversion Start.
8–9	P1.0–P1.1	I/O	Bidirectional Port Pins with Internal Pull-Up Resistors. Port 1 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs ,with Port 1 pins being pulled low externally, they source current because of the internal pull-up resistors When driving a 0-to-1 output transition a strong pull-up is active during S1 of the instruction cycle. Port 1 pins also have various secondary functions which are described as follows.
8	P1.0/T2	I/O	Timer 2 Digital Input. Input to Timer/Counter 2. When enabled, Counter 2 is incremented in response to a 1 to 0 transition of the T2 input.
9	P1.1/T2EX	I/O	Digital Input. Capture/Reload trigger for Counter 2.
10	RESET	I	Reset Input. A high level on this pin while the oscillator is running resets the device. There is an internal weak pull-down and a Schmitt-trigger input stage on this pin.
11–12	P1.2–P1.3	I	Port 1.2 to P1.3. These pins have no digital output drivers, i.e., they can only function as digital inputs, for which 0 must be written to the port bit. These port pins also have the following analog functionality:
11	P1.2/ADC0	I	ADC Input Channel 0. Selected via ADCCON2 SFR.
12	P1.3/ADC1	I	ADC Input Channel 1. Selected via ADCCON2 SFR.
13	AV_{DD}	S	Analog Positive Supply Voltage, 3 V or 5 V.
14–15	AGND	G	Analog Ground. Ground reference point for the analog circuitry.
16	V_{REF}	I/O	Reference Input/Output. This pin is connected to the internal reference through a switch and is the reference source for the analog to digital converter. The nominal internal reference voltage is 2.5 V and this appears at the pin. This pin can be used to connect an external reference to the analog to digital converter by setting ADCCON1.6 to 1. Connect 0.1 µF between this pin and AGND.

Pin No.	Mnemonic	Type	Function
17	C_{REF}	I	Decoupling Input for On-Chip Reference. Connect 0.1 μF between this pin and AGND.
18–21	P1.4–P1.7	I	Port 1.4 to P1.7. These pins have no digital output drivers, i.e., they can only function as digital inputs, for which 0 must be written to the port bit. These port pins also have the following analog functionality:
18	P1.4/ADC2	I	ADC Input Channel 2. Selected via ADCCON2 SFR.
19	P1.5/ADC3	I	ADC Input Channel 2. Selected via ADCCON2 SFR.
20	P1.6/ADC4/ DAC0	I/O	ADC Input Channel 4. Selected via ADCCON2 SFR. The voltage DAC Channel 0 can also be configured to appear on P1.6.
21	P1.7/ ADC5/DAC1	I/O	ADC Input Channel 5, selected via ADCCON2 SFR. The voltage DAC Channel 1 can also be configured to appear on P1.7.
22–24	P3.5–P3.7	I/O	Bidirectional Port Pins with Internal Pull-Up Resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs ,with Port 3 pins being pulled low externally, they source current because of the internal pull-up resistors. When driving a 0-to-1 output transition a strong pull-up is active during S1 of the instruction cycle. Port 3 pins also have various secondary functions which are described as follows.
22	P3.5/T1		I/O Timer/Counter 1 Input. P3.5–P3.7 pins also have SPI interface functions. To enable these functions, Bit 0 of the CFG814 SFR must be set to 1.
22	P3.5/$\overline{SS}$ /EXTCLK	I/O	This pin also functions as the Slave Select input for the SPI interface when the device is operated in slave mode. P3.5 can also function as an input for an external clock. This clock effectively bypasses the PLL. This function is enabled by setting Bit 1 of the CFG814 SFR.
23	P3.6/MISO	I/O	SPI Master Input/Slave Output Data Input/Output Pin.
24	P3.7/SDATA/ MOSI	I/O	SPI Master Output/Slave Input Data Input/Output Pin.
25	SCLOCK	I/O	Serial Clock Pin for SPI Serial Interface Clock.
26	XTAL1	I	Input to the Crystal Oscillator Inverter.
27	XTAL2	O	Output from the Crystal Oscillator Inverter.
28	DV_{DD}	S	Analog Positive Supply Voltage, 3 V or 5 V.

I = Input, O = Output, S = Supply, G - Ground.

The following notes apply to the entire data sheet:

- In bit designation tables, *set* implies a Logic 1 state, and *cleared* implies a Logic 0 state, unless otherwise stated.
- *Set* and *cleared* also imply that the bit is set or cleared by the ADuC814 hardware, unless otherwise stated.
- User software should not write to reserved or unimplemented bits as they may be used in future products.

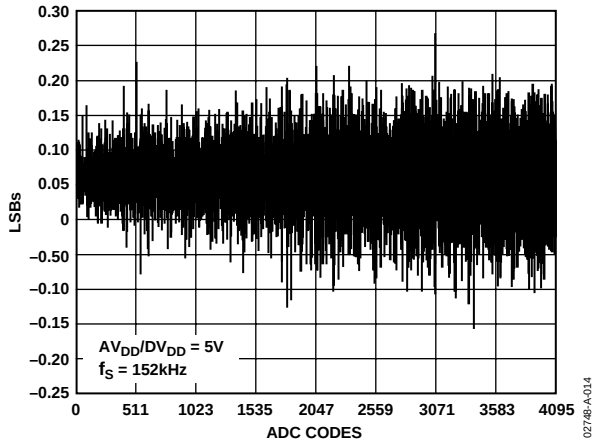

Figure 7. Typical DNL Error, V_{DD} = 5 V

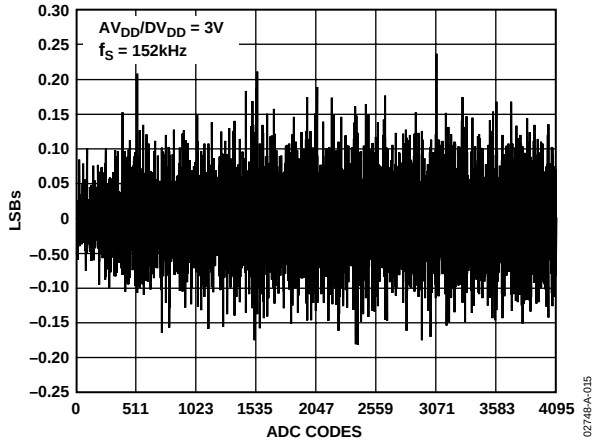

Figure 8. Typical DNL Error, V_{DD} = 3 V

Figure 9 and Figure 10 show the variation in worst-case positive (WCP) DNL and worst-case negative (WCN) DNL versus external reference input voltage.

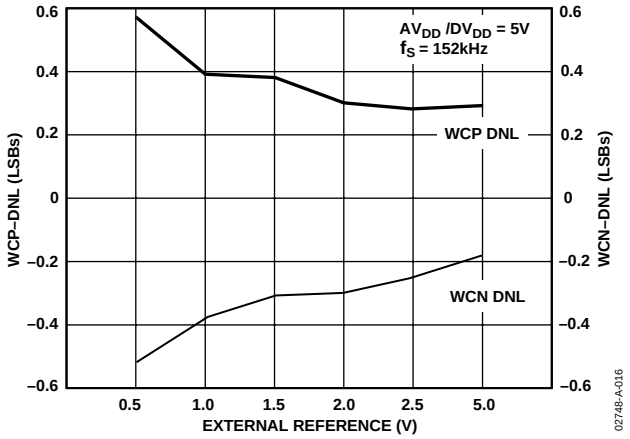

Figure 9. Typical Worst-Case DNL Error vs. V_{REF}, V_{DD} = 5 V

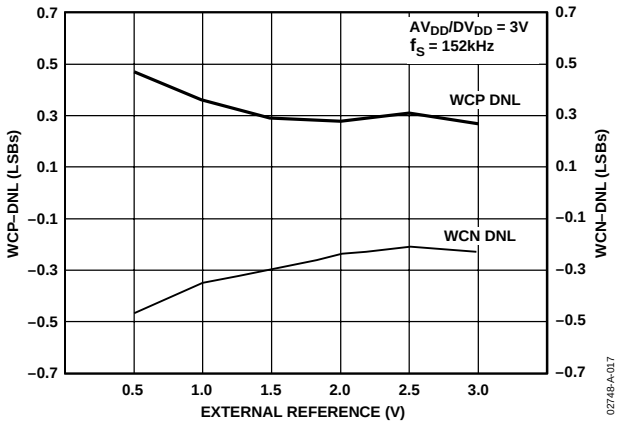

Figure 10. Typical Worst-Case DNL Error vs. V_{REF}, V_{DD} = 3 V

Figure 11 shows a histogram plot of 10,000 ADC conversion results on a dc input with V_{DD} = 5 V. The plot illustrates an excellent code distribution pointing to the low noise performance of the on-chip precision ADC.

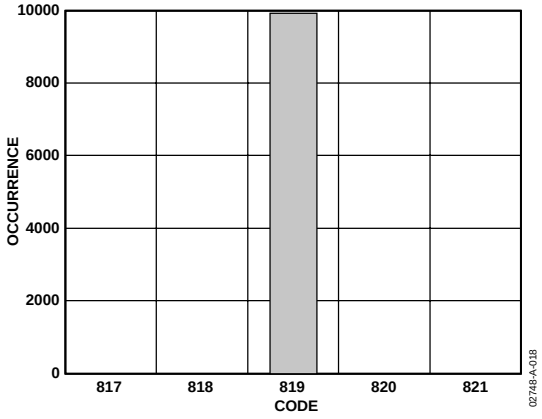

Figure 11. Code Histogram plot, V_{DD} = 5 V

Figure 12 shows a histogram plot of 10,000 ADC conversion results on a dc input for V_{DD} = 3 V. The plot again illustrates a very tight code distribution of 1 LSB with the majority of codes appearing in one output bin.

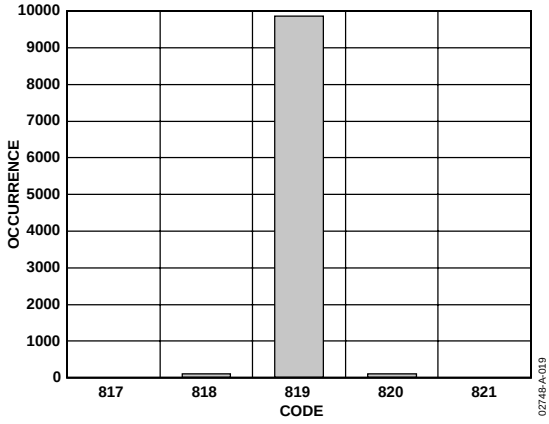

Figure 12. Code Histogram Plot, V_{DD} = 3 V

Figure 13 and Figure 14 show typical FFT plots for the ADuC814. These plots were generated using an external clock input via P3.5 to achieve coherent sampling. The ADC is using its internal reference (2.5 V) sampling a full-scale, 10 kHz sine wave test tone input at a sampling rate of 149.79 kHz. The resultant FFTs shown at 5 V and 3 V supplies illustrate an excellent 100 dB noise floor, a 71 dB signal-to-noise ratio (SNR), and a THD greater than −80 dB.

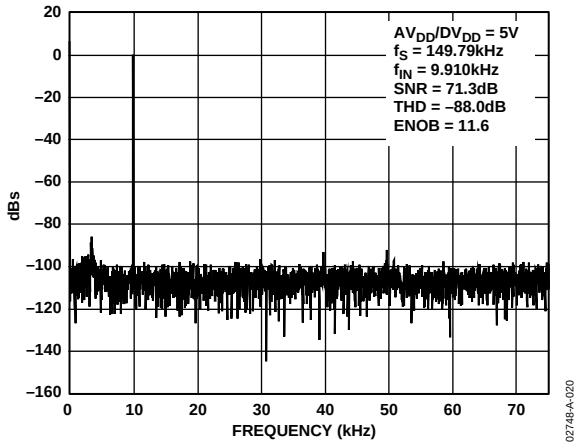

Figure 13. ADuC814 Dynamic Performance at V_{DD} = 5 V

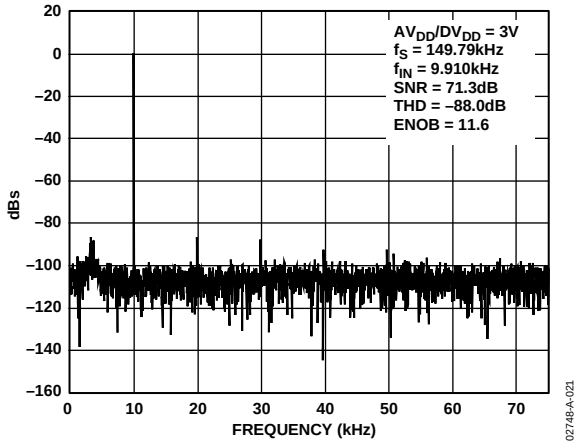

Figure 14. ADuC814 Dynamic Performance at V_{DD} = 3 V

Figure 15 and Figure 16 show typical dynamic performance versus external reference voltages. Again excellent ac performance can be observed in both plots with some roll-off being observed as V_{REF} falls below 1 V.

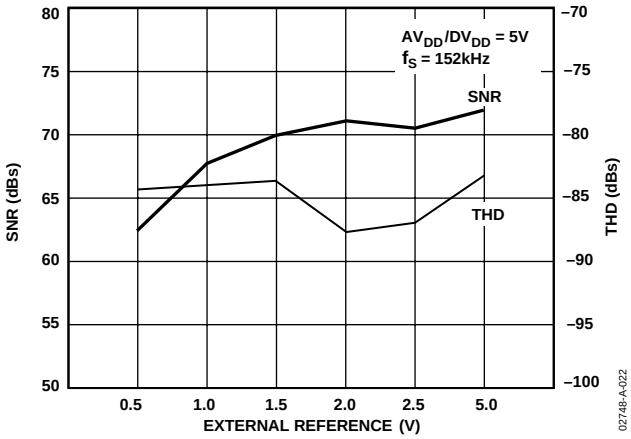

Figure 15. Typical Dynamic Performance vs. V_{REF}, V_{DD} = 5 V

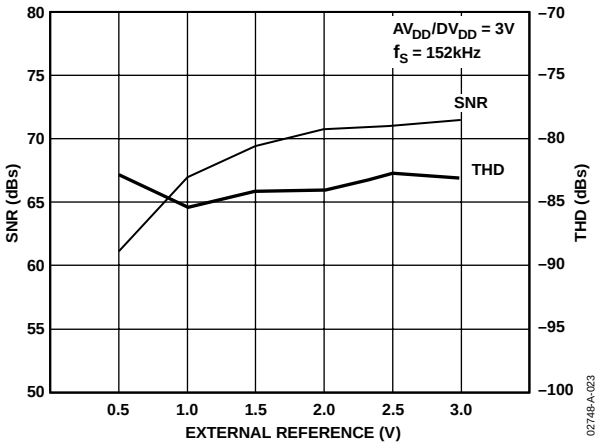

Figure 16. Typical Dynamic Performance vs. V_{REF}, V_{DD} = 3 V

DRIVING THE ADC

The ADC incorporates a successive approximation architecture (SAR) involving a charge-sampled input stage. Each ADC conversion is divided into two distinct phases as defined by the position of the switches in Figure 25. During the sampling phase (with SW1 and SW2 in the track position), a charge proportional to the voltage on the analog input is developed across the input sampling capacitor. During the conversion phase (with both switches in the hold position), the capacitor DAC is adjusted via internal SAR logic until the voltage on Node A is zero, indicating that the sampled charge on the input capacitor is balanced out by the charge being output by the capacitor DAC. The digital value finally contained in the SAR is then latched out as the result of the ADC conversion. Control of the SAR, and timing of acquisition and sampling modes, is handled automatically by built-in ADC control logic. Acquisition and conversion times are also fully configurable under user control.

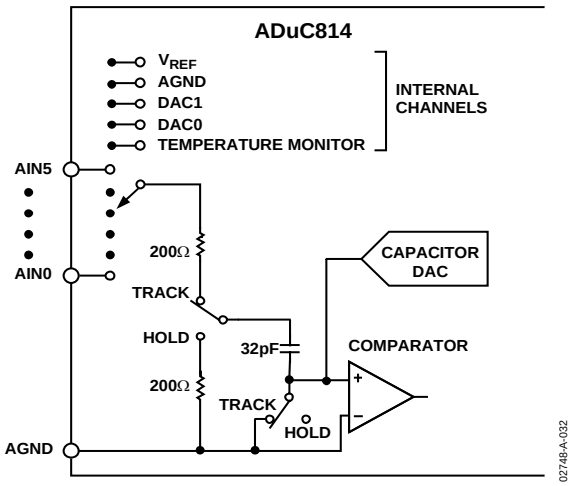

Figure 25. Internal ADC Structure

Note that whenever a new input channel is selected, a residual charge from the 32 pF sampling capacitor places a transient on the newly selected input. The signal source must be capable of recovering from this transient before the sampling switches click into hold mode. Delays can be inserted in software (between channel selection and conversion request) to account for input stage settling, but a hardware solution alleviates this burden from the software design task and ultimately results in a cleaner system implementation.

One hardware solution is to choose a very fast settling op amp to drive each analog input. Such an op amp would need to fully settle from a small signal transient in less than 300 ns in order to guarantee adequate settling under all software configurations. A better solution, recommended for use with any amplifier, is shown in Figure 26.

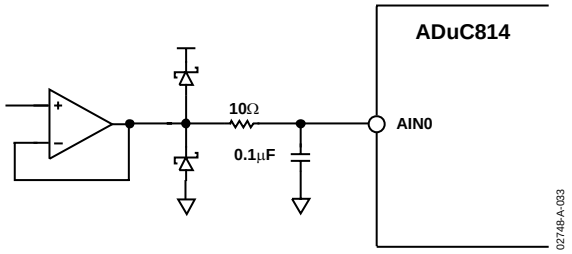

Figure 26. Buffering Analog Inputs

At first glance the circuit in Figure 26 may look like a simple anti-aliasing filter, it actually serves no such purpose. Though the R/C does help to reject some incoming high frequency noise, its primary function is to ensure that the transient demands of the ADC input stage are met. It does so by providing a capacitive bank from which the 32 pF sampling capacitor can draw its charge. Since the 0.1 μF capacitor in Figure 26 is more than 3000 times the size of the 32 pF sampling capacitor, its voltage does not change by more than one count of the 12-bit transfer function when the 32 pF charge from a previous channel is dumped onto it. A larger capacitor can be used if desired, but care needs to be taken if choosing a larger resistor (see Table 9).

The Schottky diodes in Figure 26 may be necessary to limit the voltage applied to the analog input pin as per the Absolute Maximum Ratings. They are not necessary if the op amp is powered from the same supply as the ADuC814 because, in that case, the op amp is unable to generate voltages above V_{DD} or below ground. An op amp of some kind is necessary unless the signal source is very low impedance to begin with. DC leakage currents at the ADuC814 analog inputs can cause measurable dc errors with external source impedances as little as 100 Ω or so. To ensure accurate ADC operation, keep the total source impedance at each analog input less than 61 Ω. Table 9 illustrates examples of how source impedance can affect dc accuracy.

Table 9. Source Impedance Errors

Source Impedance	Error from 1 μA Leakage Current	Error from 10 μA Leakage Current
61 Ω	61 μV = 0.1 LSB	610 μV = 1 LSB
610 Ω	610 μV = 1 LSB	6.1 mV = 10 LSB

Although Figure 26 shows the op amp operating at a gain of 1, you can configure it for any gain needed. Also, you can just as easily use an instrumentation amplifier in its place to condition differential signals. Use any modern amplifier that is capable of delivering the signal (0 V to V_{REF}) with minimal saturation. Some single-supply, rail-to-rail op-amps that are useful for this purpose include, but are certainly not limited to, the ones given in Table 10. Check the Analog Devices literature (CD ROM data book, etc.) for details on these and other op amps and instrumentation amps.

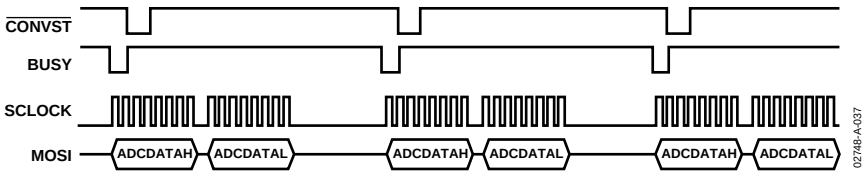

Figure 30. High Speed Data Capture Logic Timing (Pipelined Mode)

In this mode, the ADC to SPI data transfer occurs during the next ADC conversion. To avoid loss of an ADC result, the user must ensure that the ADC to SPI transfer rate is complete before the current ADC conversion ends.

To enable HSDC mode, Bit 6 in ADCCON2 (ADCSPI) must be set and to enable the ADuC814 to capture a contiguous sample stream at full ADC update rates (247 kHz).

To configure the ADuC814 in HSDC mode:

1. The ADC must be put into one of its conversion modes.
2. The SPI interface must be configured. (The SPI configuration is detailed in the Serial Peripheral Interface section).
3. Enable HSDC by setting the ADCSPI bit in the ADCCON2 SFR.
4. Apply trigger signal to the ADC to perform conversions.

Once configured and enabled, the ADC results are transferred from the ADCDATAH/L SFRs to the SPIDAT register. Figure 31 shows the HSDC logic configuration once the mode is enabled. The ADC result is transmitted most significant bit first. In this case, the channel ID is transmitted first, followed by the 12-bit ADC result. When this mode is enabled, normal SPI and Port 3 operation is disabled; however, the core is free to continue code execution, including general housekeeping and communication tasks. This mode is disabled by clearing the ADCSPI bit.

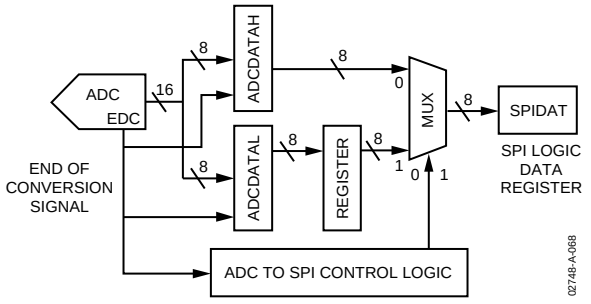

Figure 31. High Speed Data Capture Logic

ADC OFFSET AND GAIN CALIBRATION OVERVIEW

The ADC block incorporates calibration hardware and associated SFRs, which ensures optimum offset and gain performance from the ADC at all times.

As part of internal factory final test routines, the ADuC814 is calibrated to its offset and gain specifications. The offset and gain coefficients obtained from this factory calibration are stored in non-volatile Flash/EE memory. These are downloaded from the Flash/EE memory to offset and gain calibration registers automatically on a power-up or a reset event.

In many applications these factory-generated calibration coefficients suffice. However, the ADuC814 ADC offset and gain accuracy may vary from system to system due to board layout, grounding, clock speed, or system configuration, and so on. To get the best ADC accuracy in your system, an ADC calibration should be performed.

Two main advantages are derived from ensuring the ADC calibration registers are initialized correctly. First, the internal errors in the ADC can be reduced significantly to give superior dc performance; and second, system offset and gain errors can be removed. This allows the user to remove reference errors (whether an internal or external reference) and to use the full dynamic range of the ADC by adjusting the analog input range of the part for a specific system.

ADC OFFSET AND GAIN CALIBRATION COEFFICIENTS

The ADuC814 has two ADC calibration coefficients, one for offset calibration and one for gain calibration. Both the offset and gain calibration coefficients are 14-bit words, and each is stored in two registers located in the special function register (SFR) area. The offset calibration coefficient is divided into ADCOFSH (6 bits) and ADCOFSL (8 bits), and the gain calibration coefficient is divided into ADCGAINH (6 bits) and ADCGAINL (8 bits).

The offset calibration coefficient compensates for dc offset errors in both the ADC and the input signal. Increasing the offset coefficient compensates for positive offset, and effectively pushes down the ADC transfer function. Decreasing the offset coefficient compensates for negative offset, and effectively pushes up the ADC transfer function. The maximum offset that can be compensated is typically ± 3.5% of V_{REF}, which equates to typically ±87.5 mV with a 2.5 V reference.

Similarly, the gain calibration coefficient compensates for dc gain errors in both the ADC and the input signal. Increasing the gain coefficient compensates for a smaller analog input signal range and scales up the ADC transfer function, effectively increasing the slope of the transfer function. Decreasing the

USER INTERFACE TO OTHER ON-CHIP ADuC814 PERIPHERALS

This section gives a brief overview of the various peripherals also available on-chip. A summary of the SFRs used to control and configure these peripherals is also given.

DACS

The ADuC814 incorporates two 12-bit, voltage output DACs on-chip. Each DAC has a rail-to-rail voltage output buffer capable of driving 10 kΩ/100 pF. They have two selectable ranges, 0 V to V_{REF} (an external or the internal band gap 2.5 V reference) and 0 V to AV_{DD}, and can operate in 12-bit or 8-bit modes. DAC operation is controlled by a single special function (SFR) register, DACCON. Each DAC has two data registers, DACxH/L. The DAC0 and DAC1 outputs share pins with ADC inputs ADC4 and ADC5, respectively. When both DACs are on, the number of analog inputs is reduced to four. Note that in 12-bit mode, the DAC voltage output is updated as soon as the DACL data SFR has been written; therefore, the DAC data registers should be updated as DACH first, followed by DACL.

When using the DACs on the V_{REF} range it is necessary to power up the ADC to enable the reference to the DAC section. See Note 1.

DACCON	**DAC Control Register**
SFR Address	FDH
Power-On Default	04H
Bit Addressable	No

MODE	RNG1	RNG0	$\overline{CLR1}$	$\overline{CLR0}$	SYNC	$\overline{PD1}$	$\overline{PD0}$

Table 12. DACCON SFR Bit Designations

Bit No.	Name	Description
7	MODE	Mode Select Bit. Selects either 12-bit or 8-bit mode for both DACs. Set to 1 by the user to enable 8-bit mode (DACxL is the active data register). Set to 0 by the user to enable 12-bit mode.
6	RNG1	DAC1 Output Voltage Range Select Bit. Set to 1 by the user to configure DAC1 range of 0 V to AV_{DD}. Set to 0 by the user to configure DAC1 range of 0 V to 2.5 V (V_{REF} range) [1].
5	RNG0	DAC0 Output Voltage Range Select Bit. Set to 1 by he user to configure DAC0 range of 0 V to AV_{DD}. Set to 0 by the user to configure DAC0 range of 0 V to 2.5 V (V_{REF} range) [1].
4	$\overline{CLR1}$	DAC1 Clear Bit. Set to 1 by the user to enable normal DAC1 operation. Set to 0 by the user to force DAC1 output voltage to 0 V.
3	$\overline{CLR0}$	DAC0 Clear Bit. Set to 1 by the user to enable normal DAC0 operation. Set to 0 by the user to force DAC0 output voltage to 0 V.
2	SYNC	DAC0/1 Update Synchronization Bit. Set to 1 by the user to enable asynchronous update mode. The DAC outputs update as soon as the DACxL SFRs are written. Set to 0 by the user to enable synchronous update mode. The user can simultaneously update both DACs by first updating the DACxH/L SFRs while SYNC is 0. Both DACs then update simultaneously when the SYNC bit is set to 1.
1	$\overline{PD1}$	DAC1 Power-Down Bit. Set to 1 by the user to power up DAC1. Set to 0 by the user to power down DAC1.
0	$\overline{PD0}$	DAC0 Power-Down Bit. Set to 1 by the user to power up DAC0. Set to 0 by the user to power down DAC0.

[1]For correct DAC operation on the 2.5 V to V_{REF} range, the ADC must be powered on.

TIME INTERVAL COUNTER (TIC)

A time interval counter is provided on-chip for counting longer intervals than the standard 8051 compatible timers are capable of. The TIC is capable of time-out intervals ranging from 1/128th second to 255 hours. Furthermore, this counter is clocked by the crystal oscillator rather than by the PLL and thus has the ability to remain active in power-down mode and to time long power-down intervals. This has obvious applications for remote battery-powered sensors where regular, widely spaced readings are required.

Six SFRs are associated with the time interval counter, TIMECON being its control register. Depending on the configuration of the IT0 and IT1 bits in TIMECON, the selected time counter register overflow clocks the interval counter. When this counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) is set and generates an interrupt if enabled. (See IEIP2 SFR description under the Interrupt System section.) If the ADuC814 is in power-down mode, again with TIC interrupt enabled, the TII bit wakes up the device and resumes code execution by vectoring directly to the TIC interrupt service vector address at 0053H. The TIC-related SFRs are described in Table 14. Note that the time based SFRs can be written initially with the current time; the TIC can then be controlled and accessed by the user software. In effect, this facilitates the implementation of a real-time clock. A block diagram of the TIC is shown in Figure 43.

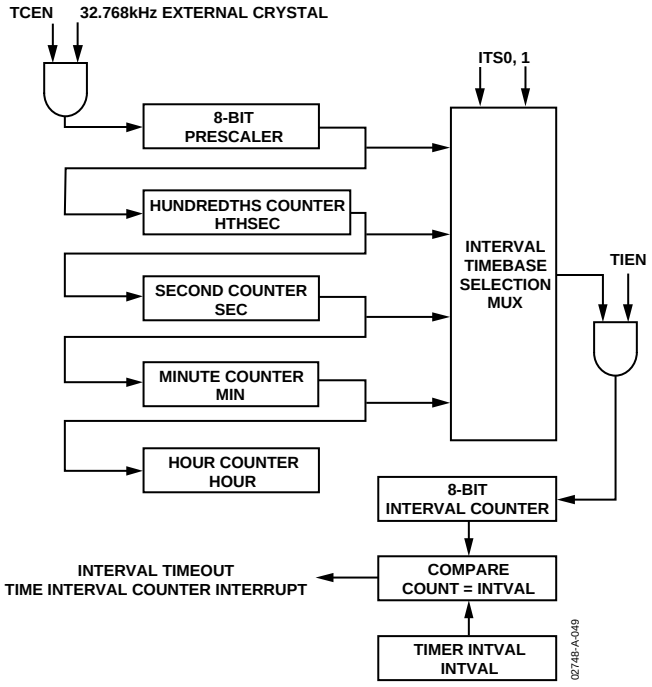

Figure 43. Time Interval Counter, Simplified Block Diagram

TIMERS/COUNTERS

The ADuC814 has three 16-bit timer/counters: Timer 0, Timer 1, and Timer 2. The timer/counter hardware has been included on-chip to relieve the processor core of the overhead inherent in implementing timer/counter functionality in software. Each timer/counter consists of two 8-bit registers, THx and TLx (x = 0, 1 and 2). All three can be configured to operate either as timers or event counters.

In timer function, the TLx register is incremented every machine cycle. Thus one can think of it as counting machine cycles. Since a machine cycle consists of 12 core clock periods, the maximum count rate is 1/12 of the core clock frequency.

In counter function, the TLx register is incremented by a 1-to-0 transition at its corresponding external input pin, T0, T1, or T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes two machine cycles (16 core clock periods) to recognize a 1-to-0 transition, the maximum count rate is 1/16 of the core clock frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it must be held for a minimum of one full machine cycle. Remember that the core clock frequency is programmed via the CD0–CD2 selection bits in the PLLCON SFR. User configuration and control of all timer operating modes is achieved via three SFRs: TMOD, TCON, and T2CON.

TMOD	**Timer/Counter 0 and 1 Mode Register**
SFR Address	89H
Power-On Default	00H
Bit Addressable	No

GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0

Table 22. TMOD SFR Bit Designations

Bit	Name	Description
7	GATE	Timer 1 Gating Control. Set by software to enable Timer/Counter 1 only while $\overline{INT1}$ pin is high and TR1 control bit is set. Cleared by software to enable Timer 1 whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer 1 Timer or Counter Select Bit. Set by software to select counter operation (input from T1 pin). Cleared by software to select timer operation (input from internal system clock).
5	M1	Timer 1 Mode Select Bit 1 (Used with M0 Bit).
4	M0	Timer 1 Mode Select Bit 0. M1 M0 0 0 TH1 operates as an 8-bit timer/counter. TL1 serves as 5-bit prescaler. 0 1 16-Bit Timer/Counter. TH1 and TL1 are cascaded; there is no prescaler. 1 0 8-Bit Auto-Reload Timer/Counter. TH1 holds a value which is to be reloaded into TL1 each time it overflows. 1 1 Timer/Counter 1 Stopped.
3	Gate	Timer 0 Gating Control. Set by software to enable Timer/Counter 0 only while $\overline{INT0}$ pin is high and the TR0 control bit is set. Cleared by software to enable Timer 0 whenever the TR0 control bit is set.
2	C/$\overline{T}$	Timer 0 Timer or Counter Select Bit. Set by software to select counter operation (input from T0 pin). Cleared by software to select timer operation (input from internal system clock).
1	M1	Timer 0 Mode Select Bit 1.
0	M0	Timer 0 Mode Select Bit 0. M1 M0 0 0 TH0 operates as an 8-bit timer/counter. TL0 serves as 5-bit prescaler. 0 1 16-Bit Timer/Counter. TH0 and TL0 are cascaded; there is no prescaler. 1 0 8-Bit Autoreload Timer/Counter. TH0 holds a value which is to be reloaded into TL0 each time it overflows. 1 1 TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits.

TIMER/COUNTER 2 OPERATING MODES

This section describes the operating modes for Timer/Counter 2. The operating modes are selected by bits in the T2CON SFR as shown in Table 27.

Table 25. Mode Selection in T2CON

RCLK (or) TCLK	CAP2	TR2	MODE
0	0	1	16-Bit Autoreload
0	1	1	16-Bit Capture
1	X	1	Baud Rate
X	X	0	OFF

16-Bit Autoreload Mode

In autoreload mode, there are two options that are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then when Timer 2 rolls over, it not only sets TF2 but also causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1, then Timer 2 still performs the above, but with the added feature that a 1-to-0 transition at external input T2EX also triggers the 16-bit reload and sets EXF2. The autoreload mode is illustrated in Figure 49.

16-Bit Capture Mode

In the capture mode, there are again two options that are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which, upon overflowing, sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, then Timer 2 still performs the above, but a 1-to-0 transition on external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt. Capture mode is illustrated in Figure 50.

The baud rate generator mode is selected by RCLK = 1 and/or TCLK = 1. In either case, if Timer 2 is being used to generate the baud rate, the TF2 interrupt flag does not occur. Therefore Timer 2 interrupts do not occur so they do not have to be disabled. In this mode, the EXF2 flag, however, can still cause interrupts; this can be used as a third external interrupt. Baud rate generation is described as part of the UART Serial Interface section that follows.

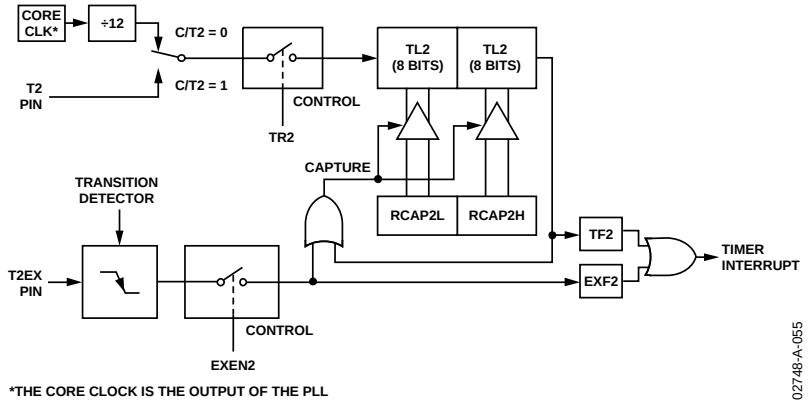

Figure 49. Timer/Counter 2, 16-Bit Autoreload Mode

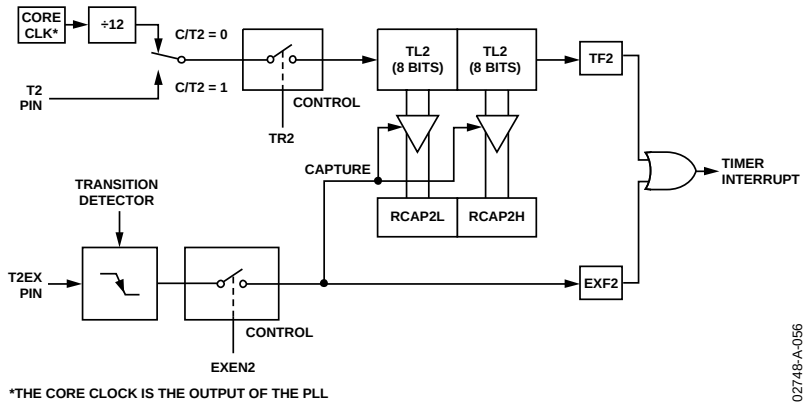

Figure 50. Timer/Counter 2, 16-Bit Capture Mode

Mode 0: 8-Bit Shift Register Mode

Mode 0 is selected by clearing both the SM0 and SM1 bits in the SFR SCON. Serial data enters and exits through RxD. TxD outputs the shift clock. Eight data bits are transmitted or received. Transmission is initiated by any instruction that writes to SBUF. The data is shifted out of the RxD line. The eight bits are transmitted with the least-significant bit (LSB) first, as shown in Figure 52.

Reception is initiated when the receive enable bit (REN) is 1 and the receive interrupt bit (RI) is 0. When RI is cleared the data is clocked into the RxD line and the clock pulses are output from the TxD line.

Mode 1: 8-Bit UART, Variable Baud Rate

Mode 1 is selected by clearing SM0 and setting SM1. Each data byte (LSB first) is preceded by a start bit (Bit 0) and followed by a stop bit (Bit 1). Therefore 10 bits are transmitted on TxD or received on RxD. The baud rate is set by the Timer 1 or Timer 2 overflow rate, or a combination of the two (one for transmission and the other for reception).

Transmission is initiated by writing to SBUF. The write-to-SBUF signal also loads a 1 (stop bit) into the ninth bit position of the transmit shift register. The data is output bit by bit until the stop bit appears on TxD and the transmit interrupt flag (TI) is automatically set as shown in Figure 51.

Reception is initiated when a 1-to-0 transition is detected on RxD. Assuming a valid start bit was detected, character reception continues. The start bit is skipped and the eight data bits are clocked into the serial port shift register. When all eight bits have been clocked in, the following events occur:

- The eight bits in the receive shift register are latched into SBUF.
- The ninth bit (stop bit) is clocked into RB8 in SCON. The receiver interrupt flag (RI) is set if, and only if, the following conditions are met at the time the final shift pulse is generated:
  - RI = 0
  - Either SM2 = 0 or SM2 = 1 and the received stop bit = 1

  If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set.

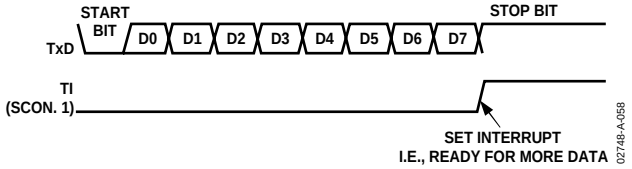

Figure 51. UART Serial Port Transmission, Mode 1

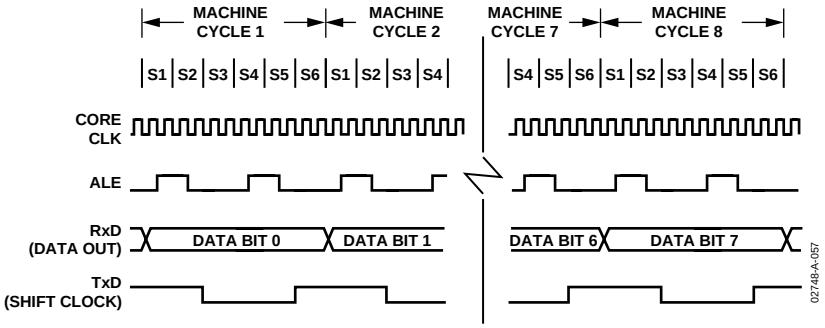

Figure 52. UART Serial Port Transmission, Mode 0

Timer 2 Generated Baud Rates

Baud rates can also be generated using Timer 2. Using Timer 2 is similar to using Timer 1 in that the timer must overflow 16 times before a bit is transmitted/received. Because Timer 2 has a 16-bit autoreload mode, a wide range of baud rates is possible using Timer 2.

Modes 1 and 3 Baud Rate = (1/16) × (*Timer 2 Overflow Rate*)

Therefore, when Timer 2 is used to generate baud rates, the timer increments every two clock cycles and not every core machine cycle as before. Therefore, it increments six times faster than Timer 1, and therefore baud rates six times faster are possible. Because Timer 2 has 16-bit autoreload capability, very low baud rates are still possible. Timer 2 is selected as the baud rate generator by setting the CLK and/or RCLK in T2CON. The baud rates for transmit and receive can be simultaneously different. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode as shown in Figure 53.

In this case, the baud rate is given by the formula

Modes 1 and 3 Baud Rate = (*Core Clk*)/
(32 × [65536 – (*RCAP2H*, *RCAP2L*)])

Table 28 shows some commonly used baud rates and how they could be calculated from a core clock frequency of 2.0971 MHz and 16.7772 MHz.

Table 28. Commonly Used Baud Rates, Timer 2

Ideal Baud	Core CLK	RCAP2H Value	RCAP2L Value	Actual Baud	% Error
19200	16.78	–1 (FFH)	–27 (E5H)	19418	1.14
9600	16.78	–1 (FFH)	–55 (C9H)	9532	0.7
2400	16.78	–1 (FFH)	–218 (26H)	2405	0.21
1200	16.78	–2 (FEH)	–181 (4BH)	1199	0.02
9600	2.10	–1 (FFH)	–7 (FBH)	9362	2.4
2400	2.10	–1 (FFH)	–27 (ECH)	2427	1.14
1200	2.10	–1 (FFH)	–55 (D7H)	1191	0.7

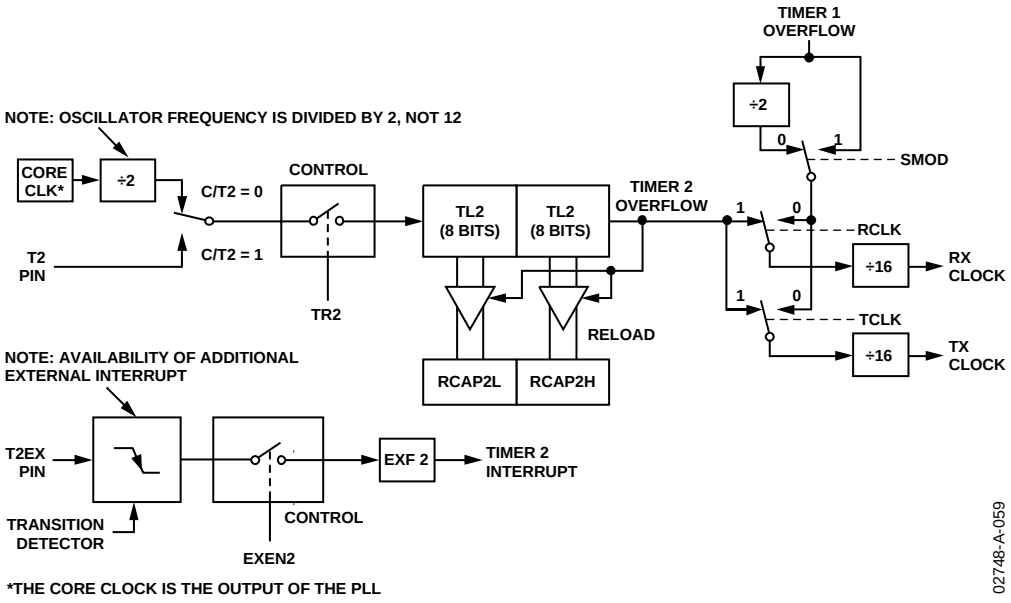

Figure 53. Timer 2, UART Baud Rates

INTERRUPT SYSTEM

The ADuC814 provides a total of twelve interrupt sources with two priority levels. The control and configuration of the interrupt system is carried out through three interrupt-related SFRs.

IE	Interrupt Enable Register
IP	Interrupt Priority Register
IEIP2	Secondary Interrupt Enable and Priority Register

IE	**Interrupt Enable Register**
SFR Address	A8H
Power-On Default	00H
Bit Addressable	Yes

EA	EADC	ET2	ES	ET1	EX1	ET0	EX0

Table 29. IE SFR Bit Designations

Bit No.	Name	Description
7	EA	Global Interrupt Enable. Set by the user to enable all interrupt sources. Cleared by the user to disable all interrupt sources.
6	EADC	ADC Interrupt. Set by the user to enable the ADC interrupt. Cleared by the user to disable the ADC interrupt.
5	ET2	Timer 2 Interrupt. Set by the user to enable the Timer 2 interrupt. Cleared by the user to disable the Timer 2 interrupt.
4	ES	UART Serial Port Interrupt. Set by the user to enable the UART serial port interrupt. Cleared by the user to disable the UART serial port interrupt.
3	ET1	Timer 1 Interrupt. Set by the user to enable the Timer 1 interrupt. Cleared by the user to disable the Timer 1 interrupt.
2	EX1	INT1 Interrupt. Set by the user to enable the External Interrupt 1. Cleared by the user to disable the External Interrupt 1.
1	ET0	Timer 0 Interrupt. Set by the user to enable the Timer 0 interrupt. Cleared by the user to disable the Timer 0 interrupt.
0	EX0	INT0 Interrupt. Set by the user to enable the External Interrupt 0. Cleared by the user to disable the External Interrupt 0.

IP **Interrupt Priority Register**
SFR Address B8H
Power-On Default 00H
Bit Addressable Yes

---	PADC	PT2	PS	PT1	PX1	PT0	PX0

Table 30. IP SFR Bit Designations

Bit No.	Name	Description
7	---	Reserved.
6	PADC	ADC Interrupt Priority. Written to by user to set interrupt priority level (1 = High; 0 = Low).
5	PT2	Timer 2 Interrupt Priority. Written to by the user to set interrupt priority level (1 = High; 0 = Low).
4	PS	UART Serial Port Interrupt Priority. Written to by the user to set interrupt priority level (1 = High; 0 = Low).
3	PT1	Timer 1 Interrupt Priority. Written to by the user to set interrupt priority level (1 = High; 0 = Low).
2	PX1	External Interrupt 1 Priority (INT1). Written to by the user to set interrupt priority level (1 = High; 0 = Low).
1	PT0	Timer 0 Interrupt Priority. Written to by the user to set interrupt priority level (1 = High; 0 = Low).
0	PX0	External Interrupt 0 Priority (INT0). Written to by the user to set interrupt priority level (1 = High; 0 = Low).

IEIP2 **Secondary Interrupt Enable and Priority Register**
SFR Address A9H
Power-On Default A0H
Bit Addressable No

---	PT1	PPSM	PSI	---	ETI	EPSM	ESI

Table 31. IEIP2 SFR Bit Designations

Bit No.	Name	Description
7	---	Reserved.
6	PTI	Time Interval Counter Interrupt Priority. Written to by the user to set TIC interrupt priority (1 = High; 0 = Low).
5	PPSM	PSM Interrupt Priority. Written to by the user to select power supply monitor interrupt priority (1 = High; 0 = Low).
4	PSI	SPI Serial Port Interrupt Priority. Written to by the user to select SPI serial port interrupt priority (1 = High; 0 = Low).
3	---	Reserved. This bit must be 0.
2	ETI	TIC Interrupt. Set by the user to enable the TIC interrupt. Cleared by the user to disable the TIC interrupt.
1	EPSM	Power Supply Monitor Interrupt. Set by the user to enable the power supply monitor interrupt. Cleared by the user to disable the power supply monitor interrupt.
0	ESI	SPI Serial Port Interrupt. Set by the user to enable the SPI serial port interrupt. Cleared by the user to disable the SPI serial port interrupt.

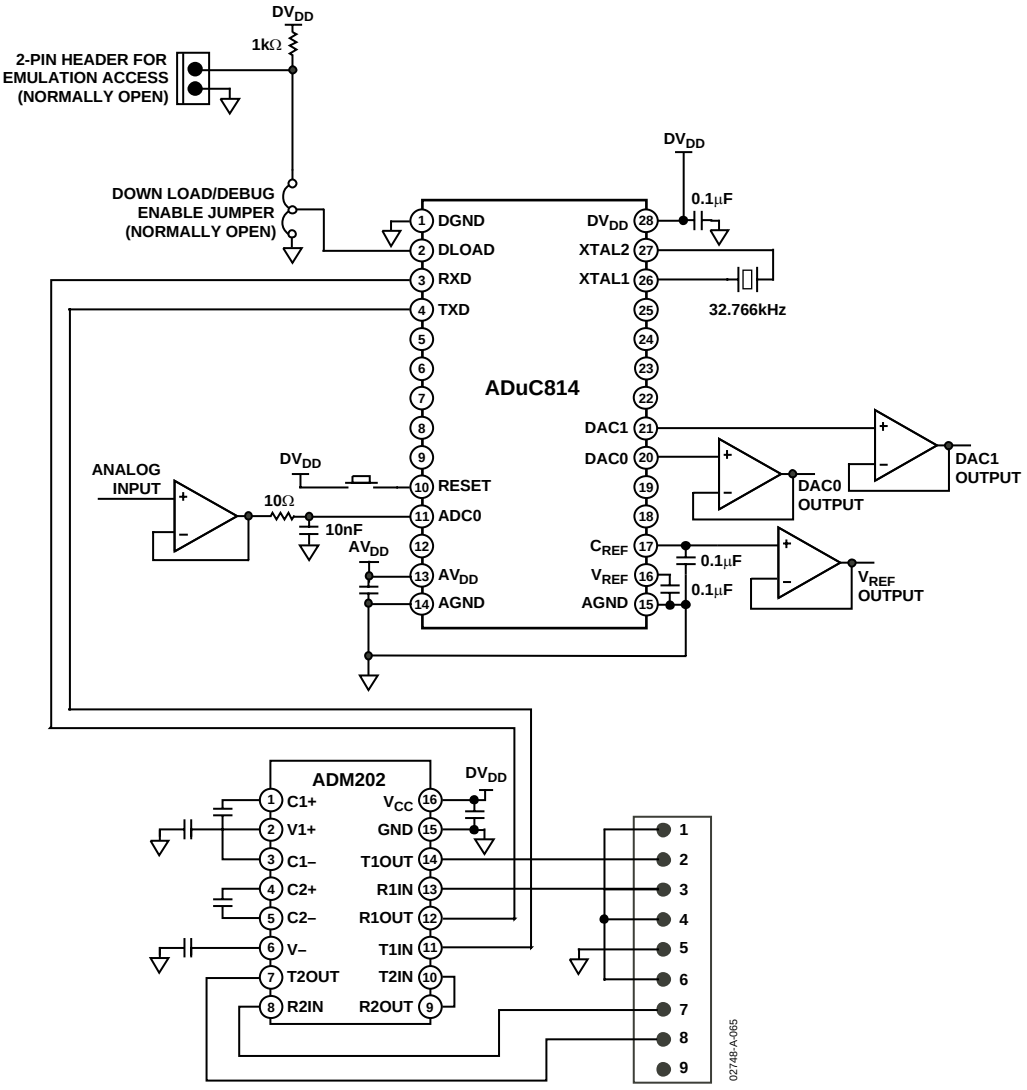

Figure 59. Typical ADuC814 System Connection Diagram

Single-Pin Emulation Mode

Also built into the ADuC814 is a dedicated controller for single-pin in-circuit emulation (ICE) using standard production ADuC814 devices. In this mode, emulation access is gained by connection to a single pin, again the DLOAD pin is used for this function. As described previously, this pin is either high to enable entry into serial download and serial debug modes or low to select normal code execution. To enable single-pin emulation mode, however, users need to pull the DLOAD pin high through a 1 kΩ resistor. The emulator then connects to the 2-pin header. To be compatible with the standard connector that comes with the single-pin emulator available from Accutron Limited (www.accutron.com), use a 2-pin 0.1-inch pitch friction lock header from Molex (www.molex.com) such as their part number 22-27-2021. Be sure to observe the polarity of this header. When the friction lock tab is at the right, the ground pin should be the lower of the two pins (when viewed from the top).

TIMING SPECIFICATIONS[1,2,3]

Table 34. Clock Input (External Clock Driven XTAL1)

AV_{DD} = 2.7 V to 3.3 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.3 V or 4.75 V to 5.25 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted

		32.768 kHz External Crystal			
Parameter		**Min**	**Typ**	**Max**	**Unit**
t_{CK}	XTAL1 Period		30.52		µs
t_{CKL}	XTAL1 Width Low		15.16		µs
t_{CKH}	XTAL1 Width High		15.16		µs
t_{CKR}	XTAL1 Rise Time		20		ns
t_{CKF}	XTAL1 Fall Time		20		ns
$1/t_{CORE}$	ADuC814 Core Clock Frequency[4]	0.131		16.78	MHz
t_{CORE}	ADuC814 Core Clock Period[5]		0.476		µs
t_{CYC}	ADuC814 Machine Cycle Time[6]	0.72	5.7	91.55	µs

[1] AC inputs during testing are driven at DV_{DD} – 0.5 V for a Logic 1, and at 0.45 V for a Logic 0. Timing measurements are made at V_{IH} min for a Logic 1, and at V_{IL} max for a Logic 0 as shown in Figure 61.
[2] For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs as shown in Figure 61.
[3] C_{LOAD} for all outputs = 80 pF, unless otherwise noted.
[4] ADuC814 internal PLL locks onto a multiple (512 times) the external crystal frequency of 32.768 kHz to provide a stable 16.777216 MHz internal clock for the system. The core can operate at this frequency or at a binary submultiple called Core_Clk, selected via the PLLCON SFR.
[5] This number is measured at the default Core_Clk operating frequency of 2.09 MHz.
[6] ADuC814 Machine Cycle Time is nominally defined as 12/Core_CLK.

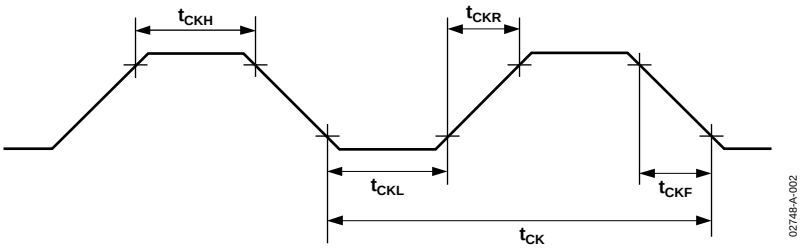

Figure 60. XTAL1 Input

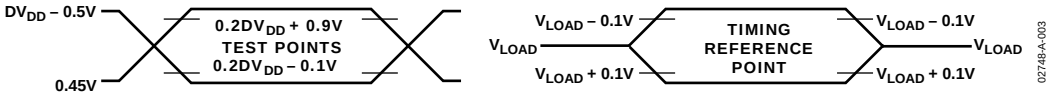

Figure 61. Timing Waveform Characteristics

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADuC814ARU	−40°C to +125°C	Thin Shrink Small Outline (TSSOP)	RU-28
ADuC814ARU-REEL	−40°C to +125°C	Thin Shrink Small Outline (TSSOP)	RU-28
ADuC814ARU-REEL7	−40°C to +125°C	Thin Shrink Small Outline (TSSOP)	RU-28
ADuC814BRU	−40°C to +125°C	Thin Shrink Small Outline (TSSOP)	RU-28
ADuC814BRU-REEL	−40°C to +125°C	Thin Shrink Small Outline (TSSOP)	RU-28
ADuC814BRU-REEL7	−40°C to +125°C	Thin Shrink Small Outline (TSSOP)	RU-28

QuickStart Development System Model	Description
EVAL-ADUC814QS	Development System for the ADuC814 MicroConverter
EVAL-ADUC814QSP[1]	QuickStart PLUS Development System

[1]Only available to order through the web.

NOTES

C02748-0-12/03(A)