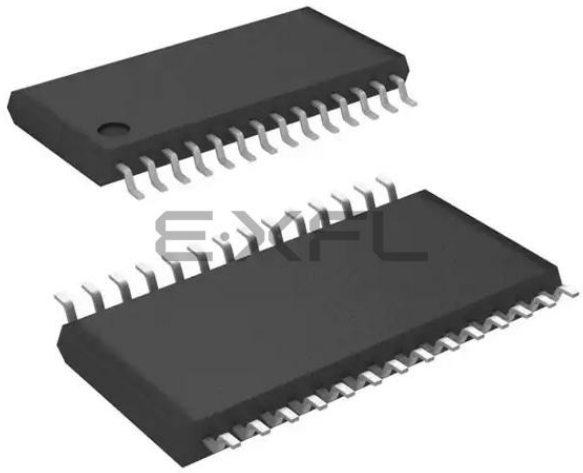

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	16.78MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PSM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 6x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	28-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc814bruz

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Added detailed description of product .... Universal

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Parameter	V_{DD} = 5 V	V_{DD} = 3 V	Unit	Test Conditions
Oscillator Powered Down[16]				OSC_PD = 1 in PLLCON SFR
Wake-Up with $\overline{INT0}$ Interrupt	150	400	ms typ	
Wake-Up with SPI/I²C Interrupt	150	400	ms typ	
Wake-Up with External RESET	150	400	ms typ	
After External RESET in Normal Mode	3	3	ms typ	
After WDT Reset in Normal Mode	3	3	ms typ	Controlled via WDCON SFR
FLASH/EE MEMORY RELIABILITY CHARACTERISTICS[17]				
Endurance[18]	100,000	100,000	Cycles min	
Data Retention[19]	100	100	Years min	
POWER REQUIREMENTS[20, 21]				
Power Supply Voltages				
AV_{DD}/DV_{DD} – AGND		2.7	V min	AV_{DD}/DV_{DD} = 3 V nom
		3.3	V max	
	4.5		V min	AV_{DD}/DV_{DD} = 5 V nom
	5.5		V max	
Power Supply Currents, Normal Mode				
D_{VDD} Current[14]	5	2.5	mA max	Core CLK = 2.097 MHz
	4	2	mA typ	(CD bits in PLLCON = 3)
A_{VDD} Current[14]	1.7	1.7	mA max	
D_{VDD} Current	20	10	mA max	Core CLK = 16.78MHz (max)
	16	8	mA typ	(CD bits in PLLCON = 0)
A_{VDD} Current	1.7	1.7	mA max	
D_{VDD} Current[14]	3.5	1.5	mA max	Core CLK = 131.2 kHz (min)
	2.8	1.2	mA typ	(CD bits in PLLCON = 7)
A_{VDD} Current	1.7	1.7	mA max	
Power Supply Currents, Idle Mode				
D_{VDD} Current[14]	1.7	1.2	mA max	Core CLK = 2.097 MHz
	1.5	1	mA typ	(CD Bits in PLLCON = 3)
AV_{DD} Current[14]	0.15	0.15	mA max	
DV_{DD} Current[14]	6	3	mA max	Core CLK = 16.78 MHz (max)
	4	2.5	mA typ	(CD bits in PLLCON = 0)
AV_{DD} Current[14]	0.15	0.15	mA max	
DV_{DD} Current[14]	1.25	1	mA max	Core CLK = 131 kHz (min)
	1.1	0.7	mA typ	(CD bits in PLLCON = 7)
AV_{DD} Current[14]	0.15	0.15	mA max	
Power Supply Currents, Power-Down Mode				Core CLK = 2.097 MHz or 16.78 MHz (CD bits in PLLCON = 3 or 0)
DV_{DD} Current[14]		20	µA max	Oscillator on
	40	14	µA typ	
AV_{DD} Current	1	1	µA typ	
DV_{DD} Current		15	µA max	Oscillator off
	20	10	µA typ	
AV_{DD} Current	1	1	µA typ	
Typical Additional Power Supply Currents				Core CLK = 2.097 MHz, (CD bits in PLLCON = 3) $AV_{DD} = DV_{DD}$ = 5 V
PSM Peripheral	50		µA typ	
ADC	1.5		mA typ	
DAC	150		µA typ	

TERMINOLOGY

ADC SPECIFICATIONS

Integral Nonlinearity

This is the maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point1/2 LSB below the first code transition and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

This is the deviation of the first code transition (0000 … 000) to (0000 … 001) from the ideal, i.e., +1/2 LSB.

Full-Scale Error

This is the deviation of the last code transition from the ideal AIN voltage (full-scale error has been adjusted out).

Signal-to-(Noise + Distortion) Ratio

This is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$\textit{Signal-to =- (Noise + Distortion)} = (6.02N + 1.76)$$

Thus, for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion (THD)

Total harmonic distortion is the ratio of the rms sum of the harmonics to the fundamental.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and including dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is the noise peak.

DAC SPECIFICATIONS

Relative Accuracy

Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero-scale error and full-scale error.

Voltage Output Settling Time

This is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

Digital-to-Analog Glitch Impulse

This is the amount of charge injected into the analog output when the inputs change state. It is specified as the area of the glitch in nV-sec.

TYPICAL PERFORMANCE CURVES

The typical performance plots presented in this section illustrate typical performance of the ADuC814 under various operating conditions. Note that all typical plots in this section were generated using the ADuC814BRU, i.e., the B-grade part.

Figure 3 and Figure 4 show typical ADC integral nonlinearity (INL) errors from ADC Code 0 to Code 4095 at 5 V and 3 V supplies, respectively. The ADC is using its internal reference (2.5 V) and operating at a sampling rate of 152 kHz. The typical worst-case errors in both plots are just less than 0.3 LSBs.

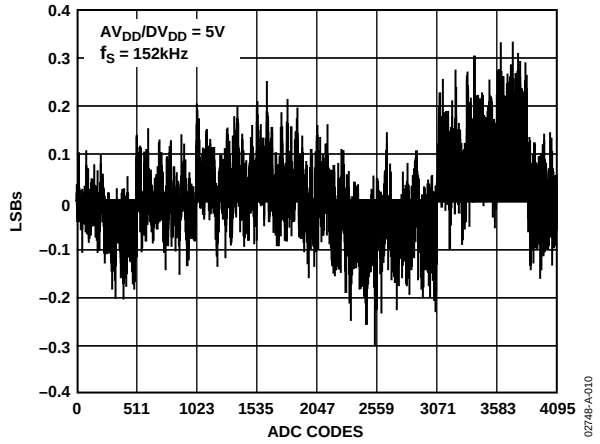

Figure 3. Typical INL Error, V_{DD} = 5 V

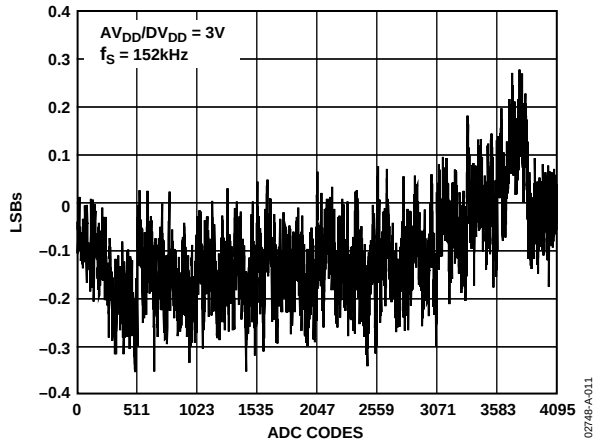

Figure 4. Typical INL Error, V_{DD} = 3 V

Figure 5 and Figure 6 show the variation in worst-case positive (WCP) INL and worst-case negative (WCN) INL versus external reference input voltage.

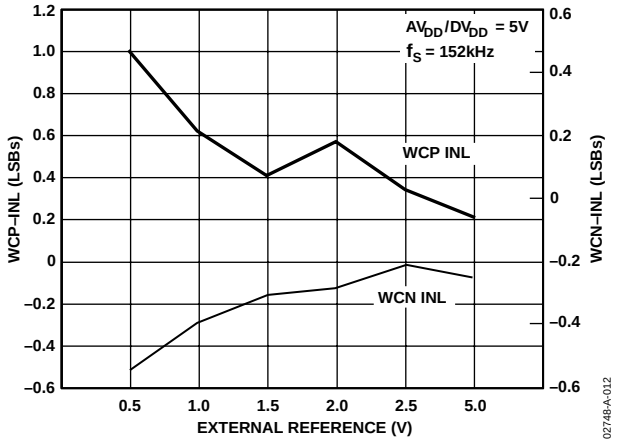

Figure 5. Typical Worst-Case INL Error vs. V_{REF}, V_{DD} = 5 V

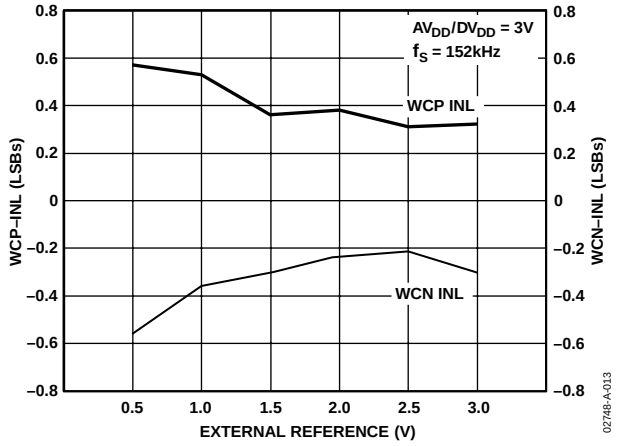

Figure 6. Typical Worst-Case INL Error vs. V_{REF}, V_{DD} = 3 V

Figure 7 and Figure 8 show typical ADC differential nonlinearity (DNL) errors from ADC Code 0 to Code 4095 at 5 V and 3 V supplies, respectively. The ADC is using its internal reference (2.5 V) and operating at a sampling rate of 152 kHz. The typical worst-case errors in both plots are just less than 0.2 LSBs.

ADC CIRCUIT INFORMATION

GENERAL OVERVIEW

The ADC block incorporates a 4.05 msec, 6-channel, 12-bit resolution, single-supply ADC. This block provides the user with a multichannel multiplexer, track-and-hold amplifier, on-chip reference, offset calibration features and ADC. All components in this block are easily configured via a 3-register SFR interface.

The ADC consists of a conventional successive-approximation converter based around a capacitor DAC. The converter accepts an analog input range of 0 V to V_{REF}. A precision, factory calibrated 2.5 V reference is provided on-chip. An external reference may also be used via the external V_{REF} pin. This external reference can be in the range 1.0 V to AV_{DD}.

Single or continuous conversion modes can be initiated in software. In hardware, a convert signal can be applied to an external pin (CONVST), or alternatively Timer 2 can be configured to generate a repetitive trigger for ADC conversions.

The ADuC814 has a high speed ADC to SPI interface data capture logic implemented on-chip. Once configured, this logic transfers the ADC data to the SPI interface without the need for CPU intervention.

The ADC has six external input channels. Two of the ADC channels are multiplexed with the DAC outputs, ADC4 with DAC0, and ADC5 with DAC1. When the DAC outputs are in use, any ADC conversion on these channels represents the DAC output voltage. Due care must be taken to ensure that no external signal is trying to drive these ADC/DAC channels while the DAC outputs are enabled.

In addition to the six external channels of the ADC, five internal signals are also routed through the front end multiplexer. These signals include a temperature monitor, DAC0, DAC1, V_{REF}, and AGND. The temperature monitor is a voltage output from an on-chip band gap reference, which is proportional to absolute temperature. These internal channels can be selected similarly to the external channels via CS3–CS0 bits in the ADCCON2 SFR.

The ADuC814 is shipped with factory programmed offset and gain calibration coefficients that are automatically downloaded to the ADC on a power-on or RESET event, ensuring optimum ADC performance. The ADC core contains automatic endpoint self-calibration and system calibration options that allow the user to overwrite the factory programmed coefficients if desired and tailor the ADC transfer function to the system in which it is being used.

ADC TRANSFER FUNCTION

The analog input range for the ADC is 0 V to V_{REF}. For this range, the designed code transitions occur midway between successive integer LSB values, i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS –3/2 LSBs. The output coding is straight binary with 1 LSB = FS/4096 or 2.5 V/4096 = 0.61 mV when V_{REF} = 2.5 V. The ideal input/output transfer characteristic for the 0 V to V_{REF} range is shown in Figure 23.

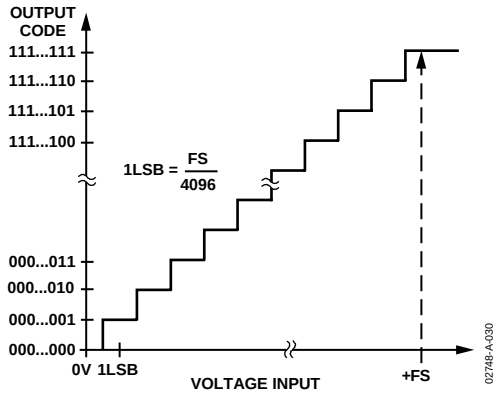

Figure 23. ADuC814 ADC Transfer Function

ADC Data Output Format

Once configured via the ADCCON1–3 SFRs, the ADC converts the analog input and provides an ADC 12-bit result word in the ADCDATAH/L SFRs. The ADCDATAL SFR contains the bottom 8 bits of the 12-bit result. The bottom nibble of the ADCDATAH SFR contains the top 4 bits of the result, while the top nibble contains the channel ID of the ADC channel which has been converted on. This ID corresponds to the channel selection bits CD3–CD0 in the ADCCON2 SFR. The format of the ADC 12-bit result word is shown in Figure 24.

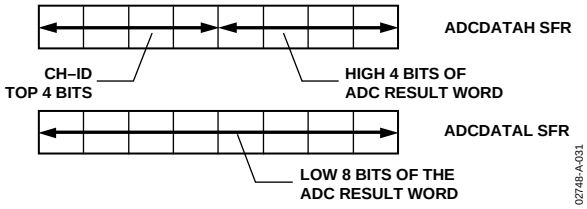

Figure 24. ADC Result Format

SFR INTERFACE TO ADC BLOCK

The ADC operation is fully controlled via three SFRs: ADCCON1, ADCCON2, and ADCCON3. These three registers control the mode of operation.

ADCCON1 (ADC CONTROL SFR 1)

The ADCCON1 register controls conversion and acquisition times, hardware conversion modes, and power-down modes as detailed below.

SFR Address EFH
SFR Power-on Default 00H
Bit Addressable No

MODE	EXT_REF	CK1	CK0	AQ1	AQ0	T2C	EXC

Table 6. ADCCON1 SFR Bit Designations

Bit No.	Name	Description
7	MODE	Mode Bit. This bit selects the operating mode of the ADC. Set to 1 by the user to power on the ADC. Set to 0 by the user to power down the ADC.
6	EXT_REF	External Reference Select Bit. This bit selects which reference the ADC uses when performing a conversion. Set to 1 by the user to switch in an external reference. Set to 0 by the user to switch in the on-chip band gap reference.
5	CK1	ADC Clock Divide Bits.
4	CK0	CK1 and CK0 combine to select the divide ratio for the PLL master clock used to generate the ADC clock. To ensure correct ADC operation, the divider ratio must be chosen to reduce the ADC clock to 4.5 MHz and below. The divider ratio is selected as follows: CK1 CK0 PLL Divider 0 0 8 0 1 4 1 0 16 1 1 32
3	AQ1	The ADC Acquisition Time Select Bits.
2	AQ0	AQ1 and AQ0 combine to select the number of ADC clocks required for the input track-and-hold amplifier to acquire the input signal. The acquisition time is selected as follows: AQ1 AQ0 No. ADC Clks 0 0 1 0 1 2 1 0 3 1 1 4
1	T2C	The Timer2 Conversion Bit. T2C is set to enable the Timer2 overflow bit to be used as the ADC convert start trigger input.
0	EXC	The External Trigger Enable Bit. EXC is set to allow the external CONVST pin be used as the active low convert start trigger input. When enabled, a rising edge on this input pin trigger a conversion. This pin should remain low for a minimum pulse width of 100 nsec at the required sample rate.

ADCCON2 (ADC CONTROL SFR 2)

The ADCCON2 (byte addressable) register controls ADC channel selection and conversion modes as detailed below.

SFR Address D8H
SFR Power-On Default 00H
Bit Addressable Yes

ADCI	ADCSPI	CCONV	SCOVC	CS3	CS2	CS1	CS0

Table 7. ADCCON2 SFR Bit Designations

Bit No.	Name	Description
7	ADCI	ADC Interrupt Bit. ADCI is set at the end of a single ADC conversion cycle. If the ADC interrupt is enabled, the ADCI bit is cleared when user code vectors to the ADC interrupt routine. Otherwise the ADCI bit should be cleared by the user code.
6	ADCSPI	ADCSPI Mode Enable Bit. ADCSPI is set to enable the ADC conversion results to be transferred directly to the SPI data buffer (SPIDAT) without intervention from the CPU.
5	CCONV	Continuous Conversion Bit. CCONV is set to initiate the ADC into a continuous mode of conversion. In this mode the ADC starts converting based on the timing and channel configuration already set up in the ADCCON SFRs. The ADC automatically starts another conversion once a previous conversion cycle has completed. When operating in this mode from 3 V supplies, the ADC should be configured for ADC clock divide of 16 using CK1 and CK0 bits in ADCCON1, and ADC acquisition time should be set to four ADC clocks using AQ1, AQ0 bits in ADCCON1 SFR.
4	SCONV	Single Conversion Bit. SCONV is set to initiate a single conversion cycle. The SCONV bit is automatically reset to 0 on completion of the single conversion cycle. When operating in this mode from 3 V supplies, the maximum ADC sampling rate should not exceed 147 kSPS.
3	CS3	Channel Selection Bits. CS3–CS0 allow the user to program the ADC channel selection under software control. Once a conversion is initiated, the channel converted is pointed to by these channel selection bits. The Channel Select bits operate as follows:
2	CS2	
1	CS1	
0	CS0	

CS3	CS2	CS1	CS0	CHANNEL	
0	0	0	0	0	
0	0	0	1	1	
0	0	1	0	2	
0	0	1	1	3	
0	1	0	0	4	
0	1	0	1	5	
0	1	1	0	X	Not a vaild selection. No ADC channel selected.
0	1	1	1	X	Not a valid selection. No ADC channel selected.
1	0	0	0	Temperature Sensor	
1	0	0	1	DAC0	
1	0	1	0	DAC1	
1	0	1	1	AGND	
1	1	0	0	V_{REF}	

ADCCON3 (ADC CONTROL SFR 3)

The ADCCON3 register controls the operation of various calibration modes as well as giving an indication of ADC busy status.

SFR Address F5H
SFR Power-On Default 00H

BUSY	GNCLD	AVGS1	AVGS0	OFCLD	MODCAL	TYPECAL	SCAL

Table 8. ADCCON3 SFR Bit Designations

Bit No.	Name	Description
7	BUSY	ADC Busy Status Bit. BUSY is a read-only status bit that is set during a valid ADC conversion or calibration cycle. Busy is automatically cleared by the core at the end of a conversion or calibration cycle.
6	GNCLD	Gain Calibration Disable Bit. This bit enables/disables the gain calibration coefficients from affecting the ADC results. Set to 0 to enable gain calibration coefficient Set to 1 to disable gain calibration coefficient.
5	AVGS1	Number of Averages Selection Bits.
4	AVGS0	This bit selects the number of ADC readings averaged for each bit decision during a calibration cycle. AVGS1 AVGS0 Number of Averages 0 0 15 0 1 1 1 0 31 1 1 63
3	OFCLD	Offset Calibration Disable Bit. This bit enables/disables the offset calibration coefficients from affecting the ADC results. Set to 0 to enable offset calibration coefficient. Set to 1 to disable the offset calibration coefficient
2	MODCAL	Calibration Mode Select Bit. This bit should be set to 1 for all calibration cycles.
1	TYPECAL	Calibration Type Select Bit. This bit selects between offset (zero-scale) and gain (full-scale) calibration. Set to 0 for offset calibration. Set to 1 for gain calibration.
0	SCAL	Start Calibration Cycle Bit. When set, this bit starts the selected calibration cycle. It is automatically cleared when the calibration cycle is completed.

NONVOLITILE FLASH/EE MEMORY

FLASH/EE MEMORY OVERVIEW

The ADuC814 incorporates Flash/EE memory technology on-chip to provide the user with nonvolatile, in-circuit reprogrammable code and data memory space.

Flash/EE memory takes the flexible in-circuit reprogrammable features of EEPROM and combines them with the space efficient/density features of EPROM (see Figure 32).

Because Flash/EE technology is based on a single transistor cell architecture, a Flash memory array such as EPROM can be implemented to achieve the space efficiencies or memory densities required by a given design.

Like EEPROM, flash memory can be programmed in-system at a byte level, although it must first be erased; the erase being performed in page blocks. Thus, flash memory is often and more correctly referred to as Flash/EE memory.

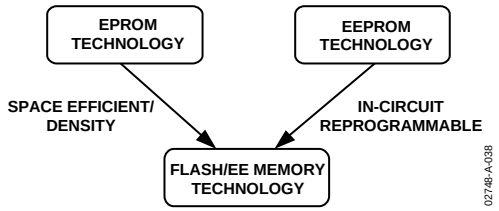

Figure 32. Flash/EE Memory Development

Incorporated in the ADuC814, Flash/EE memory technology allows the user to update program code space in-circuit without the need to replace one-time programmable (OTP) devices at remote operating nodes.

FLASH/EE MEMORY AND THE ADUC814

The ADuC814 provides two arrays of Flash/EE memory for user applications. There are 8 kbytes of Flash/EE program space provided on-chip to facilitate code execution, therefore removing the requirement for an external discrete ROM device. The program memory can be programmed using conventional third-party memory programmers. This array can also be programmed in-circuit, using the serial download mode provided.

A 640-byte Flash/EE data memory space is also provided on-chip. This may be used as a general-purpose nonvolatile scratchpad area. User access to this area is via a group of six SFRs. This space can be programmed at a byte level, although it must first be erased in 4-byte pages.

ADUC814 FLASH/EE MEMORY RELIABILITY

The Flash/EE program and data memory arrays on the ADuC814 are fully qualified for two key Flash/EE memory characteristics: Flash/EE memory cycling endurance and Flash/EE memory data retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many program, read, and erase cycles. In real terms, a single endurance cycle is composed of four independent, sequential events:

1. Initial page erase sequence
2. Read/verify sequence
3. Byte program sequence
4. Second read/verify sequence

In reliability qualification, every byte in both the program and data Flash/EE memory is cycled from 00H to FFH until a first fail is recorded signifying the endurance limit of the on-chip Flash/EE memory.

As indicated in the Specifications tables, the ADuC814 Flash/EE memory endurance qualification has been carried out in accordance with JEDEC Specification A117 over the industrial temperature range of –40°C to +125°C. The results allow the specification of a minimum endurance figure over supply and a temperature of 100,000 cycles, with an endurance figure of 700,000 cycles being typical of operation at 25°C.

Retention quantifies the ability of the Flash/EE memory to retain its programmed data over time. Again, the ADuC814 has been qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature (T_J = 55°C). As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit described above, before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its full specified retention lifetime every time the Flash/EE memory is reprogrammed. It should be noted that retention lifetime, based on an activation energy of 0.6 eV, derates with T_J as shown in Figure 33.

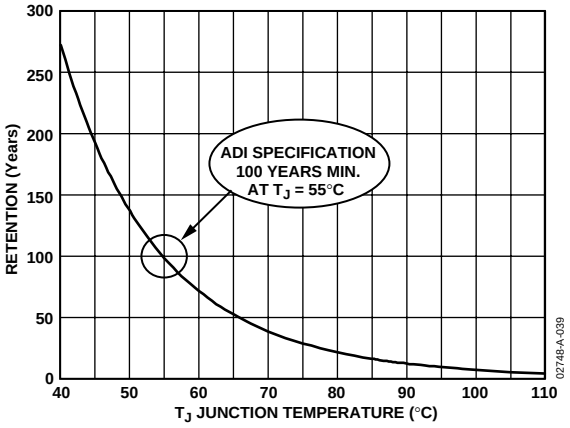

Figure 33. Flash/EE Memory Data Retention

USING FLASH/EE PROGRAM MEMORY

The Flash/EE program memory array can be programmed in one of two modes: serial downloading and parallel programming.

Serial Downloading (In-Circuit Programming)

As part of its factory boot code, the ADuC814 facilitates code download via the standard UART serial port. Serial download mode is automatically entered on power-up or during a hardware RESET operation if the external DLOAD pin is pulled high through an external resistor, as shown in Figure 34. Once in this mode, the user can download code to the program memory array while the device is sited in its target application hardware. A PC serial download executable is provided as part of the ADuC814 QuickStart development system. The Serial Download protocol is detailed in a MicroConverter Applications Note uC004 available from the ADI MicroConverter website at www.analog.com/microconverter.

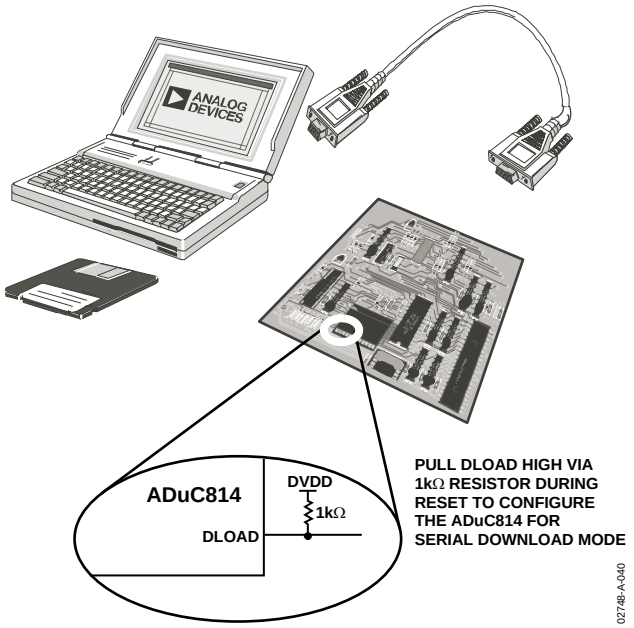

Figure 34. Flash/EE Memory Serial Download Mode Programming

Parallel Programming

The parallel programming mode is fully compatible with conventional third-party Flash or EEPROM device programmers. A block diagram of the external pin configuration required to support parallel programming is shown in Figure 35.

The high voltage (12 V) supply required for Flash/EE programming is generated using on-chip charge pumps to supply the high voltage program lines.

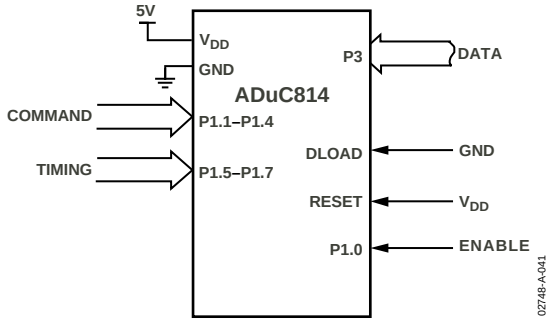

Figure 35. Flash/EE Memory Parallel Programming

FLASH/EE PROGRAM MEMORY SECURITY

The ADuC814 facilitates three modes of Flash/EE program memory security, which are described in the following sections. These modes can be independently activated, restricting access to the internal code space. These security modes can be enabled as part of the user interface available on all ADuC814 serial or parallel programming tools referenced on the MicroConverter website at www.analog.com/microconverter.

Lock Mode

This mode locks code in memory, disabling parallel programming of the program memory, although reading the memory in parallel mode is still allowed. This mode is deactivated by initiating a CODE-ERASE command in serial download or parallel programming modes.

Secure Mode

This mode locks code in memory, disabling parallel programming (program and VERIFY/READ commands). This mode is deactivated by initiating a CODE-ERASE command in serial download or parallel programming modes.

Serial Safe Mode

This mode disables serial download capability on the device. If serial safe mode is activated and an attempt is made to reset the part into serial download mode, i.e., RESET asserted and de-asserted with DLOAD high, the part interprets the serial download reset as a normal reset only. It therefore does not enter serial download mode but only executes a normal reset sequence. Serial safe mode can be disabled only by initiating a CODE-ERASE command in parallel programming mode.

DACxH/L	DAC0 and DAC1 Data Registers
Function	DAC Data Registers, written by the user to update the DAC outputs.
SFR Address	DAC0L (DAC0 data low byte) –> F9H DAC0H (DAC0 data high byte) –> FAH; DAC1L (DAC1 data low byte) –> FBH DAC1H (DAC1 data high byte) –> FCH
Power-On Default	00H –> Both DAC0 and DAC1 data registers.
Bit Addressable	No –> Both DAC0 and DAC1 data registers.

The 12-bit DAC data should be written into DACxH/L right-justified such that DACL contains the lower eight bits, and the lower nibble of DACH contains the upper four bits.

Using the DACs

The on-chip DAC architecture consists of a resistor string DAC followed by an output buffer amplifier, the functional equivalent of which is illustrated in Figure 38. Features of this architecture include inherent guaranteed monotonicity and excellent differential linearity.

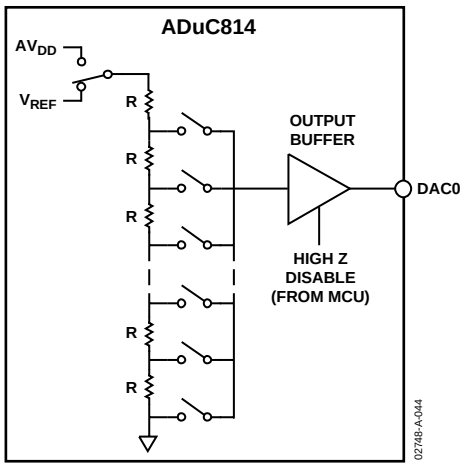

Figure 38. Resistor String DAC Functional Equivalent

As illustrated in Figure 38, the reference source for each DAC is user selectable in software. It can be either AV_{DD} or V_{REF}. In 0 V-to-AV_{DD} mode, the DAC output transfer function spans from 0 V to the voltage at the AV_{DD} pin. In 0 V-to-V_{REF} mode, the DAC output transfer function spans from 0 V to the internal V_{REF}, or if an external reference is applied, the voltage at the V_{REF} pin. The DAC output buffer features a true rail-to-rail output stage implementation. This means that, unloaded, each output is capable of swinging to within less than 100 mV of both AV_{DD} and ground. Moreover, the DAC's linearity specification (when driving a 10 kΩ resistive load to ground) is guaranteed through the full transfer function except Codes 0 to 48, and, in 0 V-to-AV_{DD} mode only, Codes 3945 to 4095. Linearity degradation near ground and V_{DD} is caused by saturation of the output buffer, and a general representation of its effects (neglecting offset and gain error) is illustrated in Figure 39. The dotted line in Figure 39 indicates the ideal transfer function, and the solid line represents what the transfer function might look like with endpoint nonlinearities due to saturation of the output buffer. Note that Figure 39 represents a transfer function in 0 V-to-V_{DD} mode only. In 0 V-to-V_{REF} mode (with $V_{REF} < V_{DD}$), the lower nonlinearity would be similar, but the upper portion of the transfer function would follow the ideal line right to the end (V_{REF} in this case, not V_{DD}), showing no signs of upper endpoint linearity error.

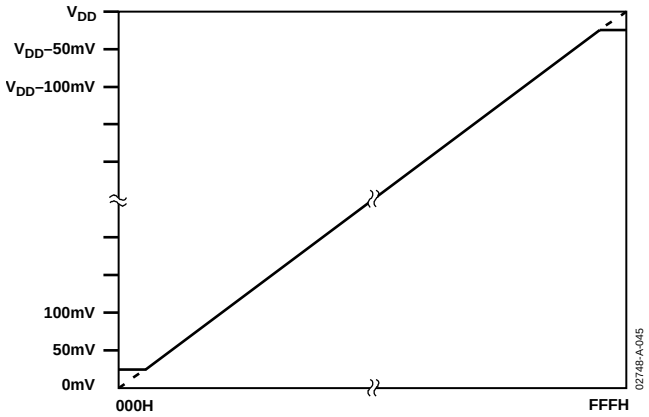

Figure 39. Endpoint Nonlinearities Due to Amplifier Saturation

The endpoint nonlinearities conceptually illustrated in Figure 39 get worse as a function of output loading. Most ADuC814 specifications assume a 10 kΩ resistive load to ground at the DAC output. As the output is forced to source or sink more current, the nonlinear regions at the top or bottom (respectively) of Figure 39 become larger. With larger current demands, this can significantly limit output voltage swing. Figure 40 and Figure 41 illustrate this behavior. Note that the upper trace in each of these figures is valid only for an output range selection of 0 V-to-AV_{DD}. In 0 V-to-V_{REF} mode, DAC loading does not cause high-side voltage drops as long as the reference voltage remains below the upper trace in the corresponding figure. For example, if AV_{DD} = 3 V and V_{REF} = 2.5 V, the high-side voltage is not affected by loads less than 5 mA. But around 7 mA, the upper curve in Figure 41 drops below 2.5 V (V_{REF}), indicating that at these higher currents the output cannot reach V_{REF}.

SERIAL PERIPHERAL INTERFACE

The ADuC814 integrates a complete hardware serial peripheral interface (SPI) on-chip. SPI is an industry-standard synchronous serial interface that allows eight bits of data to be synchronously transmitted and received simultaneously, i.e., full duplex. Note that the SPI pins MISO and MOSI are multiplexed with digital outputs P3.6 and P3.7. These pins are controlled via the CFG814.0 bit in the CFG814 SFR (Table 17), which configures the relevant Port 3 pins for normal operation or serial port operation. When the relevant Port 3 pins are configured for serial interface operation via the CFG814 SFR, the SPE bit in the SPICON SFR configures SPI or I^2C operation (see SPE bit description in Table 18). SPI can be configured for master or slave operation, and typically consists of four pins described next.

MISO (Master In, Slave Out Data I/O Pin)

The MISO pin (Pin 23) is configured as an input line in master mode and as an output line in slave mode. The MISO line on the master (data in) should be connected to the MISO line in the slave device (data out). The data is transferred as byte-wide (8-bit) serial data, MSB first.

MOSI (Master Out, Slave In Pin)

The MOSI pin (Pin 24) is configured as an output line in master mode and as an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte-wide (8-bit) serial data, MSB first.

SCLOCK (Serial Clock I/O Pin)

The SCLOCK pin (Pin 25) is used to synchronize the data being transmitted and received through the MOSI and MISO data lines. A single data bit is transmitted and received in each SCLOCK period. Therefore, a byte is transmitted/received after eight SCLOCK periods. The SCLOCK pin is configured as an output in master mode and as an input in slave mode.

In master mode, the bit rate, polarity, and phase of the clock are controlled by the CPOL, CPHA, SPR0, and SPR1 bits in the SPICON SFR (see Table 18). In slave mode, the SPICON register must be configured with the phase and polarity (CPHA and CPOL) of the expected input clock. In both master and slave modes, the data is transmitted on one edge of the SCLOCK signal and sampled on the other. It is important, therefore, that the CPHA and CPOL are configured the same for the master and slave devices.

$\overline{SS}$ (Slave Select Input Pin)

The $\overline{SS}$ input pin (Pin 22) is used only when the ADuC814 is configured in slave mode to enable the SPI peripheral. This line is active low. Data is received or transmitted in slave mode only when the $\overline{SS}$ pin is low, allowing the ADuC814 to be used in single master, multislave SPI configurations. If CPHA = 1, then the $\overline{SS}$ input may be permanently pulled low. With CPHA = 0, the $\overline{SS}$ input must be driven low before the first bit in a byte-wide transmission or reception and return high again after the last bit in that byte-wide transmission or reception. In SPI slave mode, the logic level on the external $\overline{SS}$ pin can be read via the SPR0 bit in the SPICON SFR.

The following SFR registers are used to control the SPI interface.

SPICON	**SPI Control Register**
SFR Address	F8H
Power-On Default	04H
Bit Addressable	Yes

ISPI	WCOL	SPE	SPM	CPOL	CPHA	SPR1	SPR0

Table 18. SPICON SFR Bit Designations

Bit No.	Name	Description
7	ISPI	SPI Interrupt Bit. Set by the MicroConverter at the end of each SPI transfer. Cleared directly by the user code or indirectly by reading the SPIDAT SFR.
6	WCOL	Write Collision Error Bit. Set by the MicroConverter if SPIDAT is written to while an SPI transfer is in progress. Cleared by the user.
5	SPE	SPI Interface Enable Bit. Set by the user to enable the SPI interface. Cleared by the user to enable the I^2C interface.
4	SPIM	SPI Master/Slave Mode Select Bit. Set by the user to enable master mode operation (SCLOCK is an output). Cleared by the user to enable slave mode operation (SCLOCK is an input).
3	CPOL[1]	Clock Polarity Select Bit. Set by the user if SCLOCK idles high. Cleared by the user if SCLOCK idles low.

TIMERS/COUNTERS

The ADuC814 has three 16-bit timer/counters: Timer 0, Timer 1, and Timer 2. The timer/counter hardware has been included on-chip to relieve the processor core of the overhead inherent in implementing timer/counter functionality in software. Each timer/counter consists of two 8-bit registers, THx and TLx (x = 0, 1 and 2). All three can be configured to operate either as timers or event counters.

In timer function, the TLx register is incremented every machine cycle. Thus one can think of it as counting machine cycles. Since a machine cycle consists of 12 core clock periods, the maximum count rate is 1/12 of the core clock frequency.

In counter function, the TLx register is incremented by a 1-to-0 transition at its corresponding external input pin, T0, T1, or T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes two machine cycles (16 core clock periods) to recognize a 1-to-0 transition, the maximum count rate is 1/16 of the core clock frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it must be held for a minimum of one full machine cycle. Remember that the core clock frequency is programmed via the CD0–CD2 selection bits in the PLLCON SFR. User configuration and control of all timer operating modes is achieved via three SFRs: TMOD, TCON, and T2CON.

TMOD	**Timer/Counter 0 and 1 Mode Register**
SFR Address	89H
Power-On Default	00H
Bit Addressable	No

GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0

Table 22. TMOD SFR Bit Designations

Bit	Name	Description
7	GATE	Timer 1 Gating Control. Set by software to enable Timer/Counter 1 only while $\overline{INT1}$ pin is high and TR1 control bit is set. Cleared by software to enable Timer 1 whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer 1 Timer or Counter Select Bit. Set by software to select counter operation (input from T1 pin). Cleared by software to select timer operation (input from internal system clock).
5	M1	Timer 1 Mode Select Bit 1 (Used with M0 Bit).
4	M0	Timer 1 Mode Select Bit 0. M1 M0 0 0 TH1 operates as an 8-bit timer/counter. TL1 serves as 5-bit prescaler. 0 1 16-Bit Timer/Counter. TH1 and TL1 are cascaded; there is no prescaler. 1 0 8-Bit Auto-Reload Timer/Counter. TH1 holds a value which is to be reloaded into TL1 each time it overflows. 1 1 Timer/Counter 1 Stopped.
3	Gate	Timer 0 Gating Control. Set by software to enable Timer/Counter 0 only while $\overline{INT0}$ pin is high and the TR0 control bit is set. Cleared by software to enable Timer 0 whenever the TR0 control bit is set.
2	C/$\overline{T}$	Timer 0 Timer or Counter Select Bit. Set by software to select counter operation (input from T0 pin). Cleared by software to select timer operation (input from internal system clock).
1	M1	Timer 0 Mode Select Bit 1.
0	M0	Timer 0 Mode Select Bit 0. M1 M0 0 0 TH0 operates as an 8-bit timer/counter. TL0 serves as 5-bit prescaler. 0 1 16-Bit Timer/Counter. TH0 and TL0 are cascaded; there is no prescaler. 1 0 8-Bit Autoreload Timer/Counter. TH0 holds a value which is to be reloaded into TL0 each time it overflows. 1 1 TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits.

T2CON **Timer/Counter 2 Control Register**
SFR Address C8H
Power-On Default 00H
Bit Addressable Yes

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CNT2	CAP2

Table 24. T2CON SFR Bit Designations

Bit No.	Name	Description
7	TF2	Timer 2 Overflow Flag. Set by hardware on a Timer 2 overflow. TF2 is not set when either RCLK or TCLK = 1. Cleared by the user software.
6	EXF2	Timer 2 External Flag. Set by hardware when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. Cleared by the user software.
5	RCLK	Receive Clock Enable. Set by the user to enable the serial port to use Timer 2 overflow pulses for its receive clock in serial port in Modes 1 and 3. Cleared by the user to enable Timer 1 overflow to be used for the receive clock.
4	TCLK	Transmit Clock Enable Bit. Set by the user to enable the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. Cleared by the user to enable Timer 1 overflow to be used for the transmit clock.
3	EXEN2	Timer 2 External Enable Flag. Set by the user to enable a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. Cleared by the user for Timer 2 to ignore events at T2EX.
2	TR2	Timer 2 Start/Stop Control Bit. Set by the user to start Timer 2. Cleared by the user to stop Timer 2.
1	CNT2	Timer 2 timer or counter function select bit. Set by the user to select counter function (input from external T2 pin). Cleared by the user to select timer function (input from on-chip core clock).
0	CAP2	Timer 2 Capture/Reload Select Bit. Set by the user to enable captures on negative transitions at T2EX if EXEN2 = 1. Cleared by the user to enable autoreloads with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to autoreload on Timer 2 overflow.

Timer/Counter 2 Data Registers

Timer/Counter 2 also has two pairs of 8-bit data registers associated with it. These are used as both timer data registers and timer capture/reload registers.

TH2 and TL2 Timer 2, data high byte and low byte.
SFR Address CDH, CCH, respectively

RCAP2H and RCAP2L Timer 2, Capture/Reload byte and low byte.
SFR Address CBH, CAH, respectively

TIMER/COUNTER 2 OPERATING MODES

This section describes the operating modes for Timer/Counter 2. The operating modes are selected by bits in the T2CON SFR as shown in Table 27.

Table 25. Mode Selection in T2CON

RCLK (or) TCLK	CAP2	TR2	MODE
0	0	1	16-Bit Autoreload
0	1	1	16-Bit Capture
1	X	1	Baud Rate
X	X	0	OFF

16-Bit Autoreload Mode

In autoreload mode, there are two options that are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then when Timer 2 rolls over, it not only sets TF2 but also causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1, then Timer 2 still performs the above, but with the added feature that a 1-to-0 transition at external input T2EX also triggers the 16-bit reload and sets EXF2. The autoreload mode is illustrated in Figure 49.

16-Bit Capture Mode

In the capture mode, there are again two options that are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which, upon overflowing, sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, then Timer 2 still performs the above, but a 1-to-0 transition on external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt. Capture mode is illustrated in Figure 50.

The baud rate generator mode is selected by RCLK = 1 and/or TCLK = 1. In either case, if Timer 2 is being used to generate the baud rate, the TF2 interrupt flag does not occur. Therefore Timer 2 interrupts do not occur so they do not have to be disabled. In this mode, the EXF2 flag, however, can still cause interrupts; this can be used as a third external interrupt. Baud rate generation is described as part of the UART Serial Interface section that follows.

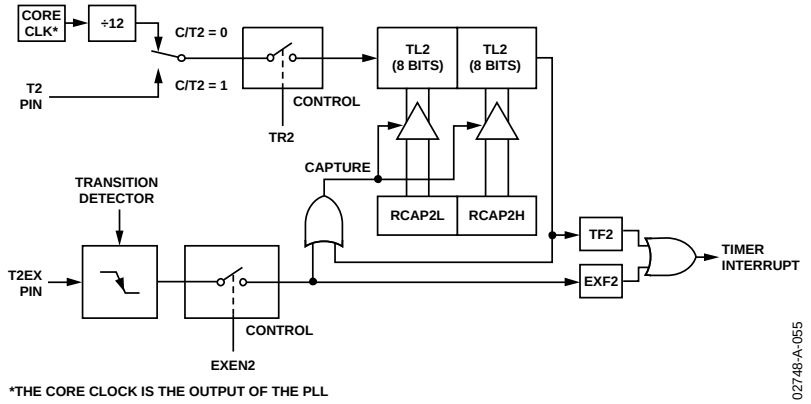

Figure 49. Timer/Counter 2, 16-Bit Autoreload Mode

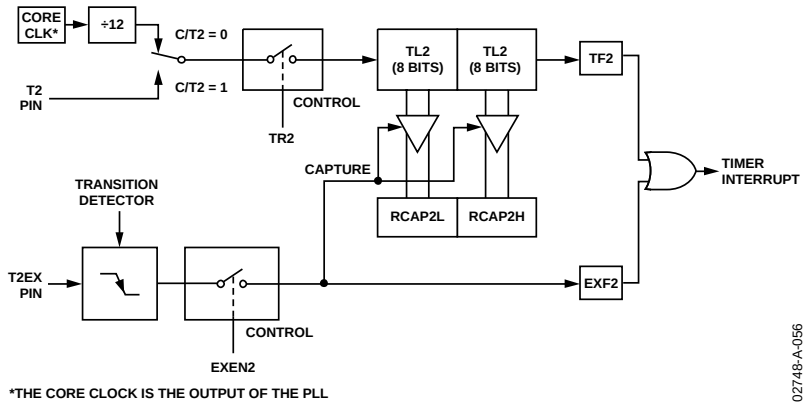

Figure 50. Timer/Counter 2, 16-Bit Capture Mode

Mode 0: 8-Bit Shift Register Mode

Mode 0 is selected by clearing both the SM0 and SM1 bits in the SFR SCON. Serial data enters and exits through RxD. TxD outputs the shift clock. Eight data bits are transmitted or received. Transmission is initiated by any instruction that writes to SBUF. The data is shifted out of the RxD line. The eight bits are transmitted with the least-significant bit (LSB) first, as shown in Figure 52.

Reception is initiated when the receive enable bit (REN) is 1 and the receive interrupt bit (RI) is 0. When RI is cleared the data is clocked into the RxD line and the clock pulses are output from the TxD line.

Mode 1: 8-Bit UART, Variable Baud Rate

Mode 1 is selected by clearing SM0 and setting SM1. Each data byte (LSB first) is preceded by a start bit (Bit 0) and followed by a stop bit (Bit 1). Therefore 10 bits are transmitted on TxD or received on RxD. The baud rate is set by the Timer 1 or Timer 2 overflow rate, or a combination of the two (one for transmission and the other for reception).

Transmission is initiated by writing to SBUF. The write-to-SBUF signal also loads a 1 (stop bit) into the ninth bit position of the transmit shift register. The data is output bit by bit until the stop bit appears on TxD and the transmit interrupt flag (TI) is automatically set as shown in Figure 51.

Reception is initiated when a 1-to-0 transition is detected on RxD. Assuming a valid start bit was detected, character reception continues. The start bit is skipped and the eight data bits are clocked into the serial port shift register. When all eight bits have been clocked in, the following events occur:

- The eight bits in the receive shift register are latched into SBUF.
- The ninth bit (stop bit) is clocked into RB8 in SCON. The receiver interrupt flag (RI) is set if, and only if, the following conditions are met at the time the final shift pulse is generated:
  - RI = 0
  - Either SM2 = 0 or SM2 = 1 and the received stop bit = 1

  If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set.

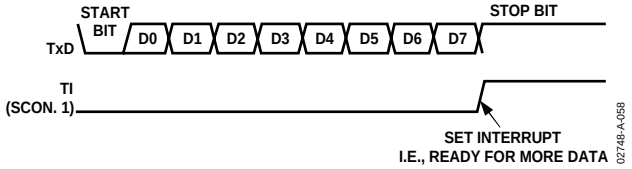

Figure 51. UART Serial Port Transmission, Mode 1

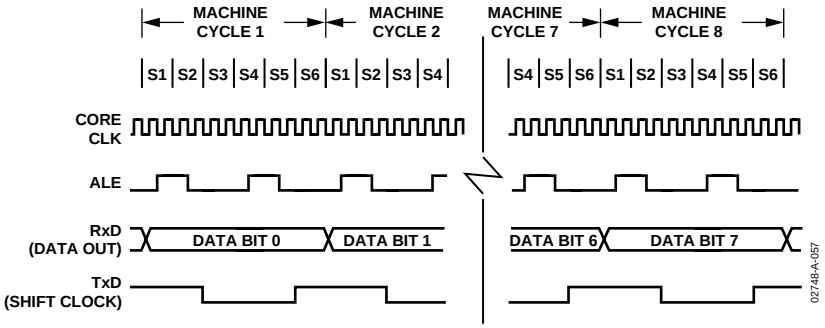

Figure 52. UART Serial Port Transmission, Mode 0

Timer 2 Generated Baud Rates

Baud rates can also be generated using Timer 2. Using Timer 2 is similar to using Timer 1 in that the timer must overflow 16 times before a bit is transmitted/received. Because Timer 2 has a 16-bit autoreload mode, a wide range of baud rates is possible using Timer 2.

Modes 1 and 3 Baud Rate = (1/16) × (*Timer 2 Overflow Rate*)

Therefore, when Timer 2 is used to generate baud rates, the timer increments every two clock cycles and not every core machine cycle as before. Therefore, it increments six times faster than Timer 1, and therefore baud rates six times faster are possible. Because Timer 2 has 16-bit autoreload capability, very low baud rates are still possible. Timer 2 is selected as the baud rate generator by setting the CLK and/or RCLK in T2CON. The baud rates for transmit and receive can be simultaneously different. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode as shown in Figure 53.

In this case, the baud rate is given by the formula

Modes 1 and 3 Baud Rate = (*Core Clk*)/
(32 × [65536 – (*RCAP2H*, *RCAP2L*)])

Table 28 shows some commonly used baud rates and how they could be calculated from a core clock frequency of 2.0971 MHz and 16.7772 MHz.

Table 28. Commonly Used Baud Rates, Timer 2

Ideal Baud	Core CLK	RCAP2H Value	RCAP2L Value	Actual Baud	% Error
19200	16.78	–1 (FFH)	–27 (E5H)	19418	1.14
9600	16.78	–1 (FFH)	–55 (C9H)	9532	0.7
2400	16.78	–1 (FFH)	–218 (26H)	2405	0.21
1200	16.78	–2 (FEH)	–181 (4BH)	1199	0.02
9600	2.10	–1 (FFH)	–7 (FBH)	9362	2.4
2400	2.10	–1 (FFH)	–27 (ECH)	2427	1.14
1200	2.10	–1 (FFH)	–55 (D7H)	1191	0.7

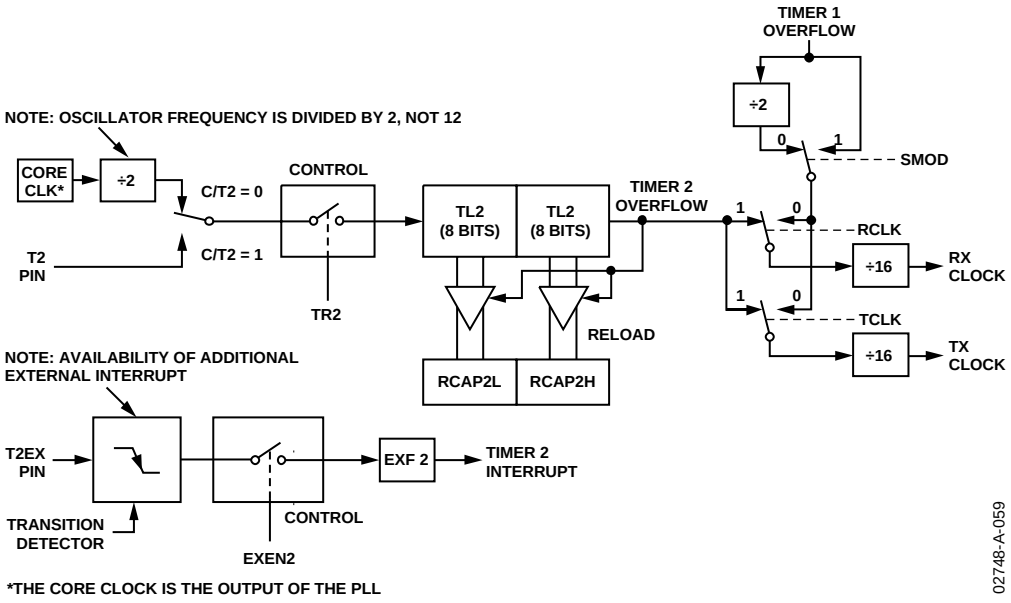

Figure 53. Timer 2, UART Baud Rates

Interrupt Priority

The interrupt enable registers are written by the user to enable individual interrupt sources, while the interrupt priority registers allow the user to select one of two priority levels for each interrupt. An interrupt of a high priority may interrupt the service routine of a low priority interrupt, and if two interrupts of different priority occur at the same time, the higher level interrupt is serviced first. An interrupt cannot be interrupted by another interrupt of the same priority level. If two interrupts of the same priority level occur simultaneously, a polling sequence is observed as shown in Table 32.

Table 32. Priority within an Interrupt Level

Source	Priority	Description
PSMI	1 (Highest)	Power Supply Monitor Interrupt
WDS	2	Watchdog Interrupt
IE0	3	External Interrupt 0
RDY0/RDY1	4	ADC Interrupt
TF0	5	Timer/Counter 0 Interrupt
IE1	6	External Interrupt 1
TF1	7	Timer/Counter 1 Interrupt
ISPI	8	SPI Interrupt
RI + TI	9	Serial Interrupt
TF2 + EXF2	10	Timer/Counter 2 Interrupt
TII	11 (Lowest)	Time Interval Counter Interrupt

Interrupt Vectors

When an interrupt occurs, the program counter is pushed onto the stack, and the corresponding interrupt vector address is loaded into the program counter. The interrupt vector addresses are shown in Table 33.

Table 33. Interrupt Vector Addresses

Source	Vector Address
IE0	0003H
TF0	000BH
IE1	0013H
TF1	001BH
RI + TI	0023H
TF2 + EXF2	002BH
RDY0/RDY1 (ADC)	0033H
ISPI	003BH
PSMI	0043H
TII	0053H
WDS (WDIR = 1)[1]	005BH

[1] The watchdog can be configured to generate an interrupt instead of a reset when it times out. This is used for logging errors or to examine the internal status of the microcontroller core to understand, from a software debug point of view, why a watchdog timeout occurred. The watchdog interrupt is slightly different from normal interrupts in that its priority level is always set to 1, and it is not possible to disable the interrupt via the global disable bit (EA) in the IE SFR. This is done to ensure that the interrupt is always responded to if a watchdog timeout occurs. The watchdog produces an interrupt only if the watchdog timeout is greater than zero.

Table 35. UART Timing (Shift Register Mode)

Parameter		16.78 MHz Core_Clk			Variable Core_Clk			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{XLXL}	Serial Port Clock Cycle Time		715			12 t_{CORE}		µs
t_{QVXH}	Output Data Setup to Clock	463			10 t_{CORE}	−133		ns
t_{DVXH}	Input Data Setup to Clock	252			2 t_{CORE}	+133		ns
t_{XHDX}	Input Data Hold after Clock	0			0			ns
t_{XHQX}	Output Data Hold after Clock	22			2 t_{CORE}	−117		ns

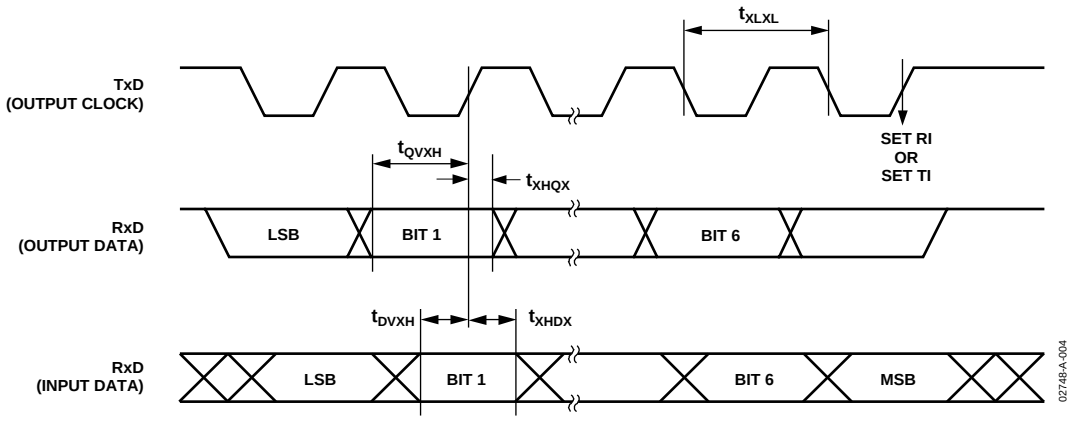

Figure 62. UART Timing in Shift Register Mode