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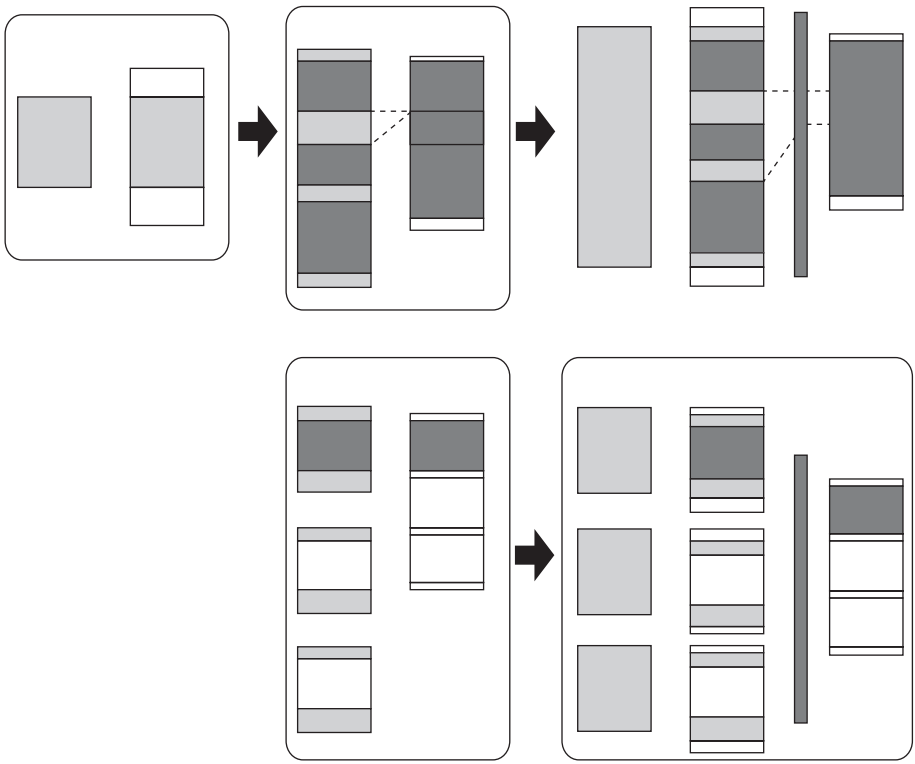
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Last Time Buy |
| Core Processor | SH-4A |
| Core Size | 32-Bit Single-Core |
| Speed | 266MHz |
| Connectivity | Audio Codec, I²C, Memory Card, SCI, SIM, SIO, SSI, USB |
| Peripherals | DMA, LCD, POR, WDT |
| Number of I/O | 107 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.15V ~ 1.35V |
| Data Converters | A/D 4x10b; D/A 2x8b |
| Oscillator Type | External |
| Operating Temperature | -20°C ~ 75°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 449-FBGA |
| Supplier Device Package | 449-FBGA (21x21) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5s77632ay266bgv |

| Pin No. | Pin Name | I/O | Function | Power Supply |
|---|---|---|---|---|
| Y3 | PTE0/INTA/PCC_DRV/ GET1_ETXD6/DREQ2 | IO/IO/O/O/I | Port/PCI interrupt/PCMCIA buffer control/GMII transmit data/DMA transfer request | VCCQ |
| Y4 | PTD7/PCIRESET/ PCC_RESET/GET1_ETXD7/ LCDM_VEPWC | O/O/O/O/O | Port/PCI reset/PCMCIA reset/GMII transmit data/LCD power supply control (mirror pin) | VCCQ |
| Y5 | VSS | | Internal GND | |
| Y21 | VCCQ | | I/O VCC | |
| Y22 | CE2A | O | PCMCIA select | VCCQ |
| Y23 | CE2B | O | PCMCIA select | VCCQ |
| Y24 | DA1 | O | Analog output | AVcc |
| Y25 | DA0 | O | Analog output | AVcc |
| AA1 | PTF1/REQ0/REQOUT/ SIM_CLK/ET1_MDC/DACK3 | IO/IO/O/O/O/O | Port/PCI bus mastership request (host)/PCI bus mastership request output/SIM clock output/ETHER management data clock/DMA transfer request acknowledge | VCCQ |
| AA2 | PTF2/AD31/SIM_RST/ ET1_MDIO/TEND3 | IO/IO/O/IO/O | Port/PCI address-and-data bus/SIM reset/ETHER management data IO/DMA transfer end | VCCQ |
| AA3 | PTG0/GND/ET1_WOL | IO/O/O | Port/PCI bus GND/ETHER wake on LAN | VCCQ |
| AA4 | PTG4/AD30/ET1_LINKSTA | IO/IO/I | Port/PCI address-and-data bus/ ETHER link status | VCCQ |
| AA5 | VSSQ | | I/O GND | |
| AA6 | VCCQ | | I/O VCC | |
| AA7 | VSSQ | | I/O GND | |
| AA8 | VCCQ | | I/O VCC | |
| AA9 | VDD | | Internal VDD | |



## 7.5 Cache Operation Instruction

### 7.5.1 Coherency between Cache and External Memory

Coherency between cache and external memory should be assured by software. In this LSI, the following six instructions are supported for cache operations. Details of these instructions are given in the Programming Manual.

€ Operand cache invalidate instruction: OCBI @Rn
Operand cache invalidation (no write-back)

€ Operand cache purge instruction: OCBP @Rn
Operand cache invalidation (with write-back)

€ Operand cache write-back instruction: OCBWB @Rn
Operand cache write-back

€ Operand cache allocate instruction: MOVCA.L R0,@Rn
Operand cache allocation

€

(PCIPINTM). Of the power management interrupts, the power state D0 interrupt (PCIPWD0) detects a transition from the power state D1/D2/D3 to D0, while power state D1 interrupt (PCIPWD1) detects a transition from the power state D0 to D1, while power state D2 interrupt (PCIPWD2) detects a transition from the power state D0/D1 to D2, while power state D3 interrupt (PCIPWD3) detects a transition from the power state D0/D1/D2 to D3. Interrupt masks can be set for each interrupt.

No power state D0 interrupt is generated at a power-on reset.

The following cautions should be noted when the PCIC is operating in normal mode and a power down interrupt is received from the host: In PCI power management, the PCI local bus clock stops within a minimum of 16 clocks after the host device has instructed a transition to power state D3. After detecting a power state D3 interrupt, do not, therefore, attempt to read or write to local registers and configuration registers that can be accessed from the SuperHyway bus and PCI local bus access (I/O and memory spaces). Because these accesses operate using the PCI local bus clock, the cycle for these accesses will not be completed if the clock stops and may be hung-up on the SuperHyway bus.

### 13.4.8 PCI Local Bus Basic Interface

The PCIC of this LSI conforms to the PCI local bus specification revision 2.2 stipulations and can be connected to a device with a PCI local bus interface. The following figures show the timing for each operation mode.

#### (1) Master Read/Write Cycle Timing

Figure 13.17 is an example of a single-write cycle in host bus bridge mode. Figure 13.18 is an example of a single read cycle in host bus bridge mode. Figure 13.19 is an example of a burst write cycle in normal mode. And Figure 13.20 is an example of a burst read cycle in normal mode. Note that the response speed of DEVSEL and TRDY differs according to the connected target device. In host bus bridge mode, master accesses always use single read/write cycles. The issuing of configuration transfers is only possible in host bus bridge mode.

To prevent a device that does not execute REQ negation and FRAME assertion simultaneously (figure 13.27) from being a bus master, preventive measure 1 or 2 below should be taken.

1. Use pseudo-round-robin mode.

   Pseudo-round-robin mode should be set (BMAM bit in PCICR = 1) as the PCI bus arbitration scheme.
2. Assign the lowest priority level to the relevant device.

   When there is only one device that does not execute REQ negation and FRAME assertion simultaneously, the device should be connected to the REQn and GNTn with the lowest priority.

However, if none of the external devices connected to the PCI has such negation/assertion timing or if none of the external devices with such negation/assertion timing can be a bus master, the above preventive measures are not required.

### 13.5.3 PCIC Master Access Parity Error Detection

When the PCIC executes a master read access, the PCIC may not detect the parity error.

[Condition]

When all the following conditions (1) and (2) are satisfied, the PCIC can not detect a data parity error. And then the PERR is not asserted, and PCIIR.MRDPEI is not set to 1 like the PCIC does not detect a data parity error.

(1) PCIC (master) condition

(1-1) PER bit in a PCI command register is set to 1. (Using parity error detection (PERR))

(1-2) PCI transaction: memory read access (single or burst)

(2) External PCI device (target) condition

(2-1) Target initiated disconnect (with data): STOP assert

[System problem]

When a target initiated disconnect (with data) occurs, the parity error for the disconnected data cycle can not be detected and the PERR is not asserted.

[Workaround]

There is no workaround by the PCIC.

### 14.5.7 DMA Transfer to DMAC Prohibited

Do not perform DMA transfer with the DMAC register specified as the transfer source or transfer destination.

### 14.5.8 NMI Interrupt

When an NMI interrupt occurs, the DMA transfer is stopped. After returning from the NMI interrupt routine, set all channels again, and then restart the DMA transfer.

### 14.5.9 Notice on Use of DMAC Burst Mode

When using burst mode of the DMAC (CHCRn.TB=1, n=0 to 5), if a manual reset occurs in either 1 or 2 conditions below, the DMAC will stall (then the SuperHyway bus of this LSI becomes bus lock state) and this LSI cannot change to the manual reset state. And then it is impossible to recover its state except a power-on reset. To avoid this problem, use the workaround shown below or use the cycle steal mode instead of the burst mode when a manual reset may occur during a burst transfer.

## 19.4 Operation

Each channel has a 32-bit timer counter (TCNT) and a 32-bit timer constant register (TCOR). Each TCNT performs count-down operation. The channels have an auto-reload function that allows cyclic count operations, and can also perform external event counting. Channel 2 also has an input capture function.

### 19.4.1 Counter Operation

When one of bits STR0 to STR2 in TSTR is set to 1, the TCNT for the corresponding channel starts counting. When TCNT underflows, the UNF flag in TCR is set. If the UNIE bit in TCR is set to 1 at this time, an interrupt request is sent to the CPU. At the same time, the value is copied from TCOR into TCNT, and the count-down continues (auto-reload function).

#### (1) Example of Count Operation Setting Procedure

Figure 19.2 shows an example of the count operation setting procedure.

| Name | Abbreviation | Power-On Reset | Manual Reset | Sleep | Standby |
|---|---|---|---|---|---|
| CAM entry table 18H register | TSU_ ADRH18 | H'00000000 | H'00000000 | Retained | Retained |
| CAM entry table 19H register | TSU_ ADRH19 | H'00000000 | H'00000000 | Retained | Retained |
| CAM entry table 20H register | TSU_ ADRH20 | H'00000000 | H'00000000 | Retained | Retained |
| CAM entry table 21H register | TSU_ ADRH21 | H'00000000 | H'00000000 | Retained | Retained |
| CAM entry table 22H register | TSU_ ADRH22 | H'00000000 | H'00000000 | Retained | Retained |
| CAM entry table 23H register | TSU_ ADRH23 | H'00000000 | H'00000000 | Retained | Retained |
| CAM entry table 24H register | TSU_ ADRH24 | H'00000000 | H'00000000 | Retained | Retained |
| CAM entry table 25H register | TSU_ ADRH25 | H'00000000 | H'00000000 | Retained | Retained |
| CAM entry table 26H register | TSU_ ADRH26 | H'00000000 | H'00000000 | Retained | Retained |
| CAM entry table 27H register | TSU_ ADRH27 | H'00000000 | H'00000000 | Retained | Retained |
| CAM entry table 28H register | TSU_ ADRH28 | H'00000000 | H'00000000 | Retained | Retained |
| CAM entry table 29H register | TSU_ ADRH29 | H'00000000 | H'00000000 | Retained | Retained |
| CAM entry table 30H register | TSU_ ADRH30 | H'00000000 | H'00000000 | Retained | Retained |
| CAM entry table 31H register | TSU_ ADRH31 | H'00000000 | H'00000000 | Retained | Retained |
| CAM entry table 0L register | TSU_ADRL0 | H'00000000 | H'00000000 | Retained | Retained |
| CAM entry table 1L register | TSU_ADRL1 | H'00000000 | H'00000000 | Retained | Retained |
| CAM entry table 2L register | TSU_ADRL2 | H'00000000 | H'00000000 | Retained | Retained |
| CAM entry table 3L register | TSU_ADRL3 | H'00000000 | H'00000000 | Retained | Retained |
| CAM entry table 4L register | TSU_ADRL4 | H'00000000 | H'00000000 | Retained | Retained |
| CAM entry table 5L register | TSU_ADRL5 | H'00000000 | H'00000000 | Retained | Retained |
| CAM entry table 6L register | TSU_ADRL6 | H'00000000 | H'00000000 | Retained | Retained |

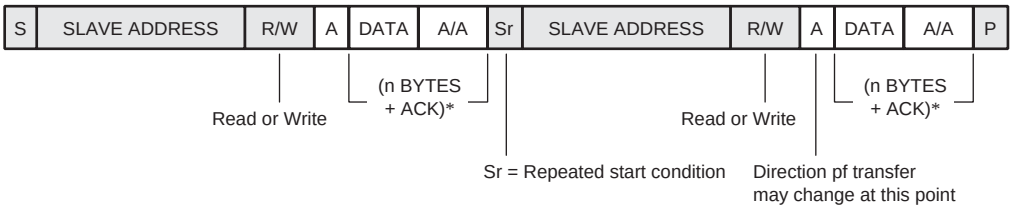
### 23.3.38 Receive/Relay Function Set Register (Port 1 to 0) (TSU_FWSL1)

TSU_FWSL1 sets the processing method (enable or disable relay operation) of each frame in port 1 reception and port 1 to 0 relay operations. For multicast frames and frames whose destinations are other than this LSI, the processing method in relay operations can be determined by referring to the CAM evaluation results. (For details, refer to section 23.4.5, CAM Function.) This register must not be written to once after relay operations have been enabled (after the FWEN0 bit in TSU_FWEN0 or the FWEN1 bit in TSU_FWEN1 is set to 1).

| Bit: | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

| Bit: | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | — | — | FW51 | FW41 | FW31 | FW21 | FW11 | — | — | — | RMSA1 | — | — | — | — |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R | R | R | R/W | R/W | R/W | R/W | R/W | R | R | R | R/W | R | R | R | R |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 31 to 13 | — | All 0 | R | Reserved<br>These bits are always read as 0. The write value should always be 0. |
| 12 | FW51 | 0 | R/W | Sets the processing method when frames from port 1 are MAC control frames.<br>0: Frames are not relayed<br>1: Frames are relayed to port 0 |
| 11 | FW41 | 0 | R/W | Sets the processing method when frames from port 1 are addressed to this LSI.<br>0: Frames are not relayed<br>1: Frames are relayed to port 0 |
| 10 | FW31 | 0 | R/W | Sets the processing method when frames from port 1 are Broadcast frames.<br>0: Frames are not relayed<br>1: Frames are relayed to port 0 |




Notes: 1. Tramsfer dorection of data and acknowledge bits depends on R/W bits.
2. Repeated START condition: Tramsfer is started whrn the IIC_SCL signal is driven high and the IIC_SDA signal is driven low.

**Figure 26.5 Combination Transfer Format of Master Transfer**

### 26.4.7 10-Bit Address Format

Description is given below on the 10-bit address transfer format supported in master mode.

This format has three transfer methods as the 7-bit address transfer format.

Figure 26.6 shows the data transmit format. The set value in the master address register is output in one byte following the first START condition (S). The value set in the transmit data register (TXD) is transmitted as a slave address in the second byte. Data on and after the third byte is transferred in the same way as the 7-bit address data.

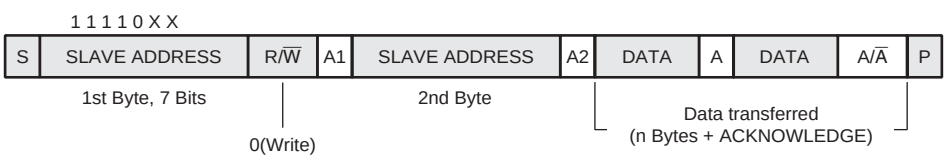



**Figure 26.6 10-Bit Address Data Transmit Format**

Figure 26.7 shows the data receive format. Two bytes of an address is transmitted a repeated START in the same way as in the data transmit format. Then, repeated START condition (Sr) is transmitted and the value set in the address register is output. At this time, STM1 must be set to 1 (receive mode). Data is transferred in the same way as in the 7-bit address data receive format.

3. Reset the MDE bit.

   Clear MDE after setting the last byte to be transmitted. After the last byte data is transmitted, MDE is generated. To clear the MDE, you must set the master control register to H'8A.

   (Set the force stop control bit).

**(5) Wait for End of Transmission**

1. Wait for the master event, MST in the master status register.
2. Reset the MST bit after confirming MNR (Master NACK Received).

### 26.5.2 Master Receiver

To set up the master interface to receive a data packet on the I²C bus, follow the following procedure:

**(1) Load Clock Control Register**

1. SCL clock generation divider (SCGD) = H'03

   (SCL frequency of 400 kHz).
2. Clock division ratio (CDF) = H'3

   (The peripheral clock is 66.7 MHz and the IIC's internal clock IICck is 16.7 MHz.)

**(2) Load Master Control Register and Address**

1. Set master address register to address of slave being accessed and STM1 bit (read mode: 1).
2. Set master control register to H'89

   (MDBS = 1, MIE = 1, ESG = 1).

**(3) Wait for Outputting Address**

1. Wait for master event (an interrupt of the MAT and MDR bits in the master status register).
2. Set the master control register to H'88

   (To suspend the data transmission, the master device will hold the SCL low until the MDR bit is cleared).

   If only one byte of data is received, set the master control register to H'8A, meaning that the stop generation is enabled. This generates a stop on the bus as soon as one byte has been received.
3. Reset the MAT bit.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 5, 4 | — | All 0 | R | Reserved<br>These bits are always read as 0. The write value should always be 0. |
| 3 to 0 | TDRA[3:0] | 0000 | R/W | Transmit Right-Channel Data Assigns 3 to 0<br>Specify the position of right-channel data in a transmit frame as B'0000 (0) to B'1110 (14).<br>1111: Setting prohibited<br>• Transmit data for the right channel is specified in the SITDR bit in SITDR. |

### 29.3.12 Receive Data Assign Register (SIRDAR)

SIRDAR is a 16-bit readable/writable register that specifies the position of the receive data in a frame.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

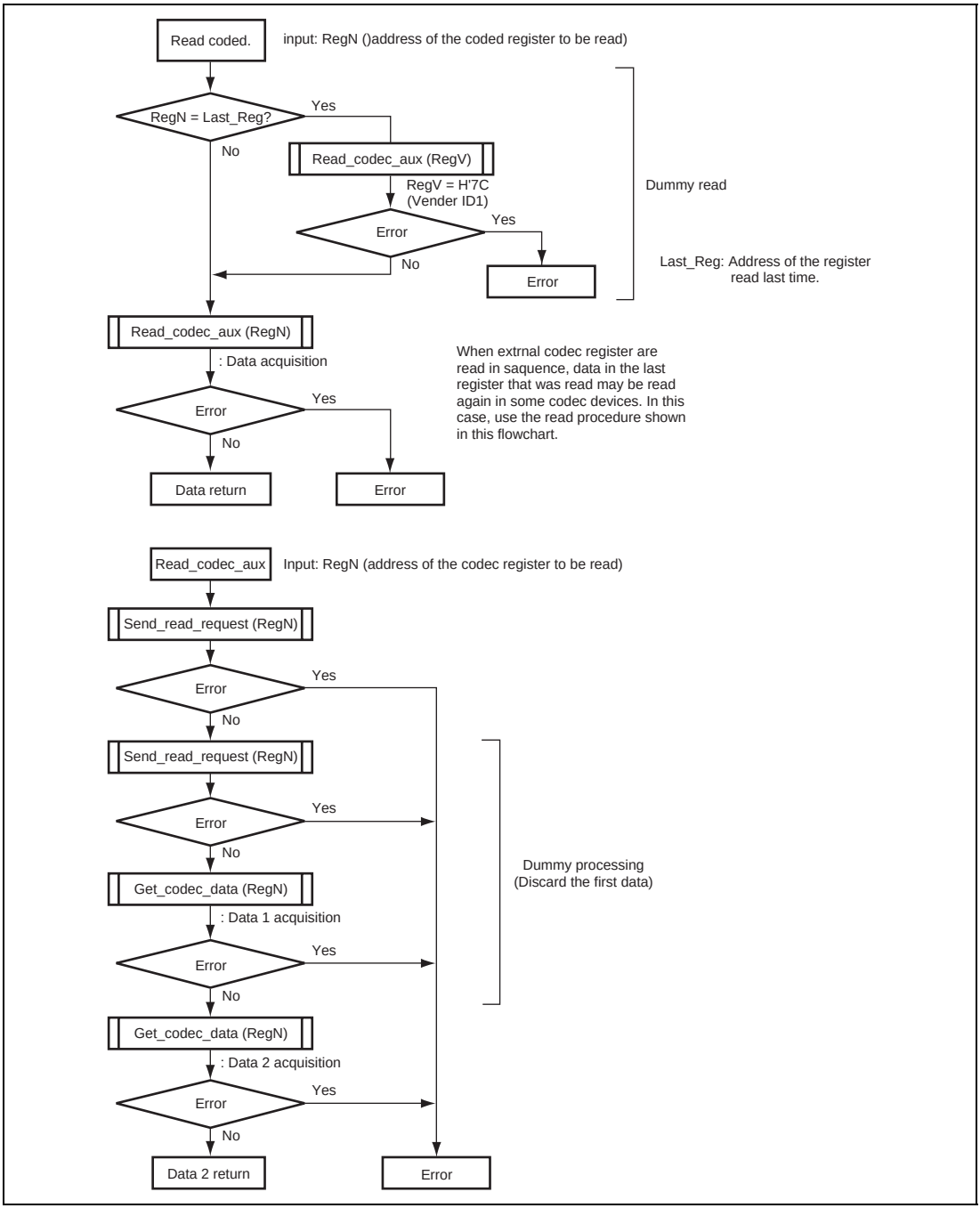



**Figure 33.5 Sample Flowchart for Off-Chip Codec Register Read (1)**

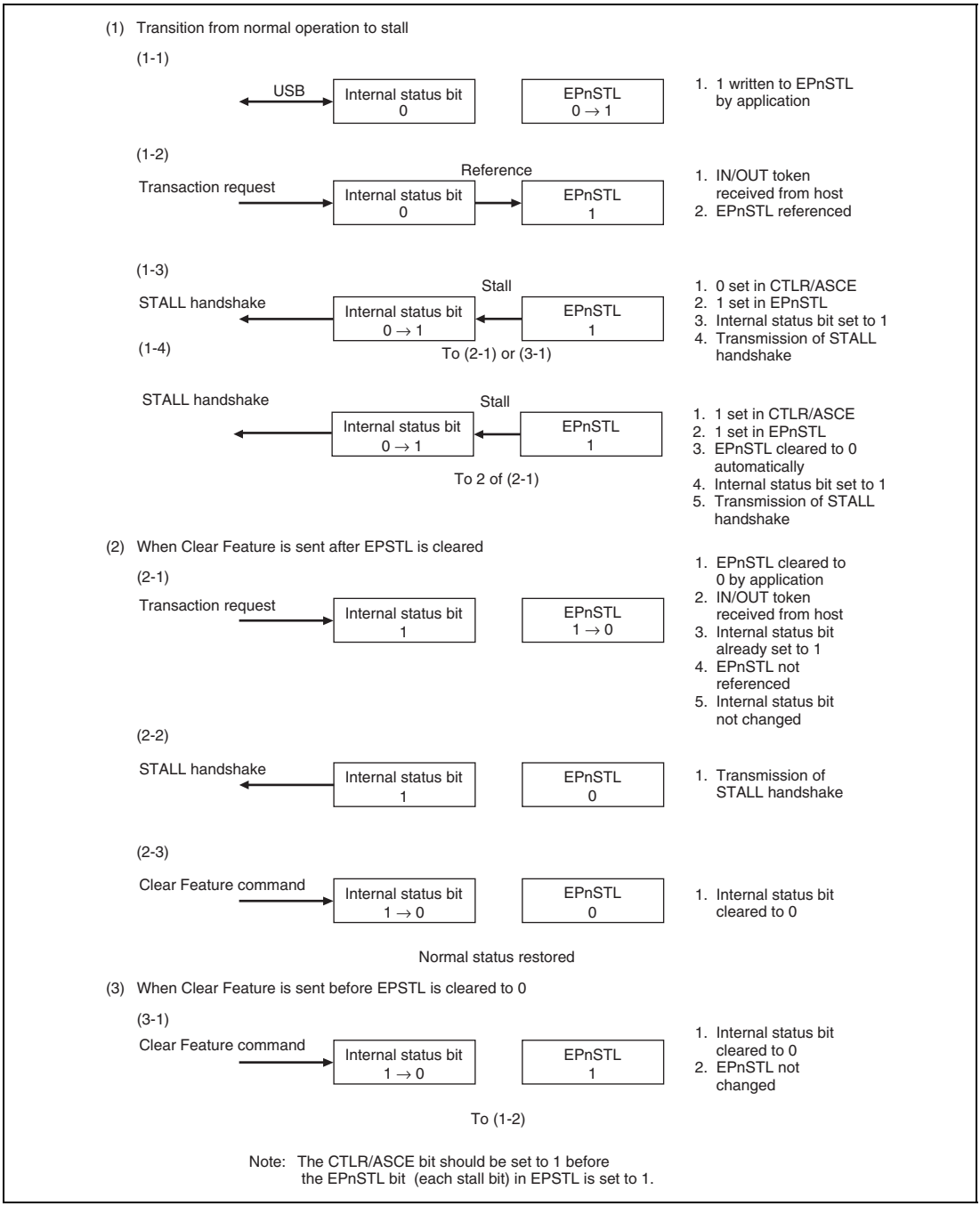



**Figure 36.17 Forcible Stall by Application**

### 40.2.16 Port A Data Register (PADR)

PADR is an 8-bit readable/writable register that stores port A data.

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | — | PA6DT | PA5DT | PA4DT | PA3DT | PA2DT | PA1DT | PA0DT |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Bit Name | Initial value | R/W | Description |
|---|---|---|---|---|
| 7 | — | 0 | R | Reserved<br>This bit is always read as 0. The write value should always be 0. |
| 6 | PA6DT | 0 | R/W | Each of these bits stores output data for the corresponding pin that is used as a general output port. If the port is read, the value of the corresponding bit in this register will be read for a pin configured as a general output port, while the state of the corresponding pin will be read for a pin configured as a general input port. |
| 5 | PA5DT | 0 | R/W | |
| 4 | PA4DT | 0 | R/W | |
| 3 | PA3DT | 0 | R/W | |
| 2 | PA2DT | 0 | R/W | |
| 1 | PA1DT | 0 | R/W | |
| 0 | PA0DT | 0 | R/W | |

### 40.2.37 Port O Pull-Up Control Register (POPUPR)

POPUPR is an 8-bit readable/writable register. Each bit of this register corresponds to PTO7 to PTO0, and when the pins of Port O are used by “other function”, pull-up control is performed for the individual pins. The settings in this register are invalid for the pins specified to function as port pins by POCR.

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | — | — | PO5PUPR | PO4PUPR | PO3PUPR | PO2PUPR | PO1PUPR | PO0PUPR |
| Initial value: | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| R/W: | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Bit Name | Initial value | R/W | Description |
|---|---|---|---|---|
| 7 | — | All 1 | R | Reserved |
| 6 | | | | These bits are always read as 1, and the write value should always be 1. |
| 5 | PO5PUPR | 1 | R/W | Controls pull-up of the PTO5 pin<br>0: PTO5 pin pull-up off<br>1: PTO5 pin pull-up on |
| 4 | PO4PUPR | 1 | R/W | Controls pull-up of the PTO4 pin<br>0: PTO4 pin pull-up off<br>1: PTO4 pin pull-up on |
| 3 | PO3PUPR | 1 | R/W | Controls pull-up of the PTO3 pin<br>0: PTO3 pin pull-up off<br>1: PTO3 pin pull-up on |
| 2 | PO2PUPR | 1 | R/W | Controls pull-up of the PTO2 pin<br>0: PTO2 pin pull-up off<br>1: PTO2 pin pull-up on |
| 1 | PO1PUPR | 1 | R/W | Controls pull-up of the PTO1 pin<br>0: PTO1 pin pull-up off<br>1: PTO1 pin pull-up on |
| 0 | PO0PUPR | 1 | R/W | Controls pull-up of the PTO0 pin<br>0: PTO0 pin pull-up off<br>1: PTO0 pin pull-up on |