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Application specific microcontrollers are engineered to

Details

Product Status	Active
Applications	USB Microcontroller
Core Processor	8051
Program Memory Type	ROMless
Controller Series	CY7C647xx
RAM Size	16K x 8
Interface	I ² C, USB, USART
Number of I/O	40
Voltage - Supply	3.15V ~ 3.45V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c64713-100axc

Table 3. INT2 USB Interrupts (continued)

USB INTERRUPT TABLE FOR INT2			
Priority	INT2VEC Value	Source	Notes
18	44		Reserved
19	48	EP0PING	EP0 OUT was Pinged and it NAK'd
20	4C	EP1PING	EP1 OUT was Pinged and it NAK'd
21	50	EP2PING	EP2 OUT was Pinged and it NAK'd
22	54	EP4PING	EP4 OUT was Pinged and it NAK'd
23	58	EP6PING	EP6 OUT was Pinged and it NAK'd
24	5C	EP8PING	EP8 OUT was Pinged and it NAK'd
25	60	ERRLIMIT	Bus errors exceeded the programmed limit
26	64		
27	68		Reserved
28	6C		Reserved
29	70	EP2ISOERR	ISO EP2 OUT PID sequence error
30	74	EP4ISOERR	ISO EP4 OUT PID sequence error
31	78	EP6ISOERR	ISO EP6 OUT PID sequence error
32	7C	EP8ISOERR	ISO EP8 OUT PID sequence error

Table 4. Individual FIFO/GPIF Interrupt Sources

Priority	INT4VEC Value	Source	Notes
1	80	EP2PF	Endpoint 2 Programmable Flag
2	84	EP4PF	Endpoint 4 Programmable Flag
3	88	EP6PF	Endpoint 6 Programmable Flag
4	8C	EP8PF	Endpoint 8 Programmable Flag
5	90	EP2EF	Endpoint 2 Empty Flag ^[3]
6	94	EP4EF	Endpoint 4 Empty Flag
7	98	EP6EF	Endpoint 6 Empty Flag
8	9C	EP8EF	Endpoint 8 Empty Flag
9	A0	EP2FF	Endpoint 2 Full Flag
10	A4	EP4FF	Endpoint 4 Full Flag
11	A8	EP6FF	Endpoint 6 Full Flag
12	AC	EP8FF	Endpoint 8 Full Flag
13	B0	GPIFDONE	GPIF Operation Complete
14	B4	GPIFWF	GPIF Waveform

If Autovectoring is enabled (AV4EN = 1 in the INTSETUP register), the FX1 substitutes its INT4VEC byte. Therefore, if the high byte ("page") of a jump-table address is preloaded at location 0x0054, the automatically inserted INT4VEC byte at 0x0055 directs the jump to the correct address out of the 14 addresses within the page. When the ISR occurs, the FX1

pushes the program counter onto its stack and then jumps to address 0x0053, where it expects to find a "jump" instruction to the ISR Interrupt service routine.

Note

3. **Errata:** In Slave FIFO Asynchronous Word Wide mode, if a single word data is transferred from the USB host to EP2, configured as OUT Endpoint (EP) in the first transaction, then the Empty flag behaves incorrectly. This does not happen if the data size is more than one word in the first transaction. For more information, see the "Errata" on page 71.

Program/Data RAM

Size

The FX1 has 16 KBytes of internal program/data RAM, where PSEN#/RD# signals are internally ORed to allow the 8051 to access it as both program and data memory. No USB control registers appear in this space.

Two memory maps are shown in the following diagrams:

- [Figure 3 on page 9](#) Internal Code Memory, EA = 0
- [Figure 4 on page 10](#) External Code Memory, EA = 1.

Internal Code Memory, EA = 0

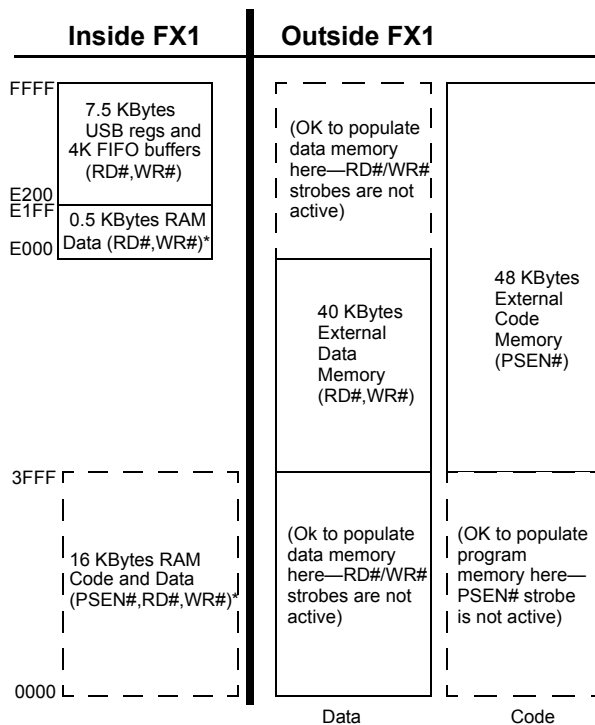
This mode implements the internal 16 KByte block of RAM (starting at 0) as combined code and data memory. When the

external RAM or ROM is added, the external read and write strobes are suppressed for memory spaces that exist inside the chip. This allows the user to connect a 64 KByte memory without requiring the address decodes to keep clear of internal memory spaces.

Only the **internal** 16 KBytes and **scratch pad** 0.5 KBytes RAM spaces have the following access:

- USB download
- USB upload
- Setup data pointer
- I²C interface boot load

Figure 3. Internal Code Memory, EA = 0.



*SUDPTR, USB upload/download, I²C interface boot access

Figure 9. CY7C64713 100-pin TQFP Pin Assignment

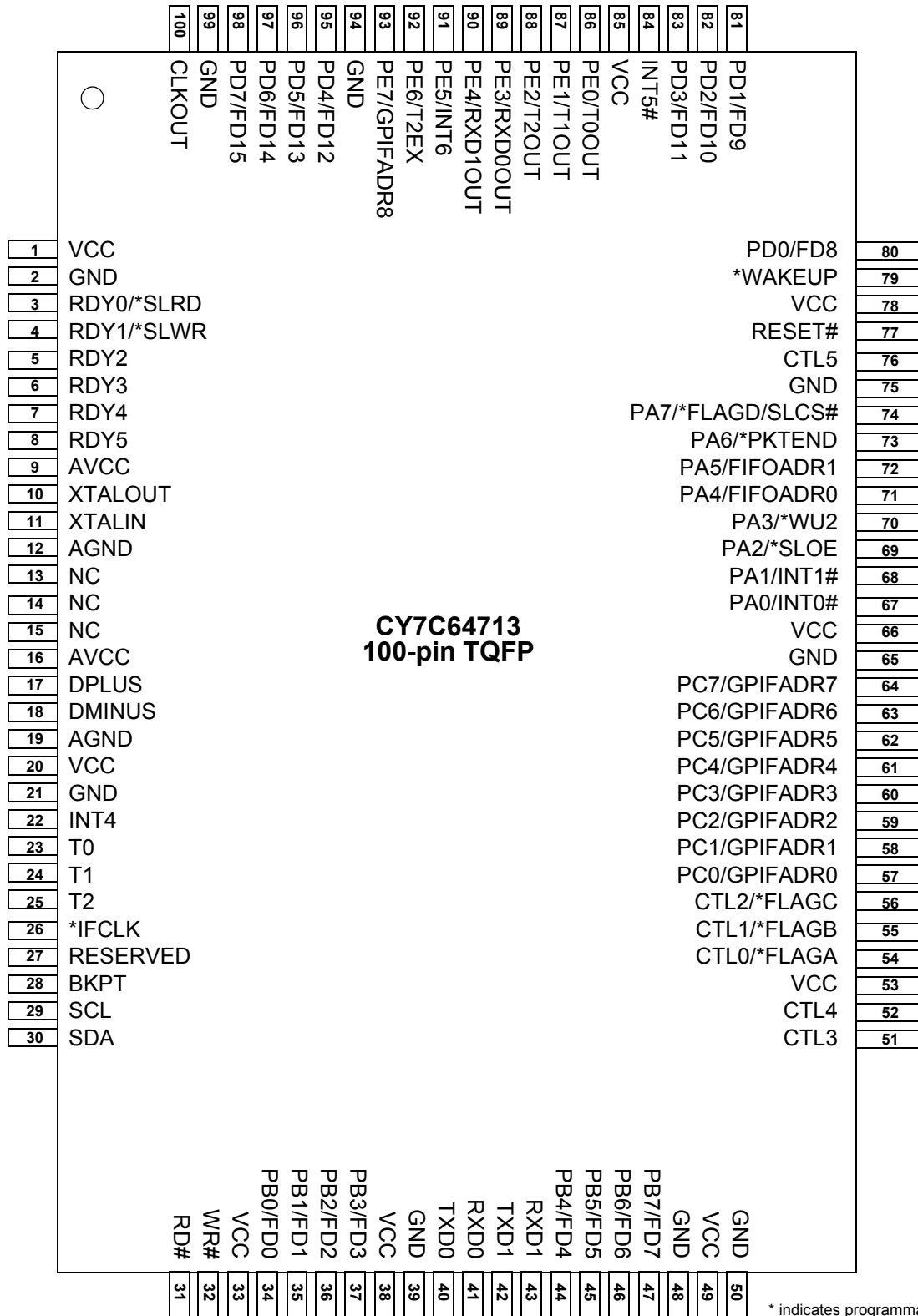


Table 8. FX1 Pin Definitions (continued)

128-pin TQFP	100-pin TQFP	56-pin SSOP	56-pin QFN	Name	Type	Default	Description
89	71	44	37	PA4 or FIFOADR0	I/O/Z	I (PA4)	Multiplexed pin whose function is selected by: IFCONFIG[1..0]. PA4 is a bidirectional I/O port pin. FIFOADR0 is an input-only address select for the slave FIFOs connected to FD[7..0] or FD[15..0].
90	72	45	38	PA5 or FIFOADR1	I/O/Z	I (PA5)	Multiplexed pin whose function is selected by: IFCONFIG[1..0]. PA5 is a bidirectional I/O port pin. FIFOADR1 is an input-only address select for the slave FIFOs connected to FD[7..0] or FD[15..0].
91	73	46	39	PA6 or PKTEND	I/O/Z	I (PA6)	Multiplexed pin whose function is selected by the IFCONFIG[1:0] bits. PA6 is a bidirectional I/O port pin. PKTEND is an input used to commit the FIFO packet data to the endpoint and whose polarity is programmable via FIFOPINPOLAR.5.
92	74	47	40	PA7 or FLAGD or SLCS#	I/O/Z	I (PA7)	Multiplexed pin whose function is selected by the IFCONFIG[1:0] and PORTACFG.7 bits. PA7 is a bidirectional I/O port pin. FLAGD is a programmable slave-FIFO output status flag signal. SLCS# gates all other slave FIFO enable/strobes
Port B							
44	34	25	18	PB0 or FD[0]	I/O/Z	I (PB0)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. PB0 is a bidirectional I/O port pin. FD[0] is the bidirectional FIFO/GPIF data bus.
45	35	26	19	PB1 or FD[1]	I/O/Z	I (PB1)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. PB1 is a bidirectional I/O port pin. FD[1] is the bidirectional FIFO/GPIF data bus.
46	36	27	20	PB2 or FD[2]	I/O/Z	I (PB2)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. PB2 is a bidirectional I/O port pin. FD[2] is the bidirectional FIFO/GPIF data bus.
47	37	28	21	PB3 or FD[3]	I/O/Z	I (PB3)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. PB3 is a bidirectional I/O port pin. FD[3] is the bidirectional FIFO/GPIF data bus.
54	44	29	22	PB4 or FD[4]	I/O/Z	I (PB4)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. PB4 is a bidirectional I/O port pin. FD[4] is the bidirectional FIFO/GPIF data bus.
55	45	30	23	PB5 or FD[5]	I/O/Z	I (PB5)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. PB5 is a bidirectional I/O port pin. FD[5] is the bidirectional FIFO/GPIF data bus.
56	46	31	24	PB6 or FD[6]	I/O/Z	I (PB6)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. PB6 is a bidirectional I/O port pin. FD[6] is the bidirectional FIFO/GPIF data bus.

Table 8. FX1 Pin Definitions *(continued)*

128-pin TQFP	100-pin TQFP	56-pin SSOP	56-pin QFN	Name	Type	Default	Description
49	39			GND	Ground	N/A	Ground.
58	48	33	26	GND	Ground	N/A	Ground.
65	50	35	28	GND	Ground	N/A	Ground.
80	65			GND	Ground	N/A	Ground.
93	75	48	41	GND	Ground	N/A	Ground.
116	94			GND	Ground	N/A	Ground.
125	99	4	53	GND	Ground	N/A	Ground.
14	13			NC	N/A	N/A	No Connect. This pin must be left open.
15	14			NC	N/A	N/A	No Connect. This pin must be left open.
16	15			NC	N/A	N/A	No Connect. This pin must be left open.

Register Summary

FX1 register bit definitions are described in the [EZ-USB TRM](#) in greater detail.

Table 9. FX1 Register Summary

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
GPIF Waveform Memories													
E400	128	WAVEDATA	GPIF Waveform Descriptor 0, 1, 2, 3 data	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E480	128	reserved											
GENERAL CONFIGURATION													
E600	1	CPUCS	CPU Control & Status	0	0	PORTCSTB	CLKSPD1	CLKSPD0	CLKINV	CLKOE	8051RES	00000010	rrbbbbb
E601	1	IFCONFIG	Interface Configuration (Ports, GPIF, slave FIFOs)	IFCLKSRC	3048MHZ	IFCLKOE	IFCLKPOL	ASYN	GSTATE	IFCFG1	IFCFG0	10000000	RW
E602	1	PINFLAGSAB ^[8]	Slave FIFO FLAGA and FLAGB Pin Configuration	FLAGB3	FLAGB2	FLAGB1	FLAGB0	FLAGA3	FLAGA2	FLAGA1	FLAGA0	00000000	RW
E603	1	PINFLAGSCD ^[8]	Slave FIFO FLAGC and FLAGD Pin Configuration	FLAGD3	FLAGD2	FLAGD1	FLAGD0	FLAGC3	FLAGC2	FLAGC1	FLAGC0	00000000	RW
E604	1	FIFORESET ^[8]	Restore FIFOs to default state	NAKALL	0	0	0	EP3	EP2	EP1	EP0	xxxxxxxx	W
E605	1	BREAKPT	Breakpoint Control	0	0	0	0	BREAK	BPPULSE	BPEN	0	00000000	rrrrbb
E606	1	BPADDRH	Breakpoint Address H	A15	A14	A13	A12	A11	A10	A9	A8	xxxxxxxx	RW
E607	1	BPADDRL	Breakpoint Address L	A7	A6	A5	A4	A3	A2	A1	A0	xxxxxxxx	RW
E608	1	UART230	230 Kbaud internally generated ref. clock	0	0	0	0	0	0	230UART1	230UART0	00000000	rrrrrrbb
E609	1	FIFOPINPOLAR ^[8]	Slave FIFO Interface pins polarity	0	0	PKTEND	SLOE	SLRD	SLWR	EF	FF	00000000	rrbbbbb
E60A	1	REVID	Chip Revision	rv7	rv6	rv5	rv4	rv3	rv2	rv1	rv0	RevA 00000001	R
E60B	1	REVCTL ^[8]	Chip Revision Control	0	0	0	0	0	0	dyn_out	enh_pkt	00000000	rrrrrrbb

Note

8. Read and writes to these register may require synchronization delay, see the section "Synchronization Delay" in the [EZ-USB TRM](#).

Table 9. FX1 Register Summary *(continued)*

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
		UDMA											
E60C	1	GPIFHOLDAMOUNT	MSTB Hold Time (for UDMA)	0	0	0	0	0	0	HOLDTIME1	HOLDTIME0	00000000	rrrrrrbb
	3	reserved											
		ENDPOINT CONFIGURATION											
E610	1	EP1OUTCFG	Endpoint 1-OUT Configuration	VALID	0	TYPE1	TYPE0	0	0	0	0	10100000	brbbrrrr
E611	1	EP1INCFG	Endpoint 1-IN Configuration	VALID	0	TYPE1	TYPE0	0	0	0	0	10100000	brbbrrrr
E612	1	EP2CFG	Endpoint 2 Configuration	VALID	DIR	TYPE1	TYPE0	SIZE	0	BUF1	BUF0	10100010	bbbbbrbb
E613	1	EP4CFG	Endpoint 4 Configuration	VALID	DIR	TYPE1	TYPE0	0	0	0	0	10100000	bbbbrrrr
E614	1	EP6CFG	Endpoint 6 Configuration	VALID	DIR	TYPE1	TYPE0	SIZE	0	BUF1	BUF0	11100010	bbbbbrbb
E615	1	EP8CFG	Endpoint 8 Configuration	VALID	DIR	TYPE1	TYPE0	0	0	0	0	11100000	bbbbrrrr
	2	reserved											
E618	1	EP2FIFOCFG ^[9]	Endpoint 2 / slave FIFO configuration	0	INFM1	OEP1	AUTOOUT	AUTOIN	ZEROLENIN	0	WORDWIDE	00000101	rbbbbbrb
E619	1	EP4FIFOCFG ^[9]	Endpoint 4 / slave FIFO configuration	0	INFM1	OEP1	AUTOOUT	AUTOIN	ZEROLENIN	0	WORDWIDE	00000101	rbbbbbrb
E61A	1	EP6FIFOCFG ^[9]	Endpoint 6 / slave FIFO configuration	0	INFM1	OEP1	AUTOOUT	AUTOIN	ZEROLENIN	0	WORDWIDE	00000101	rbbbbbrb
E61B	1	EP8FIFOCFG ^[9]	Endpoint 8 / slave FIFO configuration	0	INFM1	OEP1	AUTOOUT	AUTOIN	ZEROLENIN	0	WORDWIDE	00000101	rbbbbbrb
E61C	4	reserved											
E620	1	EP2AUTOINLENH ^[9]	Endpoint 2 AUTOIN Packet Length H	0	0	0	0	0	PL10	PL9	PL8	00000010	rrrrrrbb
E621	1	EP2AUTOINLENL ^[9]	Endpoint 2 AUTOIN Packet Length L	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00000000	RW

Note

9. Read and writes to these register may require synchronization delay, see the section "Synchronization Delay" in the [EZ-USB TRM](#).

Table 9. FX1 Register Summary *(continued)*

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E630	1	EP2FIFOPFH ^[11]	Endpoint 2 / slave FIFO Programmable Flag H ISO Mode	DECIS	PKTSTAT	IN: PKTS[2] OUT:PFC12	IN: PKTS[1] OUT:PFC11	IN: PKTS[0] OUT:PFC10	0	PFC9	PFC8	10001000	bbbbbrbb
E630	1	EP2FIFOPFH ^[11]	Endpoint 2 / slave FIFO Programmable Flag H Non-ISO Mode	DECIS	PKTSTAT	OUT:PFC12	OUT:PFC11	OUT:PFC10	0	PFC9	IN:PKTS[2] OUT:PFC8	10001000	bbbbbrbb
E631	1	EP2FIFOPFL ^[11]	Endpoint 2 / slave FIFO Programmable Flag L	IN:PKTS[1] OUT:PFC7	IN:PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E632	1	EP4FIFOPFH ^[11]	Endpoint 4 / slave FIFO Programmable Flag H ISO Mode	DECIS	PKTSTAT	0	IN: PKTS[1] OUT:PFC10	IN: PKTS[0] OUT:PFC9	0	0	PFC8	10001000	bbrbrrbb
E632	1	EP4FIFOPFH ^[11]	Endpoint 4 / slave FIFO Programmable Flag H Non-ISO Mode	DECIS	PKTSTAT	0	OUT:PFC10	OUT:PFC9	0	0	PFC8	10001000	bbrbrrbb
E633	1	EP4FIFOPFL ^[11]	Endpoint 4 / slave FIFO Programmable Flag L	IN: PKTS[1] OUT:PFC7	IN: PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E634	1	EP6FIFOPFH ^[11]	Endpoint 6 / slave FIFO Programmable Flag H ISO Mode	DECIS	PKTSTAT	INPKTS[2] OUT:PFC12	IN: PKTS[1] OUT:PFC11	IN: PKTS[0] OUT:PFC10	0	PFC9	PFC8	00001000	bbbbbrbb
E634	1	EP6FIFOPFH ^[11]	Endpoint 6 / slave FIFO Programmable Flag H Non-ISO Mode	DECIS	PKTSTAT	OUT:PFC12	OUT:PFC11	OUT:PFC10	0	PFC9	IN:PKTS[2] OUT:PFC8	00001000	bbbbbrbb

Note

11. Read and writes to these register may require synchronization delay, see the section "Synchronization Delay" in the [EZ-USB TRM](#).

Table 9. FX1 Register Summary *(continued)*

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E651	1	EP2FIFOIRQ ^[13, 14]	Endpoint 2 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000111	rrrrbbb
E652	1	EP4FIFOIE ^[14]	Endpoint 4 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW
E653	1	EP4FIFOIRQ ^[13, 14]	Endpoint 4 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000111	rrrrbbb
E654	1	EP6FIFOIE ^[14]	Endpoint 6 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW
E655	1	EP6FIFOIRQ ^[15, 16]	Endpoint 6 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000110	rrrrbbb
E656	1	EP8FIFOIE ^[16]	Endpoint 8 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW
E657	1	EP8FIFOIRQ ^[13, 14]	Endpoint 8 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000110	rrrrbbb
E658	1	IBNIE	IN-BULK-NAK Interrupt Enable	0	0	EP8	EP6	EP4	EP2	EP1	EP0	00000000	RW
E659	1	IBNIRQ ^[13]	IN-BULK-NAK interrupt Request	0	0	EP8	EP6	EP4	EP2	EP1	EP0	00xxxxx	rrbbbbbb
E65A	1	NAKIE	Endpoint Ping-NAK / IBN Interrupt Enable	EP8	EP6	EP4	EP2	EP1	EP0	0	IBN	00000000	RW
E65B	1	NAKIRQ ^[13]	Endpoint Ping-NAK / IBN Interrupt Request	EP8	EP6	EP4	EP2	EP1	EP0	0	IBN	xxxxxx0x	bbbbbbbrb

Notes

13. SFRs not part of the standard 8051 architecture.

 14. Read and writes to these register may require synchronization delay, see the section "Synchronization Delay" in the [EZ-USB TRM](#).

Table 9. FX1 Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E671	1	PORTCCFG	I/O PORTC Alternate Configuration	GPIFA7	GPIFA6	GPIFA5	GPIFA4	GPIFA3	GPIFA2	GPIFA1	GPIFA0	00000000	RW
E672	1	PORTECFG	I/O PORTE Alternate Configuration	GPIFA8	T2EX	INT6	RXD1OUT	RXD0OUT	T2OUT	T1OUT	T0OUT	00000000	RW
E673	4	XTALINSRC	XTALIN Clock Source	0	0	0	0	0	0	0	EXTCLK	00000000	rrrrrrrb
E677	1	reserved											
E678	1	I2CS	I ² C Bus Control & Status	START	STOP	LASTRD	ID1	ID0	BERR	ACK	DONE	000xx000	bbbrrrrr
E679	1	I2DAT	I ² C Bus Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW
E67A	1	I2CTL	I ² C Bus Control	0	0	0	0	0	0	STOPIE	400KHZ	00000000	RW
E67B	1	XAUTODAT1	Autopt1 MOVX access, when APTREN = 1	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E67C	1	XAUTODAT2	Autopt2 MOVX access, when APTREN = 1	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
		UDMA CRC											
E67D	1	UDMACRCH ^[17]	UDMA CRC MSB	CRC15	CRC14	CRC13	CRC12	CRC11	CRC10	CRC9	CRC8	01001010	RW
E67E	1	UDMACRCL ^[17]	UDMA CRC LSB	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0	10111010	RW
E67F	1	UDMACRC-QUALIFIER	UDMA CRC Qualifier	QENABLE	0	0	0	QSTATE	QSIGNA2	QSIGNA1	QSIGNA0	00000000	brrrbbbb
		USB CONTROL											
E680	1	USBCS	USB Control & Status	0	0	0	0	DISCON	NOSYNF	RENUM	SIGRSUM	x0000000	rrrrbbbb
E681	1	SUSPEND	Put chip into suspend	x	x	x	x	x	x	x	x	xxxxxxxx	W
E682	1	WAKEUPCS	Wakeup Control & Status	WU2	WU	WU2POL	WUPOL	0	DPEN	WU2EN	WUEN	xx000101	bbbbrrbbb
E683	1	TOGCTL	Toggle Control	Q	S	R	I/O	EP3	EP2	EP1	EP0	x0000000	rrrrbbbb
E684	1	USBFAMEH	USB Frame count H	0	0	0	0	0	FC10	FC9	FC8	00000xxx	R

Note

17. Read and writes to these register may require synchronization delay, see the section "Synchronization Delay" in the [EZ-USB TRM](#).

Table 9. FX1 Register Summary *(continued)*

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E685	1	USBFRAME_L	USB Frame count L	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	xxxxxxx	R
E686	1	reserved											
E687	1	FNADDR	USB Function address	0	FA6	FA5	FA4	FA3	FA2	FA1	FA0	0xxxxxx	R
E688	2	reserved											
		ENDPOINTS											
E68A	1	EP0BCH ^[18]	Endpoint 0 Byte Count H	(BC15)	(BC14)	(BC13)	(BC12)	(BC11)	(BC10)	(BC9)	(BC8)	xxxxxxx	RW
E68B	1	EP0BCL ^[18]	Endpoint 0 Byte Count L	(BC7)	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxx	RW
E68C	1	reserved											
E68D	1	EP1OUTBC	Endpoint 1 OUT Byte Count	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxx	RW
E68E	1	reserved											
E68F	1	EP1INBC	Endpoint 1 IN Byte Count	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxx	RW
E690	1	EP2BCH ^[18]	Endpoint 2 Byte Count H	0	0	0	0	0	BC10	BC9	BC8	xxxxxxx	RW
E691	1	EP2BCL ^[18]	Endpoint 2 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxx	RW
E692	2	reserved											
E694	1	EP4BCH ^[18]	Endpoint 4 Byte Count H	0	0	0	0	0	0	BC9	BC8	xxxxxxx	RW
E695	1	EP4BCL ^[18]	Endpoint 4 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxx	RW
E696	2	reserved											
E698	1	EP6BCH ^[18]	Endpoint 6 Byte Count H	0	0	0	0	0	BC10	BC9	BC8	xxxxxxx	RW
E699	1	EP6BCL ^[18]	Endpoint 6 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxx	RW
E69A	2	reserved											
E69C	1	EP8BCH ^[18]	Endpoint 8 Byte Count H	0	0	0	0	0	0	BC9	BC8	xxxxxxx	RW
E69D	1	EP8BCL ^[18]	Endpoint 8 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxx	RW
E69E	2	reserved											

Note

18. Read and writes to these register may require synchronization delay, see the section "Synchronization Delay" in the [EZ-USB TRM](#).

Table 9. FX1 Register Summary *(continued)*

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
	3	reserved											
		reserved											
		reserved											
E6EA	1	EP8GPIFFLGSEL ^[21]	Endpoint 8 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW
E6EB	1	EP8GPIFPFSTOP	Endpoint 8 GPIF stop transaction on prog. flag	0	0	0	0	0	0	0	FIFO8FLAG	00000000	RW
E6EC	1	EP8GPIFTRIG ^[21]	Endpoint 8 GPIF Trigger	x	x	x	x	x	x	x	x	xxxxxxx	W
	3	reserved											
E6F0	1	XGPIFSGLDATH	GPIF Data H (16-bit mode only)	D15	D14	D13	D12	D11	D10	D9	D8	xxxxxxx	RW
E6F1	1	XGPIFSGLDATLX	Read/Write GPIF Data L & trigger transaction	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxx	RW
E6F2	1	XGPIFSGLDATLNOX	Read GPIF Data L, no transaction trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxx	R
E6F3	1	GPIFREADYCFG	Internal RDY, Sync/Async, RDY pin states	INTRDY	SAS	TCXRDY5	0	0	0	0	0	00000000	bbbrrrrr
E6F4	1	GPIFREADYSTAT	GPIF Ready Status	0	0	RDY5	RDY4	RDY3	RDY2	RDY1	RDY0	00xxxxxx	R
E6F5	1	GPIFABORT	Abort GPIF Waveforms	x	x	x	x	x	x	x	x	xxxxxxx	W
E6F6	2	reserved											
		ENDPOINT BUFFERS											
E740	64	EP0BUF	EP0-IN/-OUT buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxx	RW
E780	64	EP10UTBUF	EP1-OUT buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxx	RW
E7C0	64	EP1INBUF	EP1-IN buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxx	RW
	2048	reserved											RW

Note

21. Read and writes to these register may require synchronization delay, see the section "Synchronization Delay" in the [EZ-USB TRM](#).

Table 9. FX1 Register Summary *(continued)*

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
A8	1	IE	Interrupt Enable (bit addressable)	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	00000000	RW
A9	1	reserved											
AA	1	EP2468STAT ^[25]	Endpoint 2, 4, 6, 8 status flags	EP8F	EP8E	EP6F	EP6E	EP4F	EP4E	EP2F	EP2E	01011010	R
AB	1	EP24FIFOFLGS ^[25]	Endpoint 2, 4 slave FIFO status flags	0	EP4PF	EP4EF	EP4FF	0	EP2PF	EP2EF	EP2FF	00100010	R
AC	1	EP68FIFOFLGS ^[25]	Endpoint 6, 8 slave FIFO status flags	0	EP8PF	EP8EF	EP8FF	0	EP6PF	EP6EF	EP6FF	01100110	R
AD	2	reserved											
AF	1	AUTOPTRSETUP ^[25]	Autopointer 1&2 setup	0	0	0	0	0	APTR2INC	APTR1INC	APTREN	00000110	RW
B0	1	IOD ^[24]	Port D (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
B1	1	IOE ^[25]	Port E (NOT bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
B2	1	OEA ^[25]	Port A Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
B3	1	OEB ^[25]	Port B Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
B4	1	OEC ^[25]	Port C Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
B5	1	OED ^[25]	Port D Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
B6	1	OEE ^[25]	Port E Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
B7	1	reserved											
B8	1	IP	Interrupt Priority (bit addressable)	1	PS1	PT2	PS0	PT1	PX1	PT0	PX0	10000000	RW
B9	1	reserved											
BA	1	EP01STAT ^[25]	Endpoint 0&1 Status	0	0	0	0	0	EP1INBSY	EP1OUTBSY	EP0BSY	00000000	R
BB	1	GPIFTRIG ^[25, 26]	Endpoint 2, 4, 6, 8 GPIF slave FIFO Trigger	DONE	0	0	0	0	RW	EP1	EP0	10000xxx brrrrbbb	

Notes

25. SFRs not part of the standard 8051 architecture.

26. Read and writes to these register may require synchronization delay, see the section "Synchronization Delay" in the [EZ-USB TRM](#).

Table 9. FX1 Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E1	7	reserved											
E8	1	EIE ^[28]	External Interrupt Enable(s)	1	1	1	EX6	EX5	EX4	EI ² C	EUSB	11100000	RW
E9	7	reserved											
F0	1	B	B (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
F1	7	reserved											
F8	1	EIP ^[28]	External Interrupt Priority Control	1	1	1	PX6	PX5	PX4	PI ² C	PUSB	11100000	RW
F9	7	reserved											

Legend (For the Access column)

R = all bits read-only
W = all bits write-only
r = read-only bit
w = write-only bit
b = both read/write bit

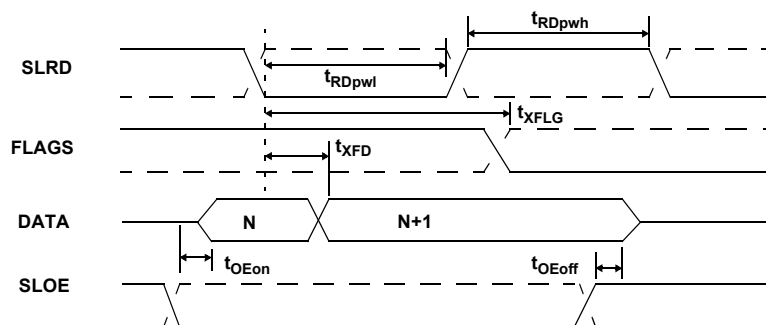
Note

28. SFRs not part of the standard 8051 architecture.

Slave FIFO Asynchronous Read

In the following figure, dashed lines indicate signals with programmable polarity.

Figure 20. Slave FIFO Asynchronous Read Timing Diagram



In the following table, the Slave FIFO asynchronous parameter values use internal IFCLK setting at 48 MHz.

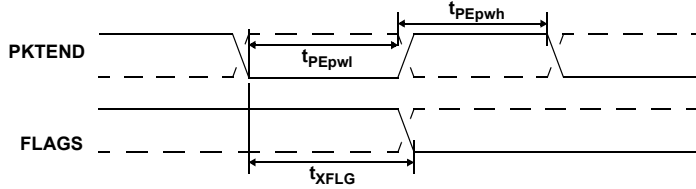
Table 17. Slave FIFO Asynchronous Read Parameters

Parameter	Description	Min	Max	Unit
t_{RDpwl}	SLRD Pulse Width LOW	50	–	ns
t_{RDpwh}	SLRD Pulse Width HIGH	50	–	ns
t_{XFLG}	SLRD to FLAGS Output Propagation Delay	–	70	ns
t_{XFD}	SLRD to FIFO Data Output Propagation Delay	–	15	ns
t_{OEon}	SLOE Turn-on to FIFO Data Valid	–	10.5	ns
t_{OEoff}	SLOE Turn-off to FIFO Data Hold	–	10.5	ns

Slave FIFO Asynchronous Packet End Strobe

In the following figure, dashed lines indicate signals with programmable polarity.

Figure 25. Slave FIFO Asynchronous Packet End Strobe Timing Diagram



In the following table, the Slave FIFO asynchronous parameter values use internal IFCLK setting at 48 MHz.

Table 23. Slave FIFO Asynchronous Packet End Strobe Parameters

Parameter	Description	Min	Max	Unit
t_{PEpwl}	PKTEND Pulse Width LOW	50	–	ns
t_{PEpwh}	PKTEND Pulse Width HIGH	50	–	ns
t_{XFLG}	PKTEND to FLAGS Output Propagation Delay	–	115	ns

Slave FIFO Output Enable

In the following figure, dashed lines indicate signals with programmable polarity.

Figure 26. Slave FIFO Output Enable Timing Diagram

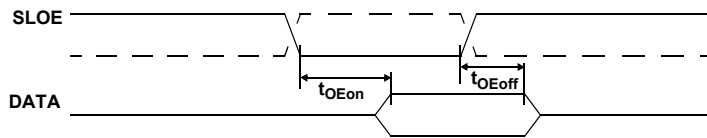


Table 24. Slave FIFO Output Enable Parameters

Parameter	Description	Max	Unit
t_{OEon}	SLOE Assert to FIFO DATA Output	10.5	ns
t_{OEoff}	SLOE Deassert to FIFO DATA Hold	10.5	ns

Slave FIFO Address to Flags/Data

In the following figure, dashed lines indicate signals with programmable polarity.

Figure 27. Slave FIFO Address to Flags/Data Timing Diagram

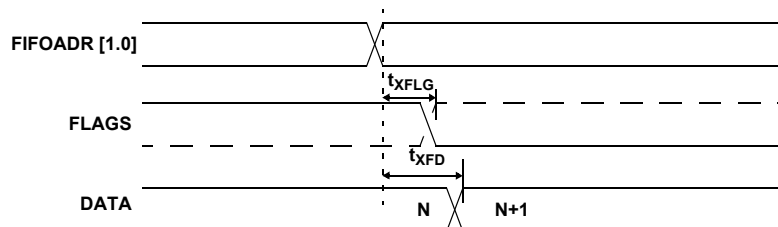
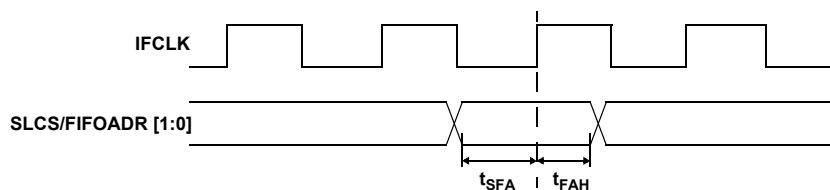


Table 25. Slave FIFO Address to Flags/Data Parameters

Parameter	Description	Max	Unit
t_{XFLG}	FIFOADR[1:0] to FLAGS Output Propagation Delay	10.7	ns
t_{XFD}	FIFOADR[1:0] to FIFODATA Output Propagation Delay	14.3	ns

Slave FIFO Synchronous Address

Figure 28. Slave FIFO Synchronous Address Timing Diagram



The following table provides the Slave FIFO Synchronous Address Parameters.^[40]

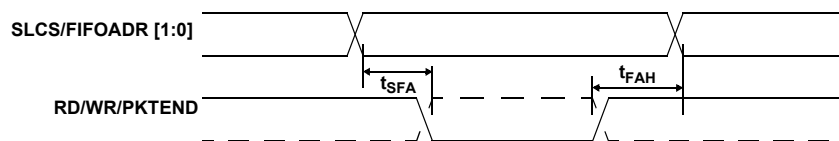
Table 26. Slave FIFO Synchronous Address Parameters

Parameter	Description	Min	Max	Unit
t_{IFCLK}	Interface Clock Period	20.83	200	ns
t_{SFA}	FIFOADR[1:0] to Clock Setup Time	25	–	ns
t_{FAH}	Clock to FIFOADR[1:0] Hold Time	10	–	ns

Slave FIFO Asynchronous Address

In the following figure, dashed lines indicate signals with programmable polarity.

Figure 29. Slave FIFO Asynchronous Address Timing Diagram



In the following table, the Slave FIFO asynchronous parameter values use internal IFCLK setting at 48 MHz.

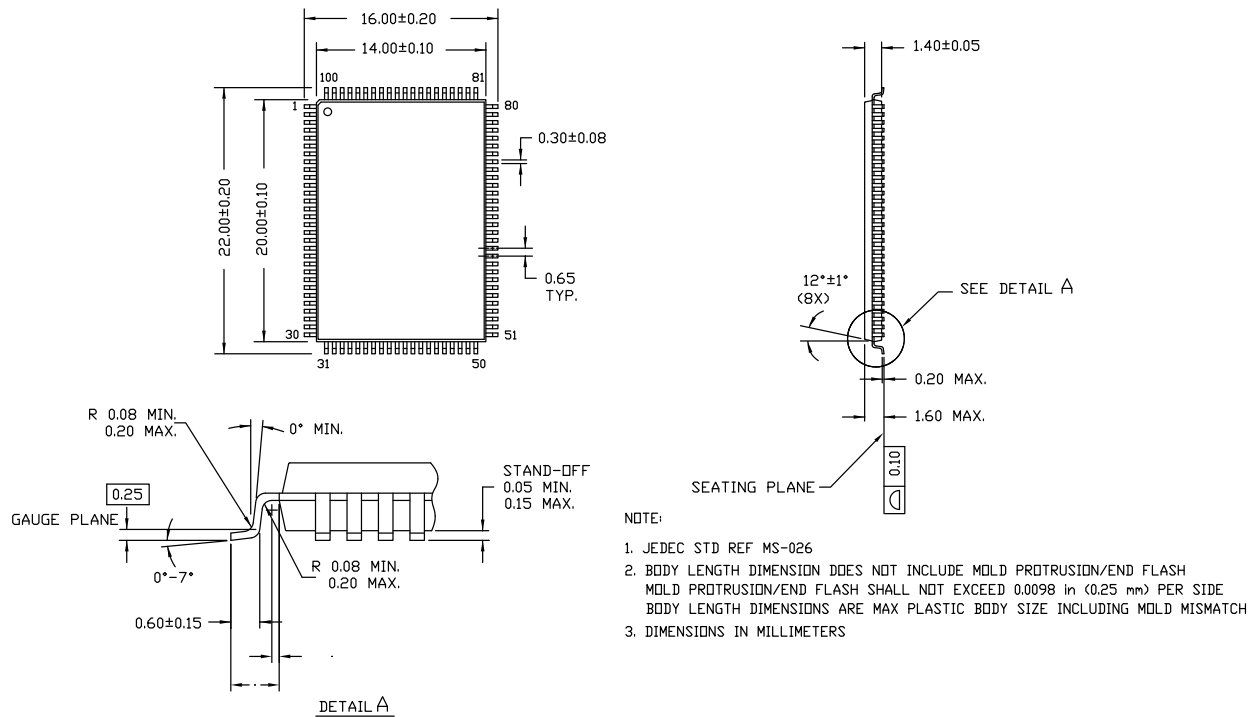
Table 27. Slave FIFO Asynchronous Address Parameters

Parameter	Description	Min	Unit
t_{SFA}	FIFOADR[1:0] to RD/WR/PKTEND Setup Time	10	ns
t_{FAH}	RD/WR/PKTEND to FIFOADR[1:0] Hold Time	10	ns

Note

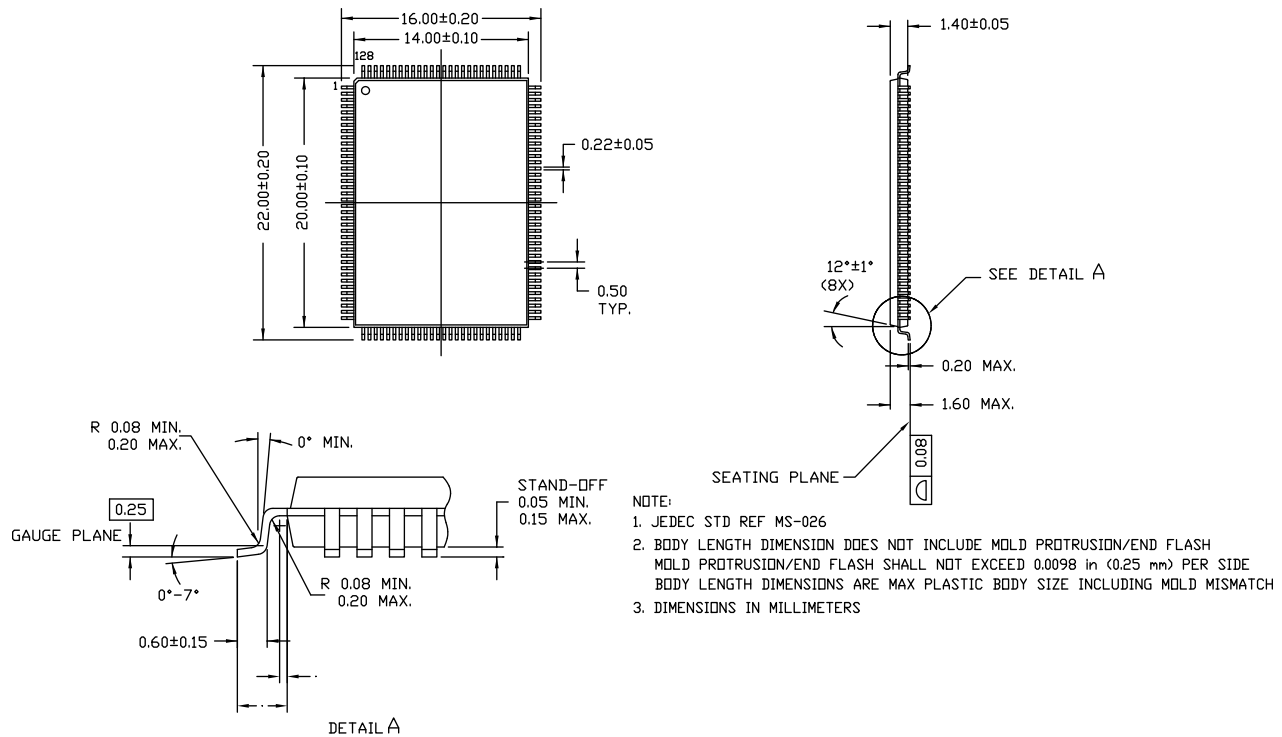
40. IFCLK must not exceed 48 MHz.

Figure 38. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA



51-85050 *E

Figure 39. 128-pin TQFP (14 × 20 × 1.4 mm) A128RA



51-85101 *F

Quad Flat Package No Leads (QFN) Package Design Notes

Electrical contact of the part to the Printed Circuit Board (PCB) is made by soldering the leads on the bottom surface of the package to the PCB. As a result, special attention is required to the heat transfer area below the package to provide a good thermal bond to the circuit board. A Copper (Cu) fill is to be designed into the PCB as a thermal pad under the package. Heat is transferred from the FX1 through the device's metal paddle on the bottom side of the package. Heat from here, is conducted to the PCB at the thermal pad. It is then conducted from the thermal pad to the PCB inner ground plane by a 5 × 5 array of via. A via is a plated through hole in the PCB with a finished diameter of 13 mil. The QFN's metal die paddle must be soldered to the PCB's thermal pad. Solder mask is placed on the board top side over each via to resist solder flow into the via. The mask on the top side also minimizes outgassing during the solder reflow process.

For further information on this package design please refer to 'Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages'. This can be found on Amkor's website <http://www.amkor.com>.

The application note provides detailed information on board mounting guidelines, soldering flow, rework process, and so on.

Figure 40 on page 69 displays a cross-sectional area underneath the package. The cross section is of only one via. The solder paste template needs to be designed to allow at least 50% solder coverage. The thickness of the solder paste template must be 5 mil. It is recommended that 'No Clean' type 3 solder paste is used for mounting the part. Nitrogen purge is recommended during reflow.

Figure 41 on page 69 is a plot of the solder mask pattern and Figure 42 on page 69 displays an X-Ray image of the assembly (darker areas indicate solder).

Document History Page *(continued)*

Document Title: CY7C64713, EZ-USB FX1™ USB Microcontroller Full Speed USB Peripheral Controller Document Number: 38-08039				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*K	3999873	SIRK	07/22/2013	Added Errata footnote (Note 3). Updated Functional Overview: Updated Interrupt System: Updated FIFO/GPIF Interrupt (INT4): Added Note 3 and referred the same note in "Endpoint 2 empty flag" in Table 4. Updated Package Diagrams: spec 51-85062 – Changed revision from *D to *F. spec 001-53450 – Changed revision from *B to *C. Added Errata. Updated in new template.
*L	4302739	DBIR	03/09/2014	Updated Package Diagrams: spec 001-53450 – Changed revision from *C to *D. spec 51-85050 – Changed revision from *D to *E. spec 51-85101 – Changed revision from *E to *F. Completing Sunset Review.