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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	USB Microcontroller
Core Processor	8051
Program Memory Type	ROMless
Controller Series	CY7C647xx
RAM Size	16K x 8
Interface	I²C, USB, USART
Number of I/O	40
Voltage - Supply	3.15V ~ 3.45V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-TQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c64713-128axc

Logic Block Diagram

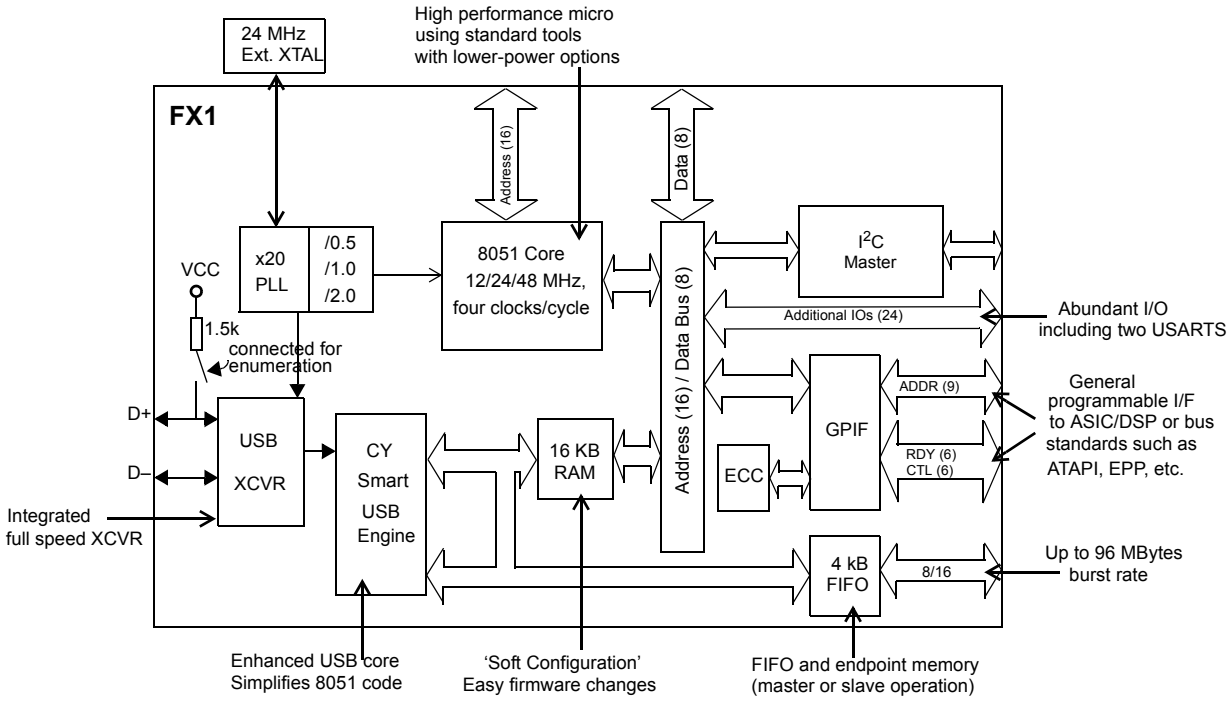


Figure 1. Crystal Configuration

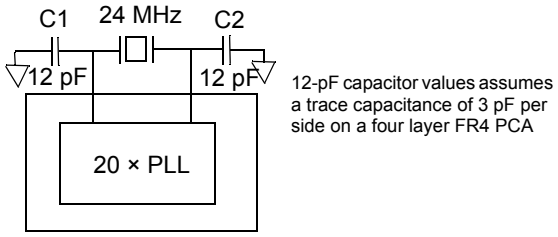


Table 1. Special Function Registers

x	8x	9x	Ax	Bx	Cx	Dx	Ex	Fx
0	**IOA**	**IOB**	**IOC**	**IOD**	SCON1	PSW	ACC	B
1	SP	**EXIF**	**INT2CLR**	**IOE**	SBUF1			
2	DPL0	**MPAGE**	**INT4CLR**	**OEA**				
3	DPH0			**OEB**				
4	**DPL1**			**OEC**				
5	**DPH1**			**OED**				
6	**DPS**			**OEE**				
7	PCON							
8	TCON	SCON0	IE	IP	T2CON	**EICON**	**EIE**	**EIP**
9	TMOD	SBUF0						
A	TL0	**AUTOPTRH1**	**EP2468STAT**	**EP01STAT**	RCAP2L			
B	TL1	**AUTOPTRL1**	**EP24FIFOFLGS**	**GPIFTRIG**	RCAP2H			
C	TH0	**reserved**	**EP68FIFOFLGS**		TL2			
D	TH1	**AUTOPTRH2**		**GPIFSGLDATH**	TH2			
E	**CKCON**	**AUTOPTRL2**		**GPIFSGLDATLX**				
F		**reserved**	**AUTOPTRSETUP**	**GPIFSGLDATLNOX**				

I²C Bus

FX1 supports the I²C bus as a master only at 100/400 KHz. SCL and SDA pins have open drain outputs and hysteresis inputs. These signals must be pulled up to 3.3 V, even if no I²C device is connected.

Buses

All packages: 8 or 16-bit ‘FIFO’ bidirectional data bus, multiplexed on I/O ports B and D. 128-pin package: adds 16-bit output only 8051 address bus, 8-bit bidirectional data bus.

USB Boot Methods

During the power up sequence, internal logic checks the I²C port for the connection of an EEPROM whose first byte is either 0xC0 or 0xC2. If found, it uses the VID/PID/DID values in the EEPROM in place of the internally stored values (0xC0). Alternatively, it boot-loads the EEPROM contents into an internal RAM (0xC2). If no EEPROM is detected, FX1 enumerates using internally stored descriptors. The default ID values for FX1 are VID/PID/DID (0x04B4, 0x6473, 0xAxxx where xxx=Chip revision).[2]

Table 2. Default ID Values for FX1

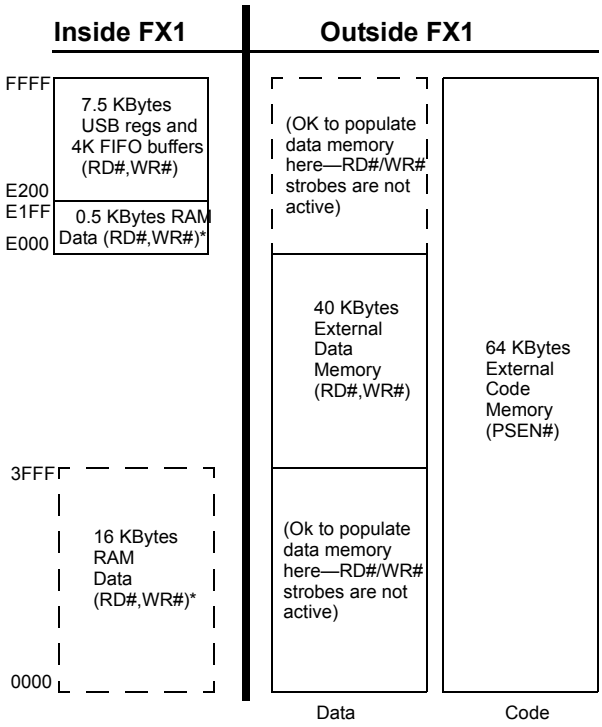
Default VID/PID/DID		
Vendor ID	0x04B4	Cypress Semiconductor
Product ID	0x6473	EZ-USB FX1
Device release	0xAnnn	Depends on chip revision (nnn = chip revision where first silicon = 001)

Notes
2. The I²C bus SCL and SDA pins must be pulled up, even if an EEPROM is not connected. Otherwise this detection method does not work properly.

External Code Memory, EA = 1

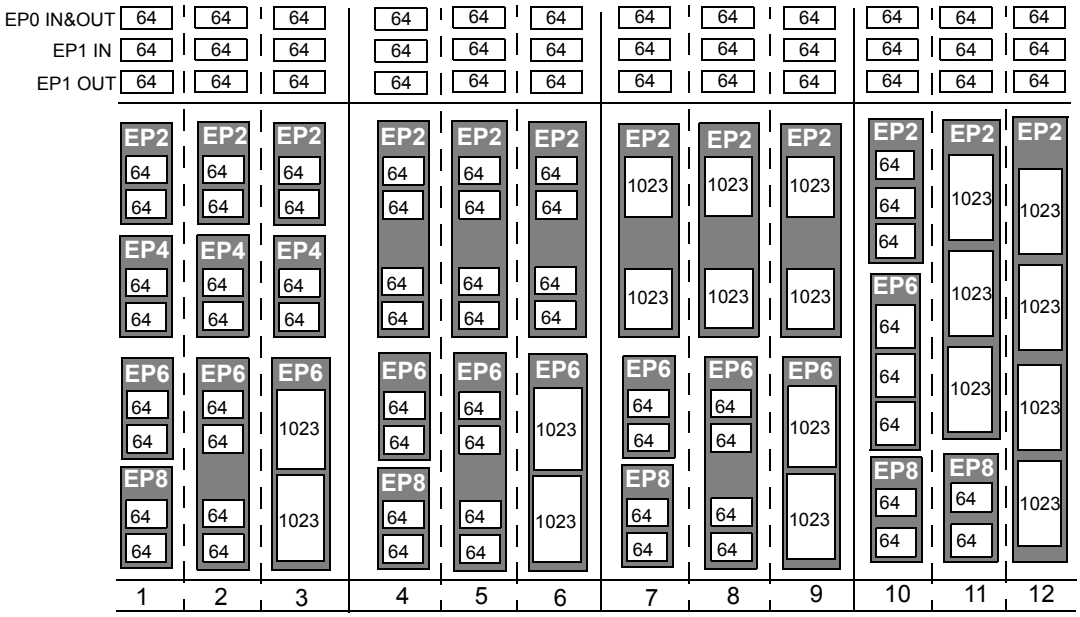
The bottom 16 KBytes of program memory is external, and therefore the bottom 16 KBytes of internal RAM is accessible only as data memory.

Figure 4. External Code Memory, EA = 1



*SUDPTR, USB upload/download, I^2C interface boot access

Figure 6. Endpoint Configuration



Master/Slave Control Signals

The FX1 endpoint FIFOS are implemented as eight physically distinct 256 × 16 RAM blocks. The 8051/SIE can switch any of the RAM blocks between two domains: the USB (SIE) domain and the 8051-I/O Unit domain. This switching is done instantaneously, giving essentially zero transfer time between “USB FIFOS” and “Slave FIFOS”. While they are physically the same memory, no bytes are actually transferred between buffers.

At any time, some RAM blocks fill or empty with USB data under SIE control, while other RAM blocks are available to the 8051 and the I/O control unit. The RAM blocks operate as a single-port in the USB domain, and dual port in the 8051-I/O domain. The blocks are configured as single, double, triple, or quad buffered.

The I/O control unit implements either an internal master (M for master) or external master (S for Slave) interface.

In Master (M) mode, the GPIF internally controls FIFOADR[1..0] to select a FIFO. The RDY pins (two in the 56-pin package, six in the 100-pin and 128-pin packages) are used as flag inputs from an external FIFO or other logic if desired. The GPIF is run from either an internally derived clock or an externally supplied clock (IFCLK), at a rate that transfers data up to 96 Megabytes/s (48 MHz IFCLK with 16-bit interface).

In Slave (S) mode, the FX1 accepts either an internally derived clock or an externally supplied clock (IFCLK with a maximum frequency of 48 MHz) and SLCS#, SLRD, SLWR, SLOE, PKTEND signals from external logic. When using an external IFCLK, the external clock must be present before switching to the external clock with the IFCLKSRC bit. Each endpoint can individually be selected for byte or word operation by an internal configuration bit, and a Slave FIFO Output Enable signal SLOE enables data of the selected width. External logic must ensure that the output enable signal is inactive when writing data to a slave FIFO. The slave interface can also operate asynchronously, where the SLRD and SLWR signals act directly as strobes, rather than a clock qualifier as in the synchronous mode. The signals SLRD, SLWR, SLOE, and PKTEND are gated by the signal SLCS#.

GPIF and FIFO Clock Rates

An 8051 register bit selects one of two frequencies for the internally supplied interface clock: 30 MHz and 48 MHz. Alternatively, an externally supplied clock of 5 to 48 MHz feeding the IFCLK pin is used as the interface clock. IFCLK is configured to function as an output clock when the GPIF and FIFOs are internally clocked. An output enable bit in the IFCONFIG register turns this clock output off, if desired. Another bit within the IFCONFIG register inverts the IFCLK signal whether internally or externally sourced.

GPIF

The GPIF is a flexible 8 or 16-bit parallel interface driven by a user programmable finite state machine. It allows the CY7C64713 to perform local bus mastering, and can implement a wide variety of protocols such as ATA interface, printer parallel port, and Utopia.

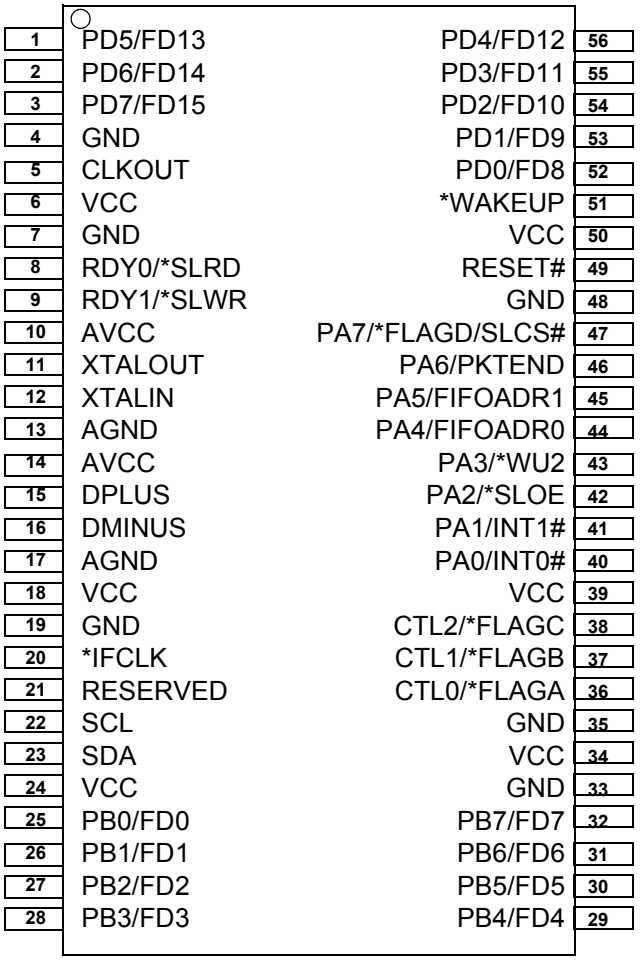
The GPIF has six programmable control outputs (CTL), nine address outputs (GPIFADRx), and six general purpose Ready inputs (RDY). The data bus width is 8 or 16 bits. Each GPIF vector defines the state of the control outputs, and determines what state a Ready input (or multiple inputs) must be before proceeding. The GPIF vector is programmed to advance a FIFO to the next data value, advance an address, and so on. A sequence of the GPIF vectors create a single waveform that executes to perform the data move between the FX1 and the external device.

Six Control OUT Signals

The 100-pin and 128-pin packages bring out all six Control Output pins (CTL0–CTL5). The 8051 programs the GPIF unit to define the CTL waveforms. The 56-pin package brings out three

Figure 10. CY7C64713 56-pin SSOP Pin Assignment

CY7C64713
56-pin SSOP



* indicates programmable polarity

Table 8. FX1 Pin Definitions *(continued)*

128-pin TQFP	100-pin TQFP	56-pin SSOP	56-pin QFN	Name	Type	Default	Description
4	3	8	1	RDY0 or SLRD	Input	N/A	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **RDY0** is a GPIF input signal. **SLRD** is the input-only read strobe with programmable polarity (FIFOPINPOLAR.3) for the slave FIFOs connected to FD[7..0] or FD[15..0].
5	4	9	2	RDY1 or SLWR	Input	N/A	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **RDY1** is a GPIF input signal. **SLWR** is the input-only write strobe with programmable polarity (FIFOPINPOLAR.2) for the slave FIFOs connected to FD[7..0] or FD[15..0].
6	5			RDY2	Input	N/A	**RDY2** is a GPIF input signal.
7	6			RDY3	Input	N/A	**RDY3** is a GPIF input signal.
8	7			RDY4	Input	N/A	**RDY4** is a GPIF input signal.
9	8			RDY5	Input	N/A	**RDY5** is a GPIF input signal.
69	54	36	29	CTL0 or FLAGA	O/Z	H	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **CTL0** is a GPIF control output. **FLAGA** is a programmable slave-FIFO output status flag signal. Defaults to programmable for the FIFO selected by the FIFOADR[1:0] pins.
70	55	37	30	CTL1 or FLAGB	O/Z	H	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **CTL1** is a GPIF control output. **FLAGB** is a programmable slave-FIFO output status flag signal. Defaults to FULL for the FIFO selected by the FIFOADR[1:0] pins.
71	56	38	31	CTL2 or FLAGC	O/Z	H	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **CTL2** is a GPIF control output. **FLAGC** is a programmable slave-FIFO output status flag signal. Defaults to EMPTY for the FIFO selected by the FIFOADR[1:0] pins.
66	51			CTL3	O/Z	H	**CTL3** is a GPIF control output.
67	52			CTL4	Output	H	**CTL4** is a GPIF control output.
98	76			CTL5	Output	H	**CTL5** is a GPIF control output.
32	26	20	13	IFCLK	I/O/Z	Z	Interface Clock, used for synchronously clocking data into or out of the slave FIFOs. IFCLK also serves as a timing reference for all slave FIFO control signals and GPIF. When internal clocking is used (IFCONFIG.7 = 1) the IFCLK pin is configured to output 30/48 MHz by bits IFCONFIG.5 and IFCONFIG.6. IFCLK may be inverted, whether internally or externally sourced, by setting the bit IFCONFIG.4 = 1.
28	22			INT4	Input	N/A	**INT4** is the 8051 INT4 interrupt request input signal. The INT4 pin is edge-sensitive, active HIGH.
106	84			INT5#	Input	N/A	**INT5#** is the 8051 INT5 interrupt request input signal. The INT5 pin is edge-sensitive, active LOW.

Table 8. FX1 Pin Definitions *(continued)*

128-pin TQFP	100-pin TQFP	56-pin SSOP	56-pin QFN	Name	Type	Default	Description
49	39			GND	Ground	N/A	**Ground**.
58	48	33	26	GND	Ground	N/A	**Ground**.
65	50	35	28	GND	Ground	N/A	**Ground**.
80	65			GND	Ground	N/A	**Ground**.
93	75	48	41	GND	Ground	N/A	**Ground**.
116	94			GND	Ground	N/A	**Ground**.
125	99	4	53	GND	Ground	N/A	**Ground**.
14	13			NC	N/A	N/A	**No Connect**. This pin must be left open.
15	14			NC	N/A	N/A	**No Connect**. This pin must be left open.
16	15			NC	N/A	N/A	**No Connect**. This pin must be left open.

Register Summary

FX1 register bit definitions are described in the EZ-USB TRM in greater detail.

Table 9. FX1 Register Summary

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
		GPIF Waveform Memories											
E400	128	WAVEDATA	GPIF Waveform Descriptor 0, 1, 2, 3 data	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E480	128	reserved											
		GENERAL CONFIGURATION											
E600	1	CPUCS	CPU Control & Status	0	0	PORTCSTB	CLKSPD1	CLKSPD0	CLKINV	CLKOE	8051RES	00000010	rrbbbbbr
E601	1	IFCONFIG	Interface Configuration (Ports, GPIF, slave FIFOs)	IFCLKSRC	3048MHZ	IFCLKOE	IFCLKPOL	ASYNC	GSTATE	IFCFG1	IFCFG0	10000000	RW
E602	1	PINFLAGSAB[8]	Slave FIFO FLAGA and FLAGB Pin Configuration	FLAGB3	FLAGB2	FLAGB1	FLAGB0	FLAGA3	FLAGA2	FLAGA1	FLAGA0	00000000	RW
E603	1	PINFLAGSCD[8]	Slave FIFO FLAGC and FLAGD Pin Configuration	FLAGD3	FLAGD2	FLAGD1	FLAGD0	FLAGC3	FLAGC2	FLAGC1	FLAGC0	00000000	RW
E604	1	FIFORESET[8]	Restore FIFOS to default state	NAKALL	0	0	0	EP3	EP2	EP1	EP0	xxxxxxxx	W
E605	1	BREAKPT	Breakpoint Control	0	0	0	0	BREAK	BPPULSE	BPEN	0	00000000	rrrrbbbr
E606	1	BPADDRH	Breakpoint Address H	A15	A14	A13	A12	A11	A10	A9	A8	xxxxxxxx	RW
E607	1	BPADDRL	Breakpoint Address L	A7	A6	A5	A4	A3	A2	A1	A0	xxxxxxxx	RW
E608	1	UART230	230 Kbaud internally generated ref. clock	0	0	0	0	0	0	230UART1	230UART0	00000000	rrrrrrbb
E609	1	FIFOPINPOLAR[8]	Slave FIFO Interface pins polarity	0	0	PKTEND	SLOE	SLRD	SLWR	EF	FF	00000000	rrbbbbbb
E60A	1	REVID	Chip Revision	rv7	rv6	rv5	rv4	rv3	rv2	rv1	rv0	RevA 00000001	R
E60B	1	REVCTL[8]	Chip Revision Control	0	0	0	0	0	0	dyn_out	enh_pkt	00000000	rrrrrrbb

Note

8. Read and writes to these register may require synchronization delay, see the section “Synchronization Delay” in the EZ-USB TRM.

Table 9. FX1 Register Summary *(continued)*

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E65C	1	USBIE	USB Int Enables	0	EP0ACK	0	URES	SUSP	SUTOK	SOF	SUDAV	00000000	RW
E65D	1	USBIRQ[15]	USB Interrupt Requests	0	EP0ACK	0	URES	SUSP	SUTOK	SOF	SUDAV	0xxxxxxx	rbbbbbbb
E65E	1	EPIE	Endpoint Interrupt Enables	EP8	EP6	EP4	EP2	EP1OUT	EP1IN	EP0OUT	EP0IN	00000000	RW
E65F	1	EPIRQ[15]	Endpoint Interrupt Requests	EP8	EP6	EP4	EP2	EP1OUT	EP1IN	EP0OUT	EP0IN	0	RW
E660	1	GPIFIE[16]	GPIF Interrupt Enable	0	0	0	0	0	0	GPIFWF	GPIFDONE	00000000	RW
E661	1	GPIFIRQ[16]	GPIF Interrupt Request	0	0	0	0	0	0	GPIFWF	GPIFDONE	000000xx	RW
E662	1	USBERRIE	USB Error Interrupt Enables	ISOEP8	ISOEP6	ISOEP4	ISOEP2	0	0	0	ERRLIMIT	00000000	RW
E663	1	USBERRIRQ[15]	USB Error Interrupt Requests	ISOEP8	ISOEP6	ISOEP4	ISOEP2	0	0	0	ERRLIMIT	0000000x	bbbbrrrb
E664	1	ERRCNTLIM	USB Error counter and limit	EC3	EC2	EC1	EC0	LIMIT3	LIMIT2	LIMIT1	LIMIT0	xxxx0100	rrrrbbbb
E665	1	CLRERRCNT	Clear Error Counter EC3:0	x	x	x	x	x	x	x	x	xxxxxxxx	W
E666	1	INT2IVEC	Interrupt 2 (USB) Autovector	0	I2V4	I2V3	I2V2	I2V1	I2V0	0	0	00000000	R
E667	1	INT4IVEC	Interrupt 4 (slave FIFO & GPIF) Autovector	1	0	I4V3	I4V2	I4V1	I4V0	0	0	10000000	R
E668	1	INTSETUP	Interrupt 2 & 4 setup	0	0	0	0	AV2EN	0	INT4SRC	AV4EN	00000000	RW
E669	7	reserved											
		INPUT / OUTPUT											
E670	1	PORTACFG	I/O PORTA Alternate Configuration	FLAGD	SLCS	0	0	0	0	INT1	INT0	00000000	RW

Notes
15. SFRs not part of the standard 8051 architecture.
16. Read and writes to these register may require synchronization delay, see the section “Synchronization Delay” in the EZ-USB TRM.

Table 9. FX1 Register Summary *(continued)*

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E6A0	1	EP0CS	Endpoint 0 Control and Status	HSNAK	0	0	0	0	0	BUSY	STALL	10000000	bbbbbbrb
E6A1	1	EP1OUTCS	Endpoint 1 OUT Control and Status	0	0	0	0	0	0	BUSY	STALL	00000000	bbbbbbrb
E6A2	1	EP1INCS	Endpoint 1 IN Control and Status	0	0	0	0	0	0	BUSY	STALL	00000000	bbbbbbrb
E6A3	1	EP2CS	Endpoint 2 Control and Status	0	NPAK2	NPAK1	NPAK0	FULL	EMPTY	0	STALL	00101000	rrrrrrrb
E6A4	1	EP4CS	Endpoint 4 Control and Status	0	0	NPAK1	NPAK0	FULL	EMPTY	0	STALL	00101000	rrrrrrrb
E6A5	1	EP6CS	Endpoint 6 Control and Status	0	NPAK2	NPAK1	NPAK0	FULL	EMPTY	0	STALL	00000100	rrrrrrrb
E6A6	1	EP8CS	Endpoint 8 Control and Status	0	0	NPAK1	NPAK0	FULL	EMPTY	0	STALL	00000100	rrrrrrrb
E6A7	1	EP2FIFOFLGS	Endpoint 2 slave FIFO Flags	0	0	0	0	0	PF	EF	FF	00000010	R
E6A8	1	EP4FIFOFLGS	Endpoint 4 slave FIFO Flags	0	0	0	0	0	PF	EF	FF	00000010	R
E6A9	1	EP6FIFOFLGS	Endpoint 6 slave FIFO Flags	0	0	0	0	0	PF	EF	FF	00000110	R
E6AA	1	EP8FIFOFLGS	Endpoint 8 slave FIFO Flags	0	0	0	0	0	PF	EF	FF	00000110	R
E6AB	1	EP2FIFOBCH	Endpoint 2 slave FIFO total byte count H	0	0	0	BC12	BC11	BC10	BC9	BC8	00000000	R
E6AC	1	EP2FIFOBCL	Endpoint 2 slave FIFO total byte count L	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	00000000	R
E6AD	1	EP4FIFOBCH	Endpoint 4 slave FIFO total byte count H	0	0	0	0	0	BC10	BC9	BC8	00000000	R

Table 9. FX1 Register Summary *(continued)*

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E6C1	1	GPIFIDLECS	GPIF Done, GPIF IDLE drive mode	DONE	0	0	0	0	0	0	IDLEDRV	10000000	RW
E6C2	1	GPIFIDLECTL	Inactive Bus, CTL states	0	0	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0	11111111	RW
E6C3	1	GPIFCTLCFG	CTL Drive Type	TRICTL	0	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0	00000000	RW
E6C4	1	GPIFADRH[19]	GPIF Address H	0	0	0	0	0	0	0	GPIFA8	00000000	RW
E6C5	1	GPIFADRL[19]	GPIF Address L	GPIFA7	GPIFA6	GPIFA5	GPIFA4	GPIFA3	GPIFA2	GPIFA1	GPIFA0	00000000	RW
		FLOWSTATE											
E6C6	1	FLOWSTATE	Flowstate Enable and Selector	FSE	0	0	0	0	FS2	FS1	FS0	00000000	brrrrbbb
E6C7	1	FLOWLOGIC	Flowstate Logic	LFUNC1	LFUNC0	TERMA2	TERMA1	TERMA0	TERMB2	TERMB1	TERMB0	00000000	RW
E6C8	1	FLOWEQ0CTL	CTL-Pin States in Flowstate (when Logic = 0)	CTL0E3	CTL0E2	CTL0E1/CTL5	CTL0E0/CTL4	CTL3	CTL2	CTL1	CTL0	00000000	RW
E6C9	1	FLOWEQ1CTL	CTL-Pin States in Flowstate (when Logic = 1)	CTL0E3	CTL0E2	CTL0E1/CTL5	CTL0E0/CTL4	CTL3	CTL2	CTL1	CTL0	00000000	RW
E6CA	1	FLOWHOLDOFF	Holdoff Configuration	HOPERIOD3	HOPERIOD2	HOPERIOD1	HOPERIOD0	HOSTATE	HOCTL2	HOCTL1	HOCTL0	00000000	RW
E6CB	1	FLOWSTB	Flowstate Strobe Configuration	SLAVE	RDYASYNC	CTLTOGL	SUSTAIN	0	MSTB2	MSTB1	MSTB0	00100000	RW
E6CC	1	FLOWSTBEDGE	Flowstate Rising/Falling Edge Configuration	0	0	0	0	0	0	FALLING	RISING	00000001	rrrrrrbb
E6CD	1	FLOWSTBPERIOD	Master-Strobe Half-Period	D7	D6	D5	D4	D3	D2	D1	D0	00000010	RW
E6CE	1	GPIFTCB3[19]	GPIF Transaction Count Byte 3	TC31	TC30	TC29	TC28	TC27	TC26	TC25	TC24	00000000	RW
E6CF	1	GPIFTCB2[19]	GPIF Transaction Count Byte 2	TC23	TC22	TC21	TC20	TC19	TC18	TC17	TC16	00000000	RW

Note
19. Read and writes to these register may require synchronization delay, see the section “Synchronization Delay” in the EZ-USB TRM.

Table 9. FX1 Register Summary *(continued)*

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
	3	reserved											
		reserved											
		reserved											
E6EA	1	EP8GPIFFLGSEL[21]	Endpoint 8 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW
E6EB	1	EP8GPIFPFSTOP	Endpoint 8 GPIF stop transaction on prog. flag	0	0	0	0	0	0	0	FIFO8FLAG	00000000	RW
E6EC	1	EP8GPIFTRIG[21]	Endpoint 8 GPIF Trigger	x	x	x	x	x	x	x	x	xxxxxxxx	W
	3	reserved											
E6F0	1	XGPIFSGLDATH	GPIF Data H (16-bit mode only)	D15	D14	D13	D12	D11	D10	D9	D8	xxxxxxxx	RW
E6F1	1	XGPIFSGLDATLX	Read/Write GPIF Data L & trigger transaction	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E6F2	1	XGPIFSGLDATLNOX	Read GPIF Data L, no transaction trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	R
E6F3	1	GPIFREADYCFG	Internal RDY, Sync/Async, RDY pin states	INTRDY	SAS	TCXRDY5	0	0	0	0	0	00000000	bbbrrrrr
E6F4	1	GPIFREADYSTAT	GPIF Ready Status	0	0	RDY5	RDY4	RDY3	RDY2	RDY1	RDY0	00xxxxxx	R
E6F5	1	GPIFABORT	Abort GPIF Waveforms	x	x	x	x	x	x	x	x	xxxxxxxx	W
E6F6	2	reserved											
		ENDPOINT BUFFERS											
E740	64	EP0BUF	EP0-IN/-OUT buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E780	64	EP10UTBUF	EP1-OUT buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E7C0	64	EP1INBUF	EP1-IN buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
	2048	reserved											RW

Note
21. Read and writes to these register may require synchronization delay, see the section “Synchronization Delay” in the EZ-USB TRM.

Table 9. FX1 Register Summary *(continued)*

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
F000	1023	EP2FIFOBUF	64/1023-byte EP 2 / slave FIFO buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
F400	64	EP4FIFOBUF	64 byte EP 4 / slave FIFO buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
F600	64	reserved											
F800	1023	EP6FIFOBUF	64/1023-byte EP 6 / slave FIFO buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
FC00	64	EP8FIFOBUF	64 byte EP 8 / slave FIFO buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
FE00	64	reserved											
xxxx		I²C Configuration Byte		0	DISCON	0	0	0	0	0	400KHZ	xxxxxxxx[23]	n/a
		Special Function Registers (SFRs)											
80	1	IOA[22]	Port A (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
81	1	SP	Stack Pointer	D7	D6	D5	D4	D3	D2	D1	D0	00000111	RW
82	1	DPL0	Data Pointer 0 L	A7	A6	A5	A4	A3	A2	A1	A0	00000000	RW
83	1	DPH0	Data Pointer 0 H	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW
84	1	DPL1[22]	Data Pointer 1 L	A7	A6	A5	A4	A3	A2	A1	A0	00000000	RW
85	1	DPH1[22]	Data Pointer 1 H	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW
86	1	DPS[22]	Data Pointer 0/1 select	0	0	0	0	0	0	0	SEL	00000000	RW
87	1	PCON	Power Control	SMOD0	x	1	1	x	x	x	IDLE	00110000	RW
88	1	TCON	Timer/Counter Control (bit addressable)	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00000000	RW
89	1	TMOD	Timer/Counter Mode Control	GATE	CT	M1	M0	GATE	CT	M1	M0	00000000	RW
8A	1	TL0	Timer 0 reload L	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW

Notes
22. SFRs not part of the standard 8051 architecture.
23. If no EEPROM is detected by the SIE then the default is 00000000.

Table 9. FX1 Register Summary *(continued)*

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E1	7	reserved											
E8	1	EIE[28]	External Interrupt Enable(s)	1	1	1	EX6	EX5	EX4	EI²C	EUSB	11100000	RW
E9	7	reserved											
F0	1	B	B (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
F1	7	reserved											
F8	1	EIP[28]	External Interrupt Priority Control	1	1	1	PX6	PX5	PX4	PI²C	PUSB	11100000	RW
F9	7	reserved											

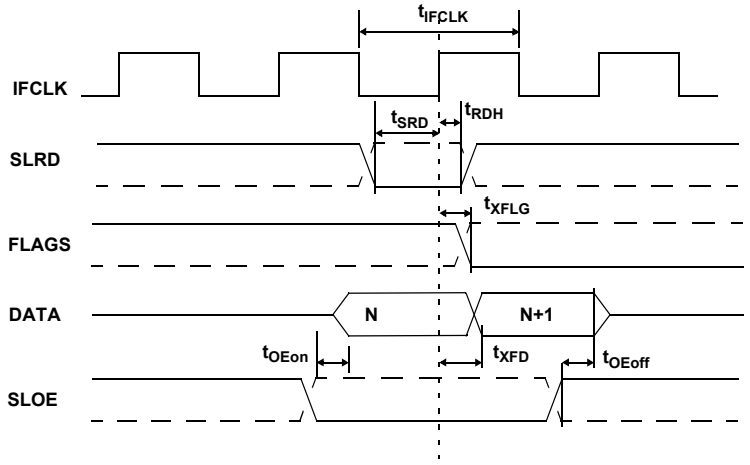
Legend (For the Access column)
R = all bits read-only
W = all bits write-only
r = read-only bit
w = write-only bit
b = both read/write bit

Note
28. SFRs not part of the standard 8051 architecture.

Slave FIFO Synchronous Read

In the following figure, dashed lines indicate signals with programmable polarity.

Figure 19. Slave FIFO Synchronous Read Timing Diagram



The following table provides the Slave FIFO Synchronous Read Parameters with Internally Sourced IFCLK. [36]

Table 15. Slave FIFO Synchronous Read Parameters with Internally Sourced IFCLK

Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK Period	20.83	–	ns
t_{SRD}	SLRD to Clock Setup Time	18.7	–	ns
t_{RDH}	Clock to SLRD Hold Time	0	–	ns
t_{OEon}	SLOE Turn on to FIFO Data Valid	–	10.5	ns
t_{OEoff}	SLOE Turn off to FIFO Data Hold	–	10.5	ns
t_{XFLG}	Clock to FLAGS Output Propagation Delay	–	9.5	ns
t_{XFD}	Clock to FIFO Data Output Propagation Delay	–	11	ns

The following table provides the Slave FIFO Synchronous Read Parameters with Externally Sourced IFCLK.[36]

Table 16. Slave FIFO Synchronous Read Parameters with Externally Sourced IFCLK

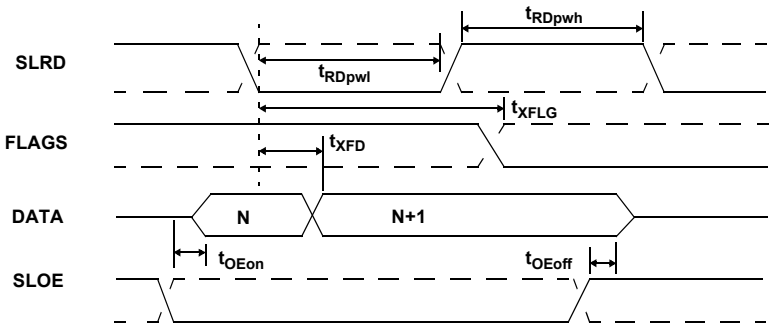
Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK Period	20.83	200	ns
t_{SRD}	SLRD to Clock Setup Time	12.7	–	ns
t_{RDH}	Clock to SLRD Hold Time	3.7	–	ns
t_{OEon}	SLOE Turn on to FIFO Data Valid	–	10.5	ns
t_{OEoff}	SLOE Turn off to FIFO Data Hold	–	10.5	ns
t_{XFLG}	Clock to FLAGS Output Propagation Delay	–	13.5	ns
t_{XFD}	Clock to FIFO Data Output Propagation Delay	–	15	ns

Note
36. IFCLK must not exceed 48 MHz.

Slave FIFO Asynchronous Read

In the following figure, dashed lines indicate signals with programmable polarity.

Figure 20. Slave FIFO Asynchronous Read Timing Diagram



In the following table, the Slave FIFO asynchronous parameter values use internal IFCLK setting at 48 MHz.

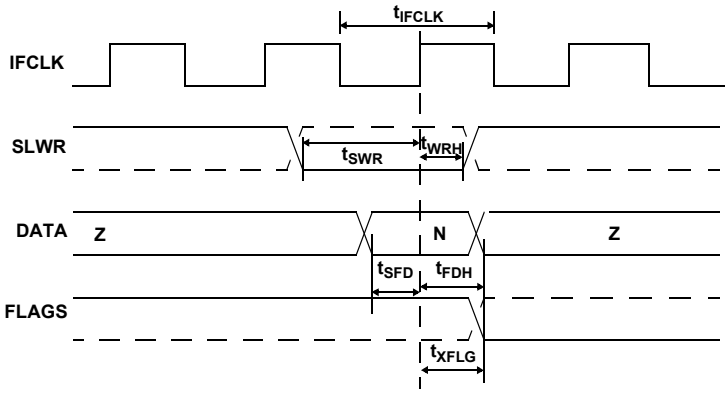
Table 17. Slave FIFO Asynchronous Read Parameters

Parameter	Description	Min	Max	Unit
t_{RDpwl}	SLRD Pulse Width LOW	50	–	ns
t_{RDpwh}	SLRD Pulse Width HIGH	50	–	ns
t_{XFLG}	SLRD to FLAGS Output Propagation Delay	–	70	ns
t_{XFD}	SLRD to FIFO Data Output Propagation Delay	–	15	ns
t_{OEon}	SLOE Turn-on to FIFO Data Valid	–	10.5	ns
t_{OEoff}	SLOE Turn-off to FIFO Data Hold	–	10.5	ns

Slave FIFO Synchronous Write

In the following figure, dashed lines indicate signals with programmable polarity.

Figure 21. Slave FIFO Synchronous Write Timing Diagram



The following table provides the Slave FIFO Synchronous Write Parameters with Internally Sourced IFCLK. [37]

Table 18. Slave FIFO Synchronous Write Parameters with Internally Sourced IFCLK

Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK Period	20.83	–	ns
t_{SWR}	SLWR to Clock Setup Time	18.1	–	ns
t_{WRH}	Clock to SLWR Hold Time	0	–	ns
t_{SFD}	FIFO Data to Clock Setup Time	9.2	–	ns
t_{FDH}	Clock to FIFO Data Hold Time	0	–	ns
t_{XFLG}	Clock to FLAGS Output Propagation Time	–	9.5	ns

The following table provides the Slave FIFO Synchronous Write Parameters with Externally Sourced IFCLK. [37]

Table 19. Slave FIFO Synchronous Write Parameters with Externally Sourced IFCLK [37]

Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK Period	20.83	200	ns
t_{SWR}	SLWR to Clock Setup Time	12.1	–	ns
t_{WRH}	Clock to SLWR Hold Time	3.6	–	ns
t_{SFD}	FIFO Data to Clock Setup Time	3.2	–	ns
t_{FDH}	Clock to FIFO Data Hold Time	4.5	–	ns
t_{XFLG}	Clock to FLAGS Output Propagation Time	–	13.5	ns

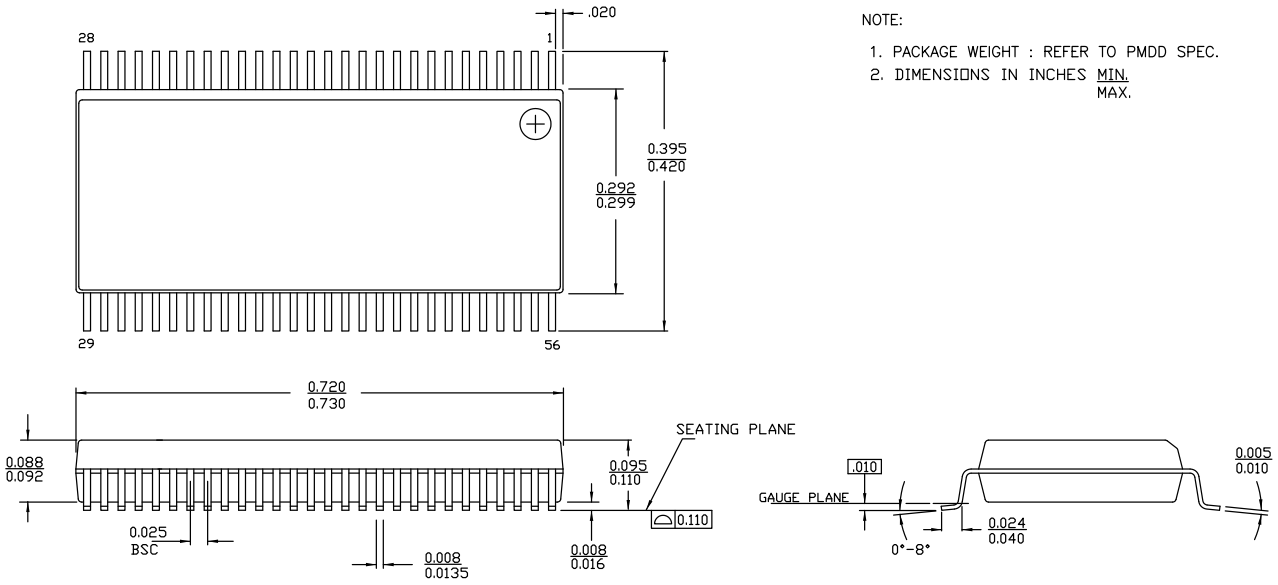
Note
37. IFCLK must not exceed 48 MHz.

Package Diagrams

The FX1 is available in four packages:

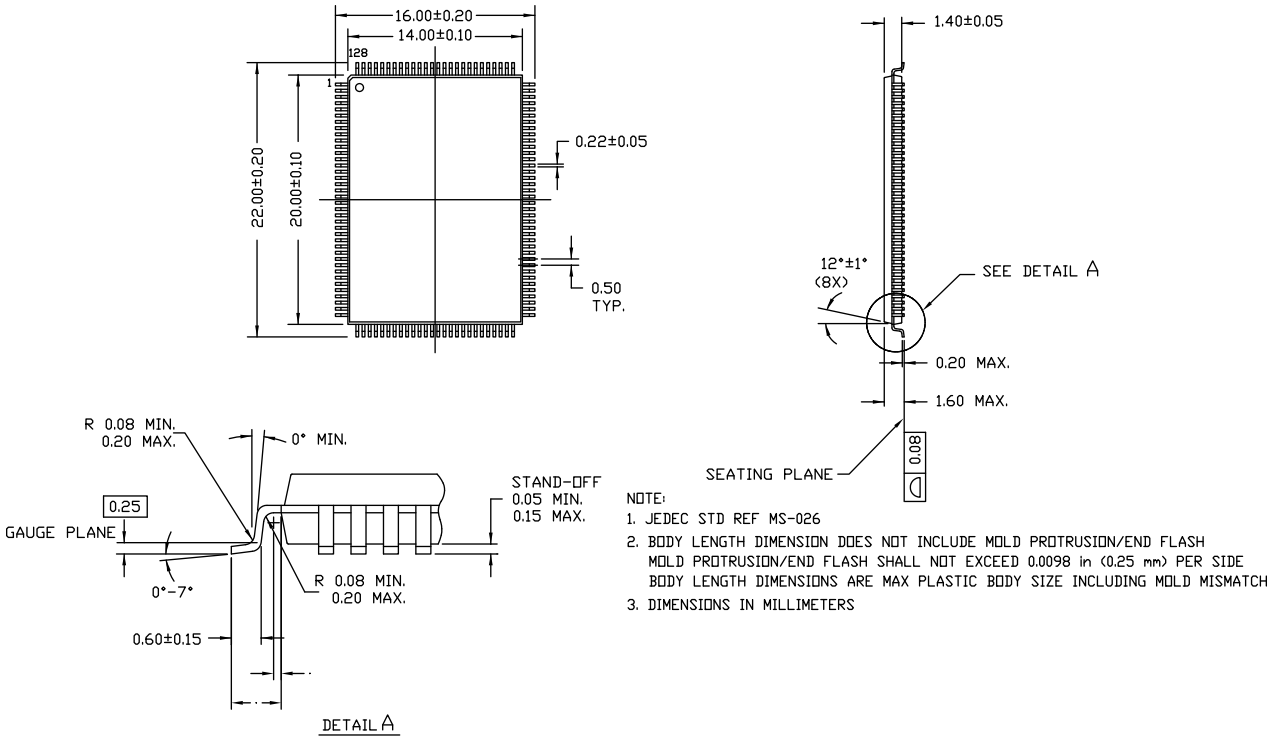
- 56-pin SSOP
- 56-pin QFN
- 100-pin TQFP
- 128-pin TQFP

Figure 36. 56-pin SSOP 300 Mils O563



51-85062 *F

Figure 39. 128-pin TQFP (14 × 20 × 1.4 mm) A128RA



51-85101 *F

Quad Flat Package No Leads (QFN) Package Design Notes

Electrical contact of the part to the Printed Circuit Board (PCB) is made by soldering the leads on the bottom surface of the package to the PCB. As a result, special attention is required to the heat transfer area below the package to provide a good thermal bond to the circuit board. A Copper (Cu) fill is to be designed into the PCB as a thermal pad under the package. Heat is transferred from the FX1 through the device's metal paddle on the bottom side of the package. Heat from here, is conducted to the PCB at the thermal pad. It is then conducted from the thermal pad to the PCB inner ground plane by a 5 × 5 array of via. A via is a plated through hole in the PCB with a finished diameter of 13 mil. The QFN's metal die paddle must be soldered to the PCB's thermal pad. Solder mask is placed on the board top side over each via to resist solder flow into the via. The mask on the top side also minimizes outgassing during the solder reflow process.

For further information on this package design please refer to 'Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages'. This can be found on Amkor's website http://www.amkor.com.

The application note provides detailed information on board mounting guidelines, soldering flow, rework process, and so on.

Figure 40 on page 69 displays a cross-sectional area underneath the package. The cross section is of only one via. The solder paste template needs to be designed to allow at least 50% solder coverage. The thickness of the solder paste template must be 5 mil. It is recommended that 'No Clean' type 3 solder paste is used for mounting the part. Nitrogen purge is recommended during reflow.

Figure 41 on page 69 is a plot of the solder mask pattern and Figure 42 on page 69 displays an X-Ray image of the assembly (darker areas indicate solder).

Document History Page

Document Title: CY7C64713, EZ-USB FX1™ USB Microcontroller Full Speed USB Peripheral Controller Document Number: 38-08039				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	132091	KKU	02/10/04	New data sheet.
*A	230709	KKU	SEE ECN	Changed Lead free Marketing part numbers in Ordering Information according to spec change in 28-00054.
*B	307474	BHA	SEE ECN	Changed default PID in Table 2 on page 5. Updated register table. Removed word compatible where associated with I2C. Changed Set-up to Setup. Added Power Dissipation. Changed Vcc from ± 10% to ± 5% Added values for V_{IH_X}, V_{IL_X} Added values for I_{CC} Added values for I_{SUSP} Removed $I_{UNCONFIGURED}$ from DC Characteristics on page 47. Changed PKTEND to FLAGS output propagation delay (asynchronous interface) in Table 10-14 from a maximum value of 70 ns to 115 ns. Removed 56 SSOP and added 56 QFN package. Provided additional timing restrictions and requirement regarding the use of PKTEND pin to commit a short one byte/word packet subsequent to committing a packet automatically (when in auto mode). Added part number CY7C64714 ideal for battery powered applications. Changed Supply Voltage in section 8 to read +3.15V to +3.45V. Added Min Vcc Ramp Up time (0 to 3.3 V). Removed Preliminary.
*C	392702	BHA	SEE ECN	Corrected signal name for pin 54 in Figure 10 on page 18. Added information on the AUTOPTR1/AUTOPTR2 address timing with regards to data memory read/write timing diagram. Removed TBD in Table 15 on page 53. Added section PORTC Strobe Feature Timings on page 51.
*D	1664787	CMCC/ JASM	See ECN	Added the 56 pin SSOP pinout and package information. Delete CY7C64714.
*E	2088446	JASM	See ECN	Updated package diagrams.
*F	2710327	DPT	05/22/2009	Added 56-Pin QFN (8 × 8 mm) package diagram Updated ordering information for CY7C64713-56LTXC part
*G	2765406	ODC	09/17/2009	Added Pb-free for the CY7C64713-56LTXC part in the ordering information table. Updated 56-Pin Sawn QFN package diagram.
*H	2896318	ODC	03/18/2010	Removed obsolete part CY7C64713-56LFXC. Updated all package diagrams.
*I	3186891	ODC	03/03/2011	Template updates. Updated package diagrams: 51-85144 , 51-85050, 51-85101
*J	3259101	ODC	05/17/2011	Added Ordering Code Definitions. Updated Package Diagrams. Added Acronyms and Units of Measure. Updated in new template.