Infineon Technologies - CY7C64713-56PVXC Datasheet

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Application specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	USB Microcontroller
Core Processor	8051
Program Memory Type	ROMless
Controller Series	CY7C647xx
RAM Size	16K x 8
Interface	I²C, USB, USART
Number of I/O	24
Voltage - Supply	3.15V ~ 3.45V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	56-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	56-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c64713-56pvxc

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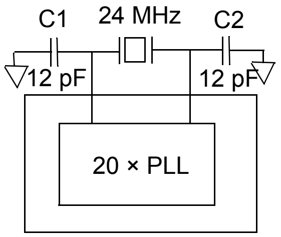
Figure 1. Crystal Configuration



12-pF capacitor values assumes a trace capacitance of 3 pF per side on a four layer FR4 PCA

Table 1. Special Function Registers

x	8x	9x	Ax	Bx	Cx	Dx	Ex	Fx
0	**IOA**	**IOB**	**IOC**	**IOD**	SCON1	PSW	ACC	B
1	SP	**EXIF**	**INT2CLR**	**IOE**	SBUF1			
2	DPL0	**MPAGE**	**INT4CLR**	**OEA**				
3	DPH0			**OEB**				
4	**DPL1**			**OEC**				
5	**DPH1**			**OED**				
6	**DPS**			**OEE**				
7	PCON							
8	TCON	SCON0	IE	IP	T2CON	**EICON**	**EIE**	**EIP**
9	TMOD	SBUF0						
A	TL0	**AUTOPTRH1**	**EP2468STAT**	**EP01STAT**	RCAP2L			
B	TL1	**AUTOPTRL1**	**EP24FIFOFLGS**	**GPIFTRIG**	RCAP2H			
C	TH0	**reserved**	**EP68FIFOFLGS**		TL2			
D	TH1	**AUTOPTRH2**		**GPIFSGLDATH**	TH2			
E	**CKCON**	**AUTOPTRL2**		**GPIFSGLDATLX**				
F		**reserved**	**AUTOPTRSETUP**	**GPIFSGLDATLNOX**				

I^{2}C Bus

FX1 supports the I^{2}C bus as a master only at 100/400 KHz. SCL and SDA pins have open drain outputs and hysteresis inputs. These signals must be pulled up to 3.3 V, even if no I^{2}C device is connected.

Buses

All packages: 8 or 16-bit 'FIFO' bidirectional data bus, multiplexed on I/O ports B and D. 128-pin package: adds 16-bit output only 8051 address bus, 8-bit bidirectional data bus.

USB Boot Methods

During the power up sequence, internal logic checks the I^{2}C port for the connection of an EEPROM whose first byte is either 0xC0 or 0xC2. If found, it uses the VID/PID/DID values in the EEPROM in place of the internally stored values (0xC0). Alternatively, it boot-loads the EEPROM contents into an internal RAM (0xC2). If no EEPROM is detected, FX1 enumerates using internally stored descriptors. The default ID values for FX1 are VID/PID/DID (0x04B4, 0x6473, 0xAxxx where xxx=Chip revision).[2]

Table 2. Default ID Values for FX1

Default VID/PID/DID		
Vendor ID	0x04B4	Cypress Semiconductor
Product ID	0x6473	EZ-USB FX1
Device release	0xAnnn	Depends on chip revision (nnn = chip revision where first silicon = 001)

Notes

[2] The I^{2}C bus SCL and SDA pins must be pulled up, even if an EEPROM is not connected. Otherwise this detection method does not work properly.

Table 3. INT2 USB Interrupts *(continued)*

USB INTERRUPT TABLE FOR INT2			
Priority	**INT2VEC Value**	**Source**	**Notes**
18	44		Reserved
19	48	EP0PING	EP0 OUT was Pinged and it NAK'd
20	4C	EP1PING	EP1 OUT was Pinged and it NAK'd
21	50	EP2PING	EP2 OUT was Pinged and it NAK'd
22	54	EP4PING	EP4 OUT was Pinged and it NAK'd
23	58	EP6PING	EP6 OUT was Pinged and it NAK'd
24	5C	EP8PING	EP8 OUT was Pinged and it NAK'd
25	60	ERRLIMIT	Bus errors exceeded the programmed limit
26	64		
27	68		Reserved
28	6C		Reserved
29	70	EP2ISOERR	ISO EP2 OUT PID sequence error
30	74	EP4ISOERR	ISO EP4 OUT PID sequence error
31	78	EP6ISOERR	ISO EP6 OUT PID sequence error
32	7C	EP8ISOERR	ISO EP8 OUT PID sequence error

Table 4. Individual FIFO/GPIF Interrupt Sources

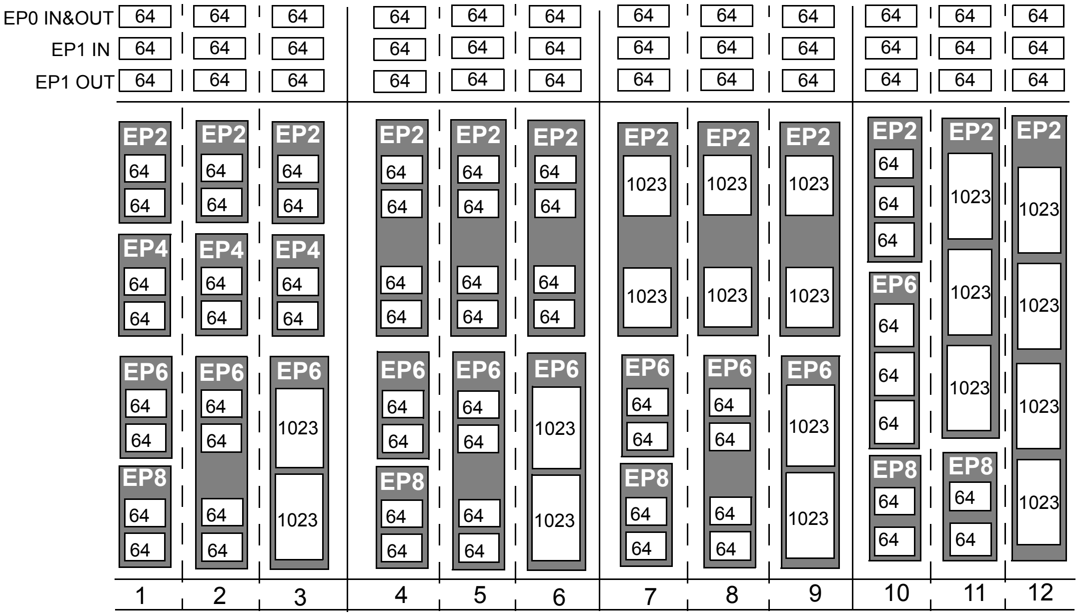
Priority	INT4VEC Value	Source	Notes
1	80	EP2PF	Endpoint 2 Programmable Flag
2	84	EP4PF	Endpoint 4 Programmable Flag
3	88	EP6PF	Endpoint 6 Programmable Flag
4	8C	EP8PF	Endpoint 8 Programmable Flag
5	90	EP2EF	Endpoint 2 Empty Flag [3]
6	94	EP4EF	Endpoint 4 Empty Flag
7	98	EP6EF	Endpoint 6 Empty Flag
8	9C	EP8EF	Endpoint 8 Empty Flag
9	A0	EP2FF	Endpoint 2 Full Flag
10	A4	EP4FF	Endpoint 4 Full Flag
11	A8	EP6FF	Endpoint 6 Full Flag
12	AC	EP8FF	Endpoint 8 Full Flag
13	B0	GPIFDONE	GPIF Operation Complete
14	B4	GPIFWF	GPIF Waveform

If Autovectoring is enabled (AV4EN = 1 in the INTSETUP register), the FX1 substitutes its INT4VEC byte. Therefore, if the high byte ("page") of a jump-table address is preloaded at location 0x0054, the automatically inserted INT4VEC byte at 0x0055 directs the jump to the correct address out of the 14 addresses within the page. When the ISR occurs, the FX1 pushes the program counter onto its stack and then jumps to address 0x0053, where it expects to find a "jump" instruction to the ISR Interrupt service routine.

Note

3. Errata: In Slave FIFO Asynchronous Word Wide mode, if a single word data is transferred from the USB host to EP2, configured as OUT Endpoint (EP) in the first transaction, then the Empty flag behaves incorrectly. This does not happen if the data size is more than one word in the first transaction. For more information, see the "Errata" on page 71.

Figure 6. Endpoint Configuration



Master/Slave Control Signals

The FX1 endpoint FIFOS are implemented as eight physically distinct 256 × 16 RAM blocks. The 8051/SIE can switch any of the RAM blocks between two domains: the USB (SIE) domain and the 8051-I/O Unit domain. This switching is done instantaneously, giving essentially zero transfer time between "USB FIFOS" and "Slave FIFOS". While they are physically the same memory, no bytes are actually transferred between buffers.

At any time, some RAM blocks fill or empty with USB data under SIE control, while other RAM blocks are available to the 8051 and the I/O control unit. The RAM blocks operate as a single-port in the USB domain, and dual port in the 8051-I/O domain. The blocks are configured as single, double, triple, or quad buffered.

The I/O control unit implements either an internal master (M for master) or external master (S for Slave) interface.

In Master (M) mode, the GPIF internally controls FIFOADR[1..0] to select a FIFO. The RDY pins (two in the 56-pin package, six in the 100-pin and 128-pin packages) are used as flag inputs from an external FIFO or other logic if desired. The GPIF is run from either an internally derived clock or an externally supplied clock (IFCLK), at a rate that transfers data up to 96 Megabytes/s (48 MHz IFCLK with 16-bit interface).

In Slave (S) mode, the FX1 accepts either an internally derived clock or an externally supplied clock (IFCLK with a maximum frequency of 48 MHz) and SLCS#, SLRD, SLWR, SLOE, PKTEND signals from external logic. When using an external IFCLK, the external clock must be present before switching to the external clock with the IFCLKSRC bit. Each endpoint can individually be selected for byte or word operation by an internal configuration bit, and a Slave FIFO Output Enable signal SLOE enables data of the selected width. External logic must ensure that the output enable signal is inactive when writing data to a slave FIFO. The slave interface can also operate asynchronously, where the SLRD and SLWR signals act directly as strobes, rather than a clock qualifier as in the synchronous mode. The signals SLRD, SLWR, SLOE, and PKTEND are gated by the signal SLCS#.

GPIF and FIFO Clock Rates

An 8051 register bit selects one of two frequencies for the internally supplied interface clock: 30 MHz and 48 MHz. Alternatively, an externally supplied clock of 5 to 48 MHz feeding the IFCLK pin is used as the interface clock. IFCLK is configured to function as an output clock when the GPIF and FIFOs are internally clocked. An output enable bit in the IFCONFIG register turns this clock output off, if desired. Another bit within the IFCONFIG register inverts the IFCLK signal whether internally or externally sourced.

GPIF

The GPIF is a flexible 8 or 16-bit parallel interface driven by a user programmable finite state machine. It allows the CY7C64713 to perform local bus mastering, and can implement a wide variety of protocols such as ATA interface, printer parallel port, and Utopia.

The GPIF has six programmable control outputs (CTL), nine address outputs (GPIFADRx), and six general purpose Ready inputs (RDY). The data bus width is 8 or 16 bits. Each GPIF vector defines the state of the control outputs, and determines what state a Ready input (or multiple inputs) must be before proceeding. The GPIF vector is programmed to advance a FIFO to the next data value, advance an address, and so on. A sequence of the GPIF vectors create a single waveform that executes to perform the data move between the FX1 and the external device.

Six Control OUT Signals

The 100-pin and 128-pin packages bring out all six Control Output pins (CTL0–CTL5). The 8051 programs the GPIF unit to define the CTL waveforms. The 56-pin package brings out three of these signals: CTL0–CTL2. CTLx waveform edges are programmed to make transitions as fast as once per clock (20.8 ns using a 48 MHz clock).

Six Ready IN Signals

The 100-pin and 128-pin packages bring out all six Ready inputs (RDY0–RDY5). The 8051 programs the GPIF unit to test the RDY pins for GPIF branching. The 56 pin package brings out two of these signals, RDY0–1.

Nine GPIF Address OUT Signals

Nine GPIF address lines are available in the 100-pin and 128-pin packages: GPIFADR[8..0]. The GPIF address lines allow indexing through up to a 512 byte block of RAM. If more address lines are needed, I/O port pins are used.

Long Transfer Mode

In Master mode, the 8051 appropriately sets the GPIF transaction count registers (GPIFTCB3, GPIFTCB2, GPIFTCB1, or GPIFTCB0) for unattended transfers of up to 2^{32} transactions. The GPIF automatically throttles data flow to prevent under or overflow until the full number of requested transactions are complete. The GPIF decrements the value in these registers to represent the current status of the transaction.

ECC Generation

The EZ-USB FX1 can calculate ECCs (Error Correcting Codes) on data that pass across its GPIF or Slave FIFO interfaces. There are two ECC configurations: Two ECCs, each calculated over 256 bytes (SmartMedia™ Standard); and one ECC calculated over 512 bytes.

The ECC can correct any one-bit error or detect any two-bit error.

Note To use the ECC logic, the GPIF or Slave FIFO interface must be configured for byte-wide operation.

ECC Implementation

The two ECC configurations are selected by the ECCM bit:

0.0.0.1 ECCM = 0

Two 3-byte ECCs, each calculated over a 256-byte block of data. This configuration conforms to the SmartMedia Standard.

Write any value to ECCRESET, then pass data across the GPIF or Slave FIFO interface. The ECC for the first 256 bytes of data is calculated and stored in ECC1. The ECC for the next 256 bytes is stored in ECC2. After the second ECC is calculated, the values in the ECCx registers do not change until the ECCRESET is written again, even if more data is subsequently passed across the interface.

0.0.0.2 ECCM = 1

One 3-byte ECC calculated over a 512-byte block of data.

Write any value to ECCRESET, then pass data across the GPIF or Slave FIFO interface. The ECC for the first 512 bytes of data is calculated and stored in ECC1; ECC2 is not used. After the ECC is calculated, the value in ECC1 does not change until the ECCRESET is written again, even if more data is subsequently passed across the interface

USB Uploads and Downloads

The core has the ability to directly edit the data contents of the internal 16 KByte RAM and of the internal 512 byte scratch pad RAM via a vendor specific command. This capability is normally used when ‘soft’ downloading user code and is available only to and from the internal RAM, only when the 8051 is held in reset. The available RAM spaces are 16 KBytes from 0x0000–0x3FFF (code/data) and 512 bytes from 0xE000–0xE1FF (scratch pad data RAM).[5]

Autopointer Access

FX1 provides two identical autopointers. They are similar to the internal 8051 data pointers, but with an additional feature: they can optionally increment after every memory access. This capability is available to and from both internal and external RAM. The autopointers are available in external FX1 registers, under the control of a mode bit (AUTOPTRSETUP.0). Using the external FX1 autopointer access (at 0xE67B–0xE67C) allows the autopointer to access all RAM, internal and external, to the part. Also, the autopointers can point to any FX1 register or endpoint buffer space. When autopointer access to external memory is enabled, the location 0xE67B and 0xE67C in XDATA and the code space cannot be used.

I^{2}C Controller

FX1 has one I^{2}C port that is driven by two internal controllers: one that automatically operates at boot time to load VID/PID/DID and configuration information; and another that the 8051, once running, uses to control external I^{2}C devices. The I^{2}C port operates in master mode only.

I^{2}C Port Pins

The I^{2}C pins SCL and SDA must have external 2.2 kΩ pull up resistors even if no EEPROM is connected to the FX1. External EEPROM device address pins must be configured properly. See Table 7 for configuring the device address pins.

Table 7. Strap Boot EEPROM Address Lines to These Values

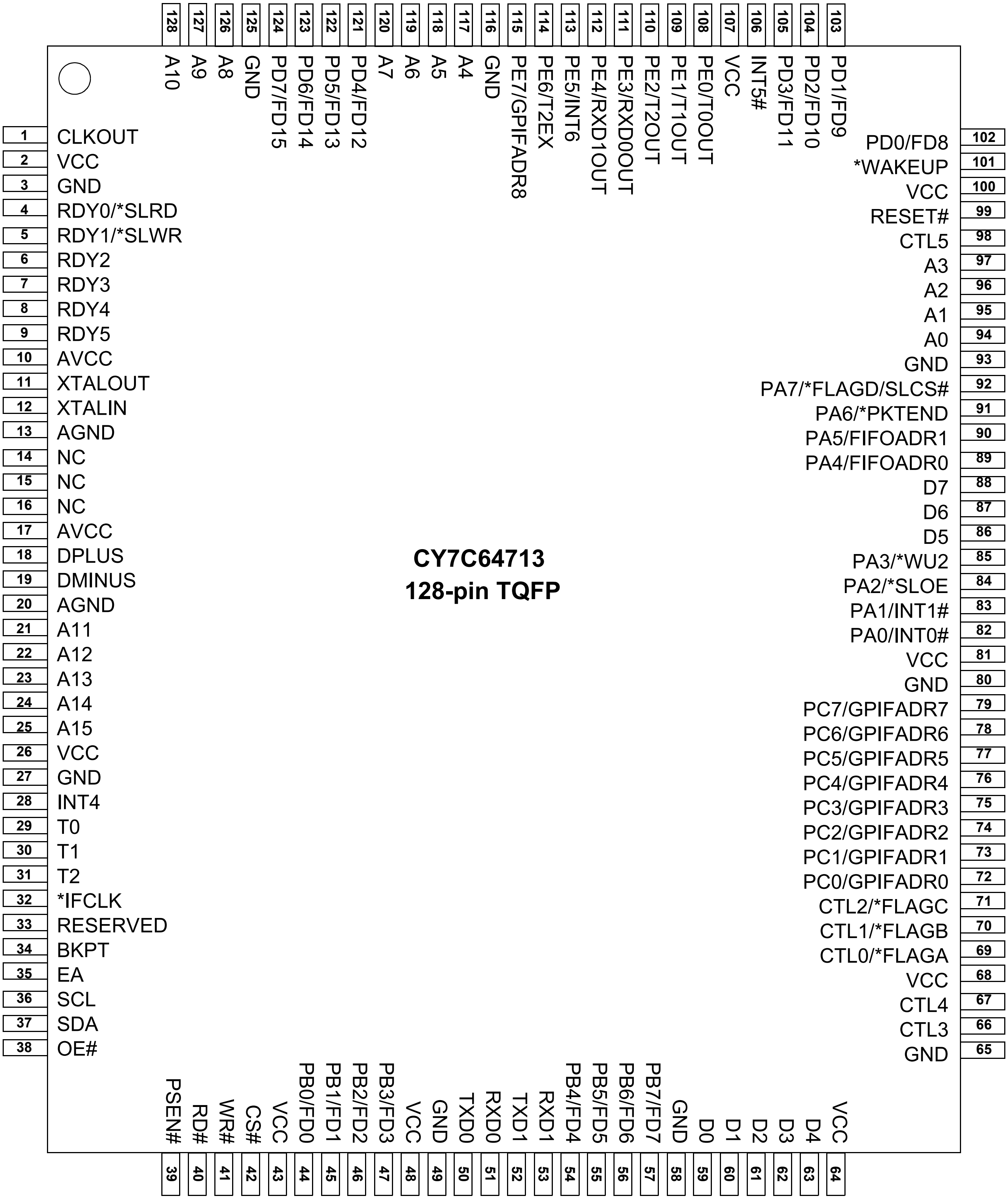
Bytes	Example EEPROM	A2	A1	A0
16	24LC00[6]	N/A	N/A	N/A
128	24LC01	0	0	0
256	24LC02	0	0	0
4K	24LC32	0	0	1
8K	24LC64	0	0	1
16K	24LC128	0	0	1

Notes

[5] After the data is downloaded from the host, a ‘loader’ executes from the internal RAM to transfer downloaded data to the external memory.

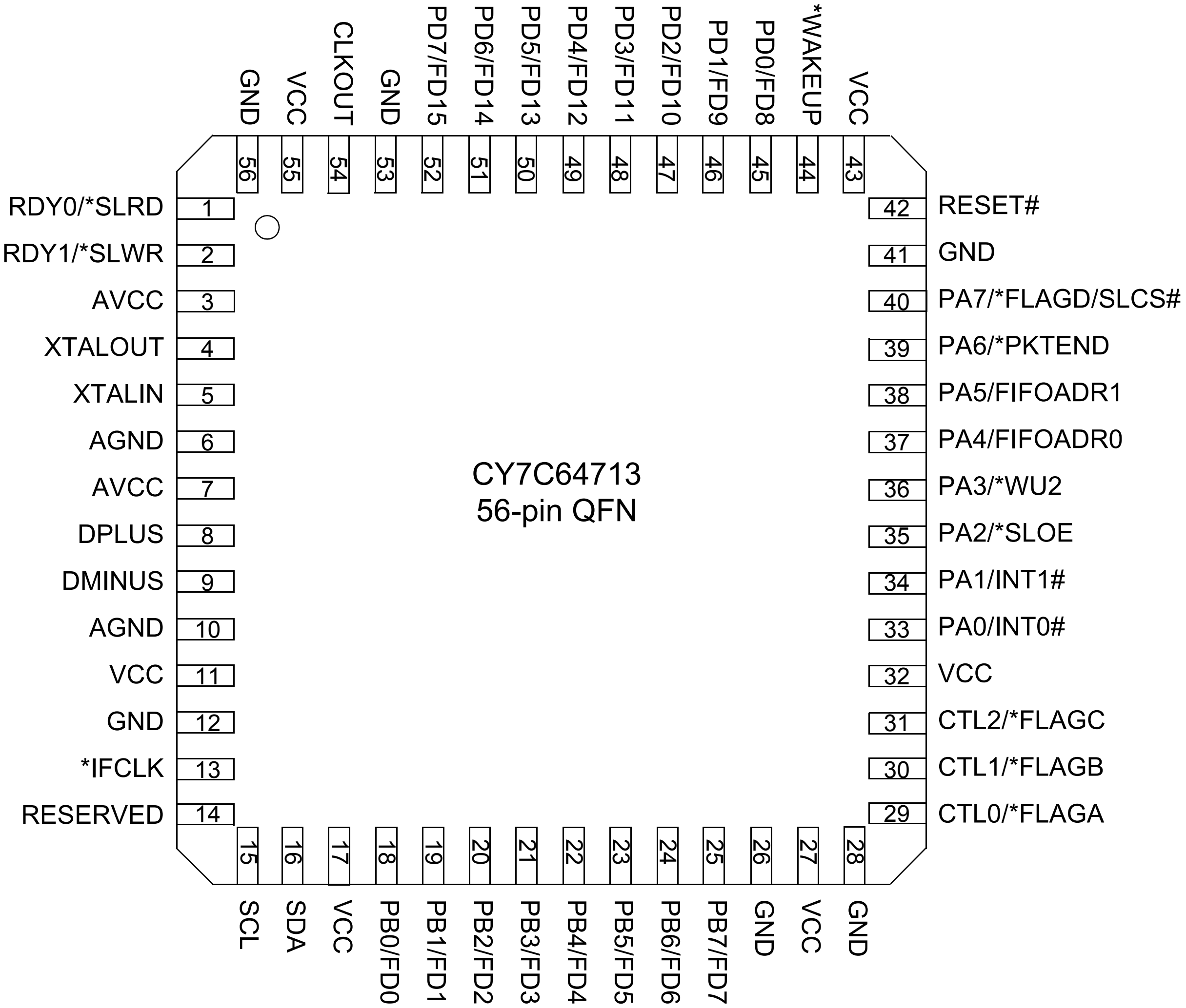
[6] This EEPROM has no address pins.

Figure 8. CY7C64713 128-pin TQFP Pin Assignment


CY7C64713
128-pin TQFP
128 A10
127 A9
126 A8
125 GND
124 PD7/FD15
123 PD6/FD14
122 PD5/FD13
121 PD4/FD12
120 A7
119 A6
118 A5
117 A4
116 GND
115 PE7/GPIFADR8
114 PE6/T2EX
113 PE5/INT6
112 PE4/RXD1OUT
111 PE3/RXD0OUT
110 PE2/T2OUT
109 PE1/T1OUT
108 PE0/T0OUT
107 VCC
106 INT5#
105 PD3/FD11
104 PD2/FD10
103 PD1/FD9
1 CLKOUT
2 VCC
3 GND
4 RDY0/*SLRD
5 RDY1/*SLWR
6 RDY2
7 RDY3
8 RDY4
9 RDY5
10 AVCC
11 XTALOUT
12 XTALIN
13 AGND
14 NC
15 NC
16 NC
17 AVCC
18 DPLUS
19 DMINUS
20 AGND
21 A11
22 A12
23 A13
24 A14
25 A15
26 VCC
27 GND
28 INT4
29 T0
30 T1
31 T2
32 *IFCLK
33 RESERVED
34 BKPT
35 EA
36 SCL
37 SDA
38 OE#
102 PD0/FD8
101 *WAKEUP
100 VCC
99 RESET#
98 CTL5
97 A3
96 A2
95 A1
94 A0
93 GND
92 PA7/*FLAGD/SLCS#
91 PA6/*PKTEND
90 PA5/FIFOADR1
89 PA4/FIFOADR0
88 D7
87 D6
86 D5
85 PA3/*WU2
84 PA2/*SLOE
83 PA1/INT1#
82 PA0/INT0#
81 VCC
80 GND
79 PC7/GPIFADR7
78 PC6/GPIFADR6
77 PC5/GPIFADR5
76 PC4/GPIFADR4
75 PC3/GPIFADR3
74 PC2/GPIFADR2
73 PC1/GPIFADR1
72 PC0/GPIFADR0
71 CTL2/*FLAGC
70 CTL1/*FLAGB
69 CTL0/*FLAGA
68 VCC
67 CTL4
66 CTL3
65 GND
39 PSEN#
40 RD#
41 WR#
42 CS#
43 VCC
44 PB0/FD0
45 PB1/FD1
46 PB2/FD2
47 PB3/FD3
48 VCC
49 GND
50 TXD0
51 RXD0
52 TXD1
53 RXD1
54 PB4/FD4
55 PB5/FD5
56 PB6/FD6
57 PB7/FD7
58 GND
59 D0
60 D1
61 D2
62 D3
63 D4
64 VCC

* indicates programmable polarity

Figure 11. CY7C64713 56-pin QFN Pin Assignment


CY7C64713
56-pin QFN
1 RDY0/*SLRD
2 RDY1/*SLWR
3 AVCC
4 XTALOUT
5 XTALIN
6 AGND
7 AVCC
8 DPLUS
9 DMINUS
10 AGND
11 VCC
12 GND
13 *IFCLK
14 RESERVED
15 SCL
16 SDA
17 VCC
18 PB0/FD0
19 PB1/FD1
20 PB2/FD2
21 PB3/FD3
22 PB4/FD4
23 PB5/FD5
24 PB6/FD6
25 PB7/FD7
26 GND
27 VCC
28 GND
29 CTL0/*FLAGA
30 CTL1/*FLAGB
31 CTL2/*FLAGC
32 VCC
33 PA0/INT0#
34 PA1/INT1#
35 PA2/*SLOE
36 PA3/*WU2
37 PA4/FIFOADR0
38 PA5/FIFOADR1
39 PA6/*PKTEND
40 PA7/*FLAGD/SLCS#
41 GND
42 RESET#
43 VCC
44 *WAKEUP
45 PD0/FD8
46 PD1/FD9
47 PD2/FD10
48 PD3/FD11
49 PD4/FD12
50 PD5/FD13
51 PD6/FD14
52 PD7/FD15
53 GND
54 CLKOUT
55 VCC
56 GND

* indicates programmable polarity

CY7C64713 Pin Definitions

The FX1 Pin Definitions for CY7C64713 follow.[7]

Table 8. FX1 Pin Definitions

128-pin TQFP	100-pin TQFP	56-pin SSOP	56-pin QFN	Name	Type	Default	Description
10	9	10	3	AVCC	Power	N/A	**Analog VCC**. Connect this pin to 3.3 V power source. This signal provides power to the analog section of the chip.
17	16	14	7	AVCC	Power	N/A	**Analog VCC**. Connect this pin to 3.3 V power source. This signal provides power to the analog section of the chip.
13	12	13	6	AGND	Ground	N/A	**Analog Ground**. Connect to ground with as short a path as possible.
20	19	17	10	AGND	Ground	N/A	**Analog Ground**. Connect to ground with as short a path as possible.
19	18	16	9	DMINUS	I/O/Z	Z	**USB D– Signal**. Connect to the USB D– signal.
18	17	15	8	DPLUS	I/O/Z	Z	**USB D+ Signal**. Connect to the USB D+ signal.
94				A0	Output	L	**8051 Address Bus**. This bus is driven at all times. When the 8051 is addressing the internal RAM it reflects the internal address.
95				A1	Output	L	
96				A2	Output	L	
97				A3	Output	L	
117				A4	Output	L	
118				A5	Output	L	
119				A6	Output	L	
120				A7	Output	L	
126				A8	Output	L	
127				A9	Output	L	
128				A10	Output	L	
21				A11	Output	L	
22				A12	Output	L	
23				A13	Output	L	
24				A14	Output	L	
25				A15	Output	L	
59				D0	I/O/Z	Z	**8051 Data Bus**. This bidirectional bus is high impedance when inactive, input for bus reads, and output for bus writes. The data bus is used for external 8051 program and data memory. The data bus is active only for external bus accesses, and is driven LOW in suspend.
60				D1	I/O/Z	Z	
61				D2	I/O/Z	Z	
62				D3	I/O/Z	Z	
63				D4	I/O/Z	Z	
86				D5	I/O/Z	Z	
87				D6	I/O/Z	Z	
88				D7	I/O/Z	Z	
39				PSEN#	Output	H	**Program Store Enable**. This active LOW signal indicates an 8051 code fetch from external memory. It is active for program memory fetches from 0x4000–0xFFFF when the EA pin is LOW, or from 0x0000–0xFFFF when the EA pin is HIGH.

Note

7. Do not leave unused inputs floating. Tie either HIGH or LOW as appropriate. Pull outputs up or down to ensure signals at power up and in standby. Note that no pins must be driven when the device is powered down.

Table 8. FX1 Pin Definitions *(continued)*

128-pin TQFP	100-pin TQFP	56-pin SSOP	56-pin QFN	Name	Type	Default	Description
124	98	3	52	PD7 or FD[15]	I/O/Z	I (PD7)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[15]** is the bidirectional FIFO/GPIF data bus.
Port E							
108	86			PE0 or T0OUT	I/O/Z	I (PE0)	Multiplexed pin whose function is selected by the PORTECFG.0 bit. **PE0** is a bidirectional I/O port pin. **T0OUT** is an active HIGH signal from 8051 Timer-counter0. T0OUT outputs a high level for one CLKOUT clock cycle when Timer0 overflows. If Timer0 is operated in Mode 3 (two separate timer/counters), T0OUT is active when the low byte timer/counter overflows.
109	87			PE1 or T1OUT	I/O/Z	I (PE1)	Multiplexed pin whose function is selected by the PORTECFG.1 bit. **PE1** is a bidirectional I/O port pin. **T1OUT** is an active HIGH signal from 8051 Timer-counter1. T1OUT outputs a high level for one CLKOUT clock cycle when Timer1 overflows. If Timer1 is operated in Mode 3 (two separate timer/counters), T1OUT is active when the low byte timer/counter overflows.
110	88			PE2 or T2OUT	I/O/Z	I (PE2)	Multiplexed pin whose function is selected by the PORTECFG.2 bit. **PE2** is a bidirectional I/O port pin. **T2OUT** is the active HIGH output signal from 8051 Timer2. T2OUT is active (HIGH) for one clock cycle when Timer/Counter 2 overflows.
111	89			PE3 or RXD0OUT	I/O/Z	I (PE3)	Multiplexed pin whose function is selected by the PORTECFG.3 bit. **PE3** is a bidirectional I/O port pin. **RXD0OUT** is an active HIGH signal from 8051 UART0. If RXD0OUT is selected and UART0 is in Mode 0, this pin provides the output data for UART0 only when it is in sync mode. Otherwise it is a 1.
112	90			PE4 or RXD1OUT	I/O/Z	I (PE4)	Multiplexed pin whose function is selected by the PORTECFG.4 bit. **PE4** is a bidirectional I/O port pin. **RXD1OUT** is an active HIGH output from 8051 UART1. When the RXD1OUT is selected and UART1 is in Mode 0, this pin provides the output data for UART1 only when it is in sync mode. In Modes 1, 2, and 3, this pin is HIGH.
113	91			PE5 or INT6	I/O/Z	I (PE5)	Multiplexed pin whose function is selected by the PORTECFG.5 bit. **PE5** is a bidirectional I/O port pin. **INT6** is the 8051 INT6 interrupt request input signal. The INT6 pin is edge-sensitive, active HIGH.
114	92			PE6 or T2EX	I/O/Z	I (PE6)	Multiplexed pin whose function is selected by the PORTECFG.6 bit. **PE6** is a bidirectional I/O port pin. **T2EX** is an active HIGH input signal to the 8051 Timer2. T2EX reloads timer 2 on its falling edge. T2EX is active only if the EXEN2 bit is set in T2CON.
115	93			PE7 or GPIFADR8	I/O/Z	I (PE7)	Multiplexed pin whose function is selected by the PORTECFG.7 bit. **PE7** is a bidirectional I/O port pin. **GPIFADR8** is a GPIF address output pin.

Table 8. FX1 Pin Definitions *(continued)*

128-pin TQFP	100-pin TQFP	56-pin SSOP	56-pin QFN	Name	Type	Default	Description
31	25			T2	Input	N/A	**T2** is the active-HIGH T2 input signal to 8051 Timer2, which provides the input to Timer2 when C/T2 = 1. When C/T2 = 0, Timer2 does not use this pin.
30	24			T1	Input	N/A	**T1** is the active-HIGH T1 signal for 8051 Timer1, which provides the input to Timer1 when C/T1 is 1. When C/T1 is 0, Timer1 does not use this bit.
29	23			T0	Input	N/A	**T0** is the active-HIGH T0 signal for 8051 Timer0, which provides the input to Timer0 when C/T0 is 1. When C/T0 is 0, Timer0 does not use this bit.
53	43			RXD1	Input	N/A	**RXD1** is an active-HIGH input signal for 8051 UART1, which provides data to the UART in all modes.
52	42			TXD1	Output	H	**TXD1** is an active-HIGH output pin from 8051 UART1, which provides the output clock in sync mode, and the output data in async mode.
51	41			RXD0	Input	N/A	**RXD0** is the active-HIGH RXD0 input to 8051 UART0, which provides data to the UART in all modes.
50	40			TXD0	Output	H	**TXD0** is the active-HIGH TXD0 output from 8051 UART0, which provides the output clock in sync mode, and the output data in async mode.
42				CS#	Output	H	**CS#** is the active-LOW chip select for external memory.
41	32			WR#	Output	H	**WR#** is the active-LOW write strobe output for external memory.
40	31			RD#	Output	H	**RD#** is the active-LOW read strobe output for external memory.
38				OE#	Output	H	**OE#** is the active LOW output enable for external memory.
33	27	21	14	Reserved	Input	N/A	**Reserved**. Connect to ground.
101	79	51	44	WAKEUP	Input	N/A	**USB Wakeup**. If the 8051 is in suspend, asserting this pin starts up the oscillator and interrupts the 8051 to allow it to exit the suspend mode. Holding WAKEUP asserted inhibits the EZ-USB FX1 chip from suspending. This pin has programmable polarity (WAKEUP.4).
36	29	22	15	SCL	OD	Z	**Clock for the I^{2}C interface**. Connect to VCC with a 2.2K resistor, even if no I^{2}C peripheral is attached.
37	30	23	16	SDA	OD	Z	**Data for I^{2}C interface**. Connect to VCC with a 2.2K resistor, even if no I^{2}C peripheral is attached.
2	1	6	55	VCC	Power	N/A	**VCC**. Connect to 3.3 V power source.
26	20	18	11	VCC	Power	N/A	**VCC**. Connect to 3.3 V power source.
43	33	24	17	VCC	Power	N/A	**VCC**. Connect to 3.3 V power source.
48	38			VCC	Power	N/A	**VCC**. Connect to 3.3 V power source.
64	49	34	27	VCC	Power	N/A	**VCC**. Connect to 3.3 V power source.
68	53			VCC	Power	N/A	**VCC**. Connect to 3.3 V power source.
81	66	39	32	VCC	Power	N/A	**VCC**. Connect to 3.3 V power source.
100	78	50	43	VCC	Power	N/A	**VCC**. Connect to 3.3 V power source.
107	85			VCC	Power	N/A	**VCC**. Connect to 3.3 V power source.
3	2	7	56	GND	Ground	N/A	**Ground**.
27	21	19	12	GND	Ground	N/A	**Ground**.

Table 9. FX1 Register Summary *(continued)*

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E685	1	USBFRAMEL	USB Frame count L	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	xxxxxxxx	R
E686	1	reserved											
E687	1	FNADDR	USB Function address	0	FA6	FA5	FA4	FA3	FA2	FA1	FA0	0xxxxxxx	R
E688	2	reserved											
		ENDPOINTS											
E68A	1	EP0BCH[18]	Endpoint 0 Byte Count H	(BC15)	(BC14)	(BC13)	(BC12)	(BC11)	(BC10)	(BC9)	(BC8)	xxxxxxxx	RW
E68B	1	EP0BCL[18]	Endpoint 0 Byte Count L	(BC7)	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E68C	1	reserved											
E68D	1	EP1OUTBC	Endpoint 1 OUT Byte Count	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E68E	1	reserved											
E68F	1	EP1INBC	Endpoint 1 IN Byte Count	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E690	1	EP2BCH[18]	Endpoint 2 Byte Count H	0	0	0	0	0	BC10	BC9	BC8	xxxxxxxx	RW
E691	1	EP2BCL[18]	Endpoint 2 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E692	2	reserved											
E694	1	EP4BCH[18]	Endpoint 4 Byte Count H	0	0	0	0	0	0	BC9	BC8	xxxxxxxx	RW
E695	1	EP4BCL[18]	Endpoint 4 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E696	2	reserved											
E698	1	EP6BCH[18]	Endpoint 6 Byte Count H	0	0	0	0	0	BC10	BC9	BC8	xxxxxxxx	RW
E699	1	EP6BCL[18]	Endpoint 6 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E69A	2	reserved											
E69C	1	EP8BCH[18]	Endpoint 8 Byte Count H	0	0	0	0	0	0	BC9	BC8	xxxxxxxx	RW
E69D	1	EP8BCL[18]	Endpoint 8 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E69E	2	reserved											

Note

[18] Read and writes to these register may require synchronization delay, see the section “Synchronization Delay” in the EZ-USB TRM.

Table 9. FX1 Register Summary *(continued)*

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E6AE	1	EP4FIFOBCL	Endpoint 4 slave FIFO total byte count L	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	00000000	R
E6AF	1	EP6FIFOBCH	Endpoint 6 slave FIFO total byte count H	0	0	0	0	BC11	BC10	BC9	BC8	00000000	R
E6B0	1	EP6FIFOBCL	Endpoint 6 slave FIFO total byte count L	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	00000000	R
E6B1	1	EP8FIFOBCH	Endpoint 8 slave FIFO total byte count H	0	0	0	0	0	BC10	BC9	BC8	00000000	R
E6B2	1	EP8FIFOBCL	Endpoint 8 slave FIFO total byte count L	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	00000000	R
E6B3	1	SUDPTRH	Setup Data Pointer high address byte	A15	A14	A13	A12	A11	A10	A9	A8	xxxxxxxx	RW
E6B4	1	SUDPTRL	Setup Data Pointer low address byte	A7	A6	A5	A4	A3	A2	A1	0	xxxxxxx0	bbbbbbbr
E6B5	1	SUDPTRCTL	Setup Data Pointer Auto Mode	0	0	0	0	0	0	0	SDPAUTO	00000001	RW
	2	reserved											
E6B8	8	SETUPDAT	8 bytes of setup data	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	R
			SETUPDAT[0] = bmRequestType										
			SETUPDAT[1] = bmRequest										
			SETUPDAT[2:3] = wValue										
			SETUPDAT[4:5] = wIndex										
			SETUPDAT[6:7] = wLength										
		GPIF											
E6C0	1	GPIFWFSELECT	Waveform Selector	SINGLEWR1	SINGLEWR0	SINGLERD1	SINGLERD0	FIFOWR1	FIFOWR0	FIFORD1	FIFORD0	11100100	RW

Table 9. FX1 Register Summary *(continued)*

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E6C1	1	GPIFIDLECS	GPIF Done, GPIF IDLE drive mode	DONE	0	0	0	0	0	0	IDLEDRV	10000000	RW
E6C2	1	GPIFIDLECTL	Inactive Bus, CTL states	0	0	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0	11111111	RW
E6C3	1	GPIFCTLCFG	CTL Drive Type	TRICTL	0	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0	00000000	RW
E6C4	1	GPIFADRH[19]	GPIF Address H	0	0	0	0	0	0	0	GPIFA8	00000000	RW
E6C5	1	GPIFADRL[19]	GPIF Address L	GPIFA7	GPIFA6	GPIFA5	GPIFA4	GPIFA3	GPIFA2	GPIFA1	GPIFA0	00000000	RW
		FLOWSTATE											
E6C6	1	FLOWSTATE	Flowstate Enable and Selector	FSE	0	0	0	0	FS2	FS1	FS0	00000000	brrrrbbb
E6C7	1	FLOWLOGIC	Flowstate Logic	LFUNC1	LFUNC0	TERMA2	TERMA1	TERMA0	TERMB2	TERMB1	TERMB0	00000000	RW
E6C8	1	FLOWEQ0CTL	CTL-Pin States in Flowstate (when Logic = 0)	CTL0E3	CTL0E2	CTL0E1/CTL5	CTL0E0/CTL4	CTL3	CTL2	CTL1	CTL0	00000000	RW
E6C9	1	FLOWEQ1CTL	CTL-Pin States in Flowstate (when Logic = 1)	CTL0E3	CTL0E2	CTL0E1/CTL5	CTL0E0/CTL4	CTL3	CTL2	CTL1	CTL0	00000000	RW
E6CA	1	FLOWHOLDOFF	Holdoff Configuration	HOPERIOD3	HOPERIOD2	HOPERIOD1	HOPERIOD0	HOSTATE	HOCTL2	HOCTL1	HOCTL0	00000000	RW
E6CB	1	FLOWSTB	Flowstate Strobe Configuration	SLAVE	RDYASYNC	CTLTOGL	SUSTAIN	0	MSTB2	MSTB1	MSTB0	00100000	RW
E6CC	1	FLOWSTBEDGE	Flowstate Rising/Falling Edge Configuration	0	0	0	0	0	0	FALLING	RISING	00000001	rrrrrrbb
E6CD	1	FLOWSTBPERIOD	Master-Strobe Half-Period	D7	D6	D5	D4	D3	D2	D1	D0	00000010	RW
E6CE	1	GPIFTCB3[19]	GPIF Transaction Count Byte 3	TC31	TC30	TC29	TC28	TC27	TC26	TC25	TC24	00000000	RW
E6CF	1	GPIFTCB2[19]	GPIF Transaction Count Byte 2	TC23	TC22	TC21	TC20	TC19	TC18	TC17	TC16	00000000	RW

Note

19. Read and writes to these register may require synchronization delay, see the section “Synchronization Delay” in the EZ-USB TRM.

Table 9. FX1 Register Summary *(continued)*

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
BC	1	reserved											
BD	1	GPIFSGLDATH[27]	GPIF Data H (16-bit mode only)	D15	D14	D13	D12	D11	D10	D9	D8	xxxxxxxx	RW
BE	1	GPIFSGLDATLX[27]	GPIF Data L w/ Trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
BF	1	GPIFSGLDATLNOX[27]	GPIF Data L w/ No Trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	R
C0	1	SCON1[27]	Serial Port 1 Control (bit addressable)	SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	00000000	RW
C1	1	SBUF1[27]	Serial Port 1 Data Buffer	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
C2	6	reserved											
C8	1	T2CON	Timer/Counter 2 Control (bit addressable)	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2	CPRL2	00000000	RW
C9	1	reserved											
CA	1	RCAP2L	Capture for Timer 2, auto-reload, up-counter	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
CB	1	RCAP2H	Capture for Timer 2, auto-reload, up-counter	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
CC	1	TL2	Timer 2 reload L	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
CD	1	TH2	Timer 2 reload H	D15	D14	D13	D12	D11	D10	D9	D8	00000000	RW
CE	2	reserved											
D0	1	PSW	Program Status Word (bit addressable)	CY	AC	F0	RS1	RS0	OV	F1	P	00000000	RW
D1	7	reserved											
D8	1	EICON[27]	External Interrupt Control	SMOD1	1	ERESI	RESI	INT6	0	0	0	01000000	RW
D9	7	reserved											
E0	1	ACC	Accumulator (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW

Note

[27] SFRs not part of the standard 8051 architecture.

PORTC Strobe Feature Timings

The RD# and WR# are present in the 100 pin version and the 128 pin package. In these 100 pin and 128 pin versions, an 8051 control bit is set to pulse the RD# and WR# pins when the 8051 reads from or writes to the PORTC. This feature is enabled by setting the PORTCSTB bit in CPUCS register.

The RD# and WR# strobes are asserted for two CLKOUT cycles when the PORTC is accessed.

The WR# strobe is asserted two clock cycles after the PORTC is updated and is active for two clock cycles after that as shown in Figure 16.

As for read, the value of the PORTC three clock cycles before the assertion of RD# is the value that the 8051 reads in. The RD# is pulsed for 2 clock cycles after 3 clock cycles from the point when the 8051 has performed a read function on PORTC.

In this feature the RD# signal prompts the external logic to prepare the next data byte. Nothing gets sampled internally on assertion of the RD# signal itself. It is just a “prefetch” type signal to get the next data byte prepared. Therefore, using it meets the set up time to the next read.

The purpose of this pulsing of RD# is to let the external peripheral know that the 8051 is done reading PORTC and that the data was latched into the PORTC three CLKOUT cycles prior to asserting the RD# signal. After the RD# is pulsed the external logic may update the data on PORTC.

The timing diagram of the read and write strobing function on accessing PORTC follows. Refer to Figure 13 on page 49 and Figure 14 on page 50 for details on propagation delay of RD# and WR# signals.

Figure 16. WR# Strobe Function when PORTC is Accessed by 8051

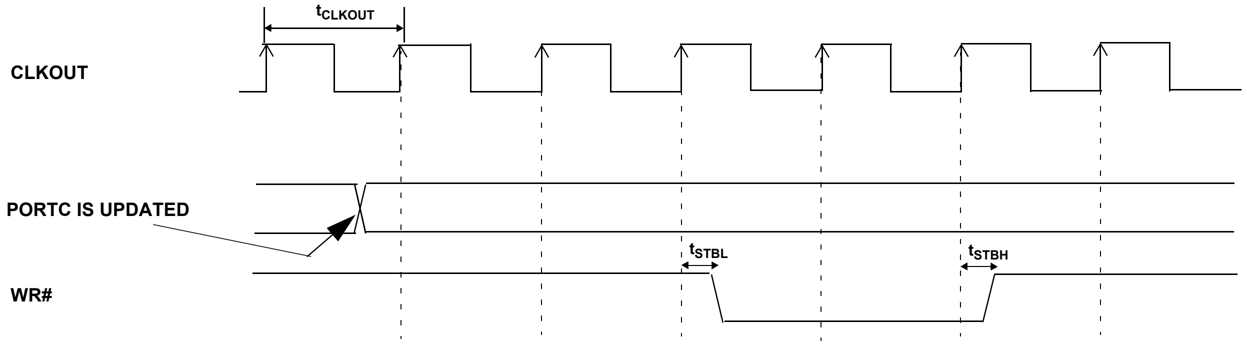
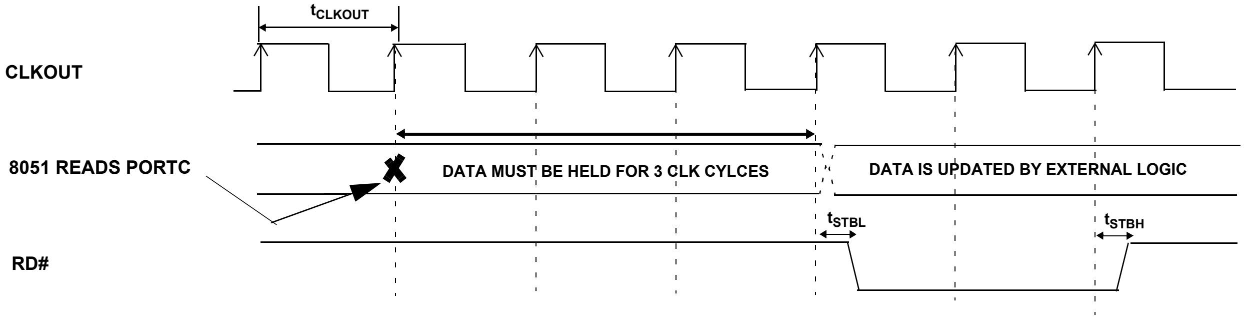


Figure 17. RD# Strobe Function when PORTC is Accessed by 8051

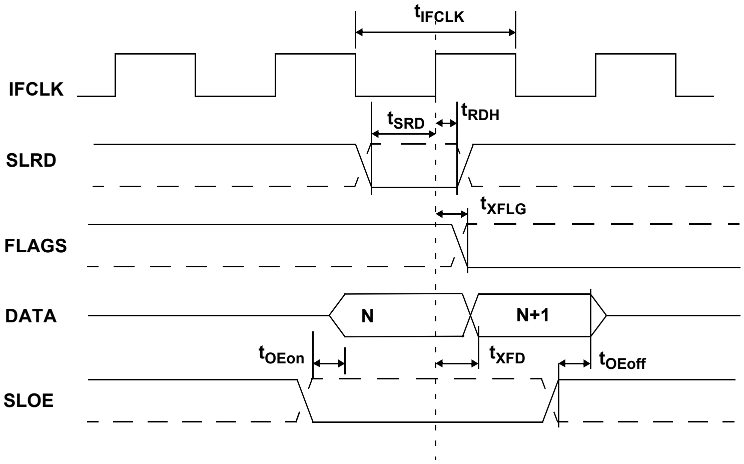


t_{CLKOUT}
CLKOUT
8051 READS PORTC
DATA MUST BE HELD FOR 3 CLK CYLCES
DATA IS UPDATED BY EXTERNAL LOGIC
t_{STBL}
t_{STBH}
RD#

Slave FIFO Synchronous Read

In the following figure, dashed lines indicate signals with programmable polarity.

Figure 19. Slave FIFO Synchronous Read Timing Diagram



The following table provides the Slave FIFO Synchronous Read Parameters with Internally Sourced IFCLK. [36]

Table 15. Slave FIFO Synchronous Read Parameters with Internally Sourced IFCLK

Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK Period	20.83	–	ns
t_{SRD}	SLRD to Clock Setup Time	18.7	–	ns
t_{RDH}	Clock to SLRD Hold Time	0	–	ns
t_{OEon}	SLOE Turn on to FIFO Data Valid	–	10.5	ns
t_{OEoff}	SLOE Turn off to FIFO Data Hold	–	10.5	ns
t_{XFLG}	Clock to FLAGS Output Propagation Delay	–	9.5	ns
t_{XFD}	Clock to FIFO Data Output Propagation Delay	–	11	ns

The following table provides the Slave FIFO Synchronous Read Parameters with Externally Sourced IFCLK.[36]

Table 16. Slave FIFO Synchronous Read Parameters with Externally Sourced IFCLK

Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK Period	20.83	200	ns
t_{SRD}	SLRD to Clock Setup Time	12.7	–	ns
t_{RDH}	Clock to SLRD Hold Time	3.7	–	ns
t_{OEon}	SLOE Turn on to FIFO Data Valid	–	10.5	ns
t_{OEoff}	SLOE Turn off to FIFO Data Hold	–	10.5	ns
t_{XFLG}	Clock to FLAGS Output Propagation Delay	–	13.5	ns
t_{XFD}	Clock to FIFO Data Output Propagation Delay	–	15	ns

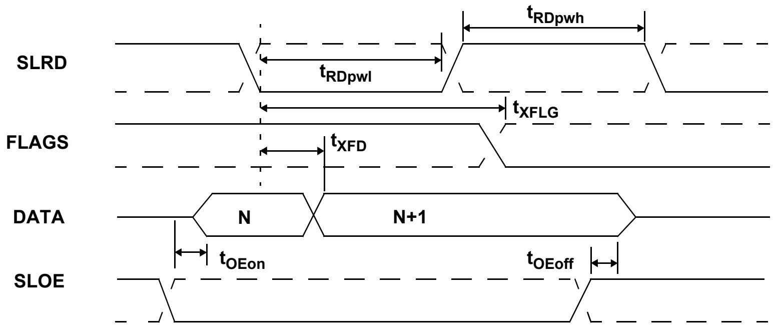
Note

[36] IFCLK must not exceed 48 MHz.

Slave FIFO Asynchronous Read

In the following figure, dashed lines indicate signals with programmable polarity.

Figure 20. Slave FIFO Asynchronous Read Timing Diagram



In the following table, the Slave FIFO asynchronous parameter values use internal IFCLK setting at 48 MHz.

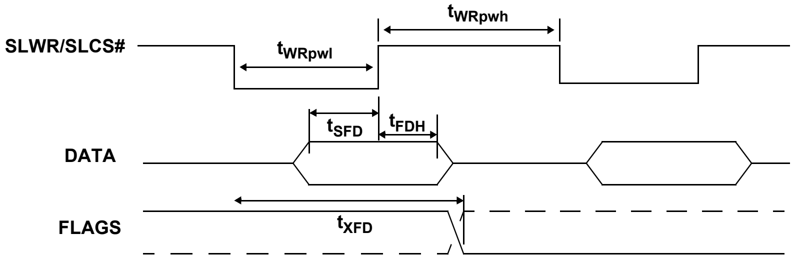
Table 17. Slave FIFO Asynchronous Read Parameters

Parameter	Description	Min	Max	Unit
t_{RDpwl}	SLRD Pulse Width LOW	50	–	ns
t_{RDpwh}	SLRD Pulse Width HIGH	50	–	ns
t_{XFLG}	SLRD to FLAGS Output Propagation Delay	–	70	ns
t_{XFD}	SLRD to FIFO Data Output Propagation Delay	–	15	ns
t_{OEon}	SLOE Turn-on to FIFO Data Valid	–	10.5	ns
t_{OEoff}	SLOE Turn-off to FIFO Data Hold	–	10.5	ns

Slave FIFO Asynchronous Write

In the following figure, dashed lines indicate signals with programmable polarity.

Figure 22. Slave FIFO Asynchronous Write Timing Diagram



In the following table, the Slave FIFO asynchronous parameter values use internal IFCLK setting at 48 MHz.

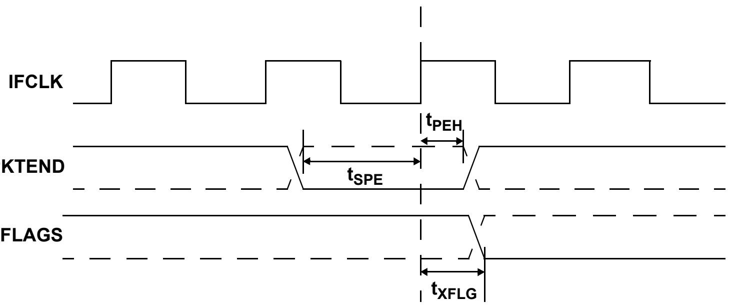
Table 20. Slave FIFO Asynchronous Write Parameters with Internally Sourced IFCLK

Parameter	Description	Min	Max	Unit
t_{WRpwl}	SLWR Pulse LOW	50	–	ns
t_{WRpwh}	SLWR Pulse HIGH	70	–	ns
t_{SFD}	SLWR to FIFO DATA Setup Time	10	–	ns
t_{FDH}	FIFO DATA to SLWR Hold Time	10	–	ns
t_{XFD}	SLWR to FLAGS Output Propagation Delay	–	70	ns

Slave FIFO Synchronous Packet End Strobe

In the following figure, dashed lines indicate signals with programmable polarity.

Figure 23. Slave FIFO Synchronous Packet End Strobe Timing Diagram



The following table provides the Slave FIFO Synchronous Packet End Strobe Parameters with Internally Sourced IFCLK. [38]

Table 21. Slave FIFO Synchronous Packet End Strobe Parameters with Internally Sourced IFCLK

Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK Period	20.83	–	ns
t_{SPE}	PKTEND to Clock Setup Time	14.6	–	ns
t_{PEH}	Clock to PKTEND Hold Time	0	–	ns
t_{XFLG}	Clock to FLAGS Output Propagation Delay	–	9.5	ns

Note

38. IFCLK must not exceed 48 MHz.

Slave FIFO Asynchronous Packet End Strobe

In the following figure, dashed lines indicate signals with programmable polarity.

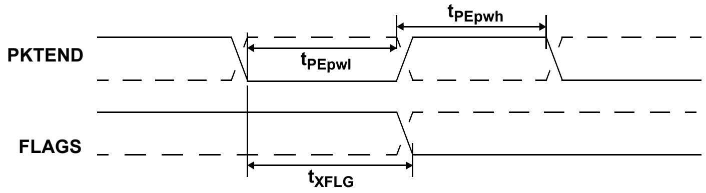


Figure 25. Slave FIFO Asynchronous Packet End Strobe Timing Diagram

In the following table, the Slave FIFO asynchronous parameter values use internal IFCLK setting at 48 MHz.

Table 23. Slave FIFO Asynchronous Packet End Strobe Parameters

Parameter	Description	Min	Max	Unit
t_{PEpwl}	PKTEND Pulse Width LOW	50	–	ns
t_{PWpwh}	PKTEND Pulse Width HIGH	50	–	ns
t_{XFLG}	PKTEND to FLAGS Output Propagation Delay	–	115	ns

Slave FIFO Output Enable

In the following figure, dashed lines indicate signals with programmable polarity.

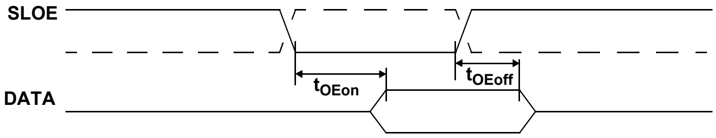


Figure 26. Slave FIFO Output Enable Timing Diagram

Table 24. Slave FIFO Output Enable Parameters

Parameter	Description	Max	Unit
t_{OEon}	SLOE Assert to FIFO DATA Output	10.5	ns
t_{OEoff}	SLOE Deassert to FIFO DATA Hold	10.5	ns

Slave FIFO Address to Flags/Data

In the following figure, dashed lines indicate signals with programmable polarity.

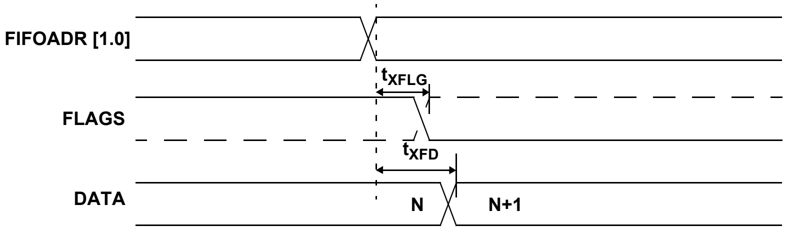


Figure 27. Slave FIFO Address to Flags/Data Timing Diagram

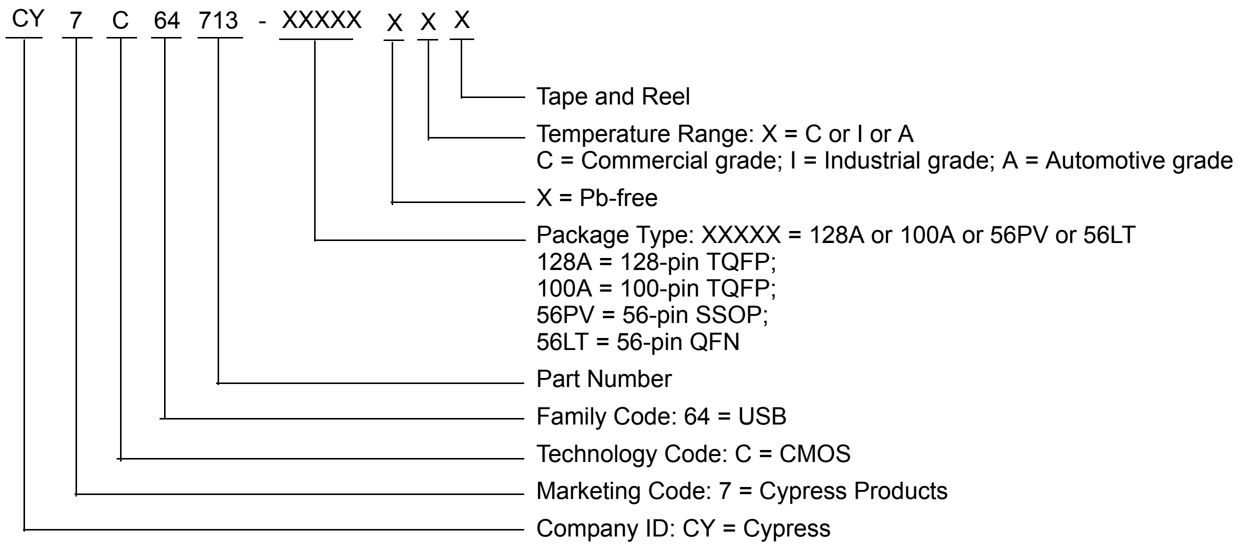
Table 25. Slave FIFO Address to Flags/Data Parameters

Parameter	Description	Max	Unit
t_{XFLG}	FIFOADR[1:0] to FLAGS Output Propagation Delay	10.7	ns
t_{XFD}	FIFOADR[1:0] to FIFODATA Output Propagation Delay	14.3	ns

Ordering Information

Ordering Code	Package Type	RAM Size	# Prog I/Os	8051 Address/Data Busses
CY7C64713-128AXC	128-pin TQFP - Pb-free	16K	40	16/8 bit
CY7C64713-100AXC	100-pin TQFP - Pb-free	16K	40	–
CY7C64713-56PVXC	56-pin SSOP - Pb-free	16K	24	–
CY7C64713-56LTXC	56-pin QFN - Pb-free	16K	24	–
CY3674	EZ-USB FX1 Development Kit			

Ordering Code Definitions



CY 7 C 64 713 - XXXXX X X X

Tape and Reel

Temperature Range: X = C or I or A
C = Commercial grade; I = Industrial grade; A = Automotive grade

X = Pb-free

Package Type: XXXXX = 128A or 100A or 56PV or 56LT
128A = 128-pin TQFP;
100A = 100-pin TQFP;
56PV = 56-pin SSOP;
56LT = 56-pin QFN

Part Number

Family Code: 64 = USB

Technology Code: C = CMOS

Marketing Code: 7 = Cypress Products

Company ID: CY = Cypress

Document History Page

Document Title: CY7C64713, EZ-USB FX1™ USB Microcontroller Full Speed USB Peripheral Controller Document Number: 38-08039				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	132091	KKU	02/10/04	New data sheet.
*A	230709	KKU	SEE ECN	Changed Lead free Marketing part numbers in Ordering Information according to spec change in 28-00054.
*B	307474	BHA	SEE ECN	Changed default PID in Table 2 on page 5. Updated register table. Removed word compatible where associated with I2C. Changed Set-up to Setup. Added Power Dissipation. Changed Vcc from ± 10% to ± 5% Added values for V_{IH_X}, V_{IL_X} Added values for I_{CC} Added values for I_{SUSP} Removed $I_{UNCONFIGURED}$ from DC Characteristics on page 47. Changed PKTEND to FLAGS output propagation delay (asynchronous interface) in Table 10-14 from a maximum value of 70 ns to 115 ns. Removed 56 SSOP and added 56 QFN package. Provided additional timing restrictions and requirement regarding the use of PKTEND pin to commit a short one byte/word packet subsequent to committing a packet automatically (when in auto mode). Added part number CY7C64714 ideal for battery powered applications. Changed Supply Voltage in section 8 to read +3.15V to +3.45V. Added Min Vcc Ramp Up time (0 to 3.3 V). Removed Preliminary.
*C	392702	BHA	SEE ECN	Corrected signal name for pin 54 in Figure 10 on page 18. Added information on the AUTOPTR1/AUTOPTR2 address timing with regards to data memory read/write timing diagram. Removed TBD in Table 15 on page 53. Added section PORTC Strobe Feature Timings on page 51.
*D	1664787	CMCC/ JASM	See ECN	Added the 56 pin SSOP pinout and package information. Delete CY7C64714.
*E	2088446	JASM	See ECN	Updated package diagrams.
*F	2710327	DPT	05/22/2009	Added 56-Pin QFN (8 × 8 mm) package diagram Updated ordering information for CY7C64713-56LTXC part
*G	2765406	ODC	09/17/2009	Added Pb-free for the CY7C64713-56LTXC part in the ordering information table. Updated 56-Pin Sawn QFN package diagram.
*H	2896318	ODC	03/18/2010	Removed obsolete part CY7C64713-56LFXC. Updated all package diagrams.
*I	3186891	ODC	03/03/2011	Template updates. Updated package diagrams: 51-85144 , 51-85050, 51-85101
*J	3259101	ODC	05/17/2011	Added Ordering Code Definitions. Updated Package Diagrams. Added Acronyms and Units of Measure. Updated in new template.