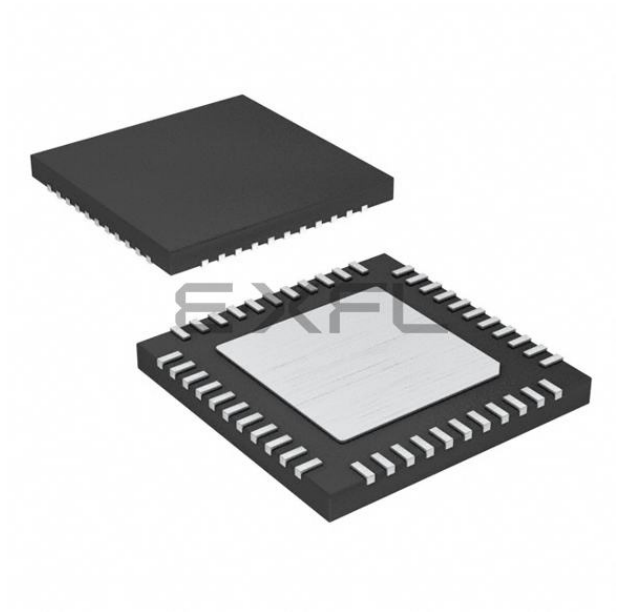
Analog Devices Inc./Maxim Integrated - MAXQ612J-0000+ Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MAXQ20S
Core Size	16-Bit
Speed	12MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Infrared, Power-Fail, POR, WDT
Number of I/O	32
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.75V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-WFQFN Exposed Pad
Supplier Device Package	44-TQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/maxq612j-0000

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RECOMMENDED OPERATING CONDITIONS (continued)

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Hysteresis (Schmitt)	V_{IHYS}			300		mV
Input Low Voltage for HFXIN	V_{IL_HFXIN}	External driven clock and not feedback connected crystal oscillator	V_{GND}		0.3 x V_{DD}	V
Input High Voltage for HFXIN	V_{IH_HFXIN}	External driven clock and not feedback connected crystal oscillator	0.7 x V_{DD}		V_{DD}	V
IRRX Input Filter Pulse-Width Reject	t_{IRRX_R}				50	ns
IRRX Input Filter Pulse-Width Accept	t_{IRRX_A}		300			ns
Output Low Voltage for IRTX	V_{OL_IRTX}	V_{DD} = 3.6V, I_{OL} = 25mA (Note 6)			1.0	V
		V_{DD} = 2.35V, I_{OL} = 10mA (Note 6)			1.0	
		V_{DD} = 1.85V, I_{OL} = 4.5mA			1.0	
Output Low Voltage for $\overline{RESET}$ and All Port Pins (Note 12)	V_{OL}	V_{DD} = 3.6V, I_{OL} = 11mA (Note 6)		0.4	0.5	V
		V_{DD} = 2.35V, I_{OL} = 8mA (Note 6)		0.4	0.5	
		V_{DD} = 1.85V, I_{OL} = 4.5mA		0.4	0.5	
Output High Voltage for IRTX and All Port Pins	V_{OH}	I_{OH} = -2mA	V_{DDIO} - 0.5		V_{DDIO}	V
Input/Output Pin Capacitance for All Port Pins Except DP, DM	C_{IO}	(Note 6)			15	pF
Input Leakage Current	I_L	Internal pullup disabled	-100		+100	nA
Input Pullup Resistor for $\overline{RESET}$, IRTX, IRRX, P0 to P6	R_{PU}	V_{DD} = 3V, V_{OL} = V_{DD}/2 (Note 6)	16	25	39	kΩ
		V_{DD} = 2V, V_{OL} = V_{DD}/2	17	27	41	
		V_{DD} = 3.0V, V_{OL} = 0.4V (Note 6)	16	28	39	
		V_{DD} = 2.0V, V_{OL} = 0.4V (Note 6)	17	30	41	
GPIO Supply Output High Voltage	V_{DDIOH}	V_{DDIOH} current is the sum of V_{DDIO} current and I_{OH} of all GPIO, I_{OH} = 10mA	V_{DD} - 0.4		V_{DD}	V
EXTERNAL CRYSTAL/RESONATOR						
Crystal/Resonator	f_{HFXIN}	(Note 13)	1		12	MHz
Crystal/Resonator Period	t_{HFXIN}			1/f_{HFXIN}		ns
Crystal/Resonator Warmup Time	t_{XTAL_RDY}	From initial oscillation		8192 x t_{HFXIN}		ms
Oscillator Feedback Resistor	R_{OSCF}	(Note 6)	0.5	1.0	1.5	MΩ
Crystal ESR		(Note 6)			60	Ω
EXTERNAL CLOCK INPUT						
External Clock Frequency	f_{XCLK}	(Note 13)	DC		12	MHz
External Clock Period	t_{XCLK}			1/f_{XCLK}		ns
External Clock Duty Cycle	t_{XCLK_DUTY}		45		55	%
System Clock Frequency	f_{CK}			f_{HFXIN}		MHz
		HFXOUT = GND		f_{XCLK}		

RECOMMENDED OPERATING CONDITIONS (continued)

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
System Clock Period	t_{CK}			$1/f_{CK}$		ns
NANOPOWER RING						
Nanopower Ring Frequency	f_{NANO}	T_A = +25°C	3	13	20	kHz
		T_A = +25°C, V_{DD} = POR voltage (Note 6)	1.7	2.4		
Nanopower Ring Duty Cycle	t_{NANO}	(Note 6)	40		60	%
Nanopower Ring Current	I_{NANO}	Typical at V_{DD} = 1.64V, T_A = +25°C (Note 6)		40	400	nA
WAKE-UP TIMER						
Wake-Up Timer Interval	t_{WAKEUP}		$1/f_{NANO}$		$65,535/f_{NANO}$	s
FLASH MEMORY						
System Clock During Flash Programming/Erase	$f_{FPSYSCLK}$		1			MHz
Flash Erase Time	t_{ME}	Mass erase	20		40	ms
	t_{ERASE}	Page erase	20		40	
Flash Programming Time per Word	t_{PROG}	(Note 14)	20		100	µs
Write/Erase Cycles			20,000			Cycles
Data Retention		T_A = +25°C	100			Years
USB						
USB Supply Voltage	V_{BUS}	(Note 15)	4.5	5.0	5.5	V
V_{BUS} Supply Current (Note 16)	I_{VBUS}	Transmitting on DP and DM at 12Mbps, C_L = 50pF on DP and DM to GND, FRCVDD = 0			13.5	mA
		Transmitting on DP and DM at 12Mbps, C_L = 50pF on DP and DM to GND, FRCVDD = 1			3.5	mA
V_{BUS} Supply Current During Idle (Note 16)	I_{VBUSID}	DP = high, DM = low, FRCVDD = 0 (Note 6)			6	mA
		DP = high, DM = low, FRCVDD = 1			0.2	mA
V_{BUS} Suspend Supply Current	$I_{VBUSSUS}$				500	µA
Single-Ended Input High Voltage DP, DM	V_{IHD}		2.0			V
Single-Ended Input Low Voltage DP, DM	V_{ILD}				0.8	V
Output Low Voltage DP, DM	V_{OLD}	R_L = 1.5kΩ from DP to 3.6V			0.3	V
Output High Voltage DP, DM	V_{OHD}	R_L = 15kΩ from DP and DM to GND	2.8			V
Differential Input Sensitivity DP, DM	V_{DI}	DP to DM	0.2			V
Common-Mode Voltage Range	V_{CM}	Includes V_{DI} range	0.8		2.5	V

RECOMMENDED OPERATING CONDITIONS (continued)

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Single-Ended Receiver Threshold	V_{SE}		0.8		2.0	V
Single-Ended Receiver Hysteresis	V_{SEH}			200		mV
Differential Output Signal Cross-Point Voltage	V_{CRS}	C_L = 50pF (Note 6)	1.3		2.0	V
DP, DM Off-State Input Impedance	R_{LZ}		300			kΩ
Driver Output Impedance	R_{DRV}	Steady-state drive	28		44	Ω
DP Pullup Resistor	R_{PU}	Idle	0.9		1.575	kΩ
		Receiving	1.425		3.090	
USB TIMING						
DP, DM Rise Time (Transmit)	t_R	C_L = 50pF	4		20	ns
DP, DM Fall Time (Transmit)	t_F	C_L = 50pF	4		20	ns
Rise/Fall Time Matching (Transmit)	t_R/t_F	C_L = 50pF (Note 6)	90		110	%
IR						
Carrier Frequency	f_{IR}				$f_{CK}/2$	Hz
SPI (Note 6)						
SPI Master Operating Frequency	$1/t_{MCK}$				$f_{CK}/2$	MHz
SPI Slave Operating Frequency	$1/t_{SCK}$				$f_{CK}/4$	MHz
SPI I/O Rise/Fall Time	t_{SPI_RF}	C_L = 15pF, pullup = 560Ω	8		24	ns
SCLK_ Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$ - t_{SPI_RF}			ns
MOSI_ Output Hold Time After SCLK_ Sample Edge	t_{MOH}		$t_{MCK}/2$ - t_{SPI_RF}			ns
MOSI_ Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$ - t_{SPI_RF}			ns
MISO_ Input Valid to SCLK_ Sample Edge Rise/Fall Setup	t_{MIS}		25			ns
MISO_ Input to SCLK_ Sample Edge Rise/Fall Hold	t_{MIH}		0			ns
SCLK_ Inactive to MOSI_ Inactive	t_{MLH}		$t_{MCK}/2$ - t_{SPI_RF}			ns
SCLK_ Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		ns
$\overline{SSEL}$_ Active to First Shift Edge	t_{SSE}		t_{SPI_RF}			ns

I²C BUS CONTROLLER TIMING

(Notes 6, 21) (Figure 2)

PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		UNITS
		MIN	MAX	MIN	MAX	
I²C Bus Operating Frequency	f_{I2C}	0	100	0	400	kHz
System Frequency	f_{SYS}	0.90		3.60		MHz
I²C Bit Rate	f_{I2C}		$f_{SYS}/8$		$f_{SYS}/8$	Hz
Hold Time After (Repeated) START	$t_{HD:STA}$	4.0		0.6		µs
Clock Low Period	t_{LOW_I2C}	4.7		1.3		µs
Clock High Period	t_{HIGH_I2C}	4.0		0.6		µs
Setup Time for Repeated START	$t_{SU:STA}$	4.7		0.6		µs
Hold Time for Data (Notes 22, 23)	$t_{HD:DAT}$	0	3.45	0	0.9	µs
Setup Time for Data (Note 24)	$t_{SU:DAT}$	250		100		ns
SDA/SCL Fall Time (Note 20)	t_{F_I2C}		300	$20 + 0.1C_B$	300	ns
SDA/SCL Rise Time (Note 20)	t_{R_I2C}		1000	$20 + 0.1C_B$	300	ns
Setup Time for STOP	$t_{SU:STO}$	4.0		0.6		µs
Bus Free Time Between STOP and START	t_{BUF}	4.7		1.3		µs
Capacitive Load for Each Bus Line	C_B		400		400	pF
Noise Margin at the Low Level for Each Connected Device (Including Hysteresis)	V_{nL_I2C}	$0.1 \times V_{DD}$		$0.1 \times V_{DD}$		V
Noise Margin at the Low Level for Each Connected Device (Including Hysteresis)	V_{nH_I2C}	$0.2 \times V_{DD}$		$0.2 \times V_{DD}$		V

Note 1: Specifications to 0°C are guaranteed by design and are not production tested.

Note 2: V_{PFW} can be programmed to the following nominal voltage trip points: 1.8V, 1.9V, 2.55V, and 2.75V ±3%. The values listed in the *Recommended Operating Conditions* table are for the default configuration of 1.8V nominal.

Note 3: It is not recommended to write to flash when the supply voltage drops below the power-fail warning levels, as there is uncertainty in the duration of continuous power supply. The user application should check the status of the power-fail warning flag before writing to flash to ensure complete write operations.

Note 4: The power-fail warning monitor and the power-fail reset monitor are designed to track each other with a minimum delta between the two of 0.11V.

Note 5: The power-fail reset and POR detectors are designed to operate in tandem to ensure that one or both of these signals is active at all times when $V_{DD} < V_{RST}$, ensuring the device maintains the reset state until minimum operating voltage is achieved.

Note 6: Guaranteed by design and not production tested.

Note 7: I_{S1} is measured with the USB data RAM powered down.

Note 8: The power-check interval (PCI) can be set to always on, or to 1024, 2048, or 4096 nanopower ring clock cycles.

Note 9: Measured on the V_{DD} pin and the device not in reset. All inputs are connected to GND or V_{DD}. Outputs do not source/sink any current. The device is executing code from flash memory.

Note 10: Current consumption during POR when powering up while V_{DD} is less than the POR release voltage.

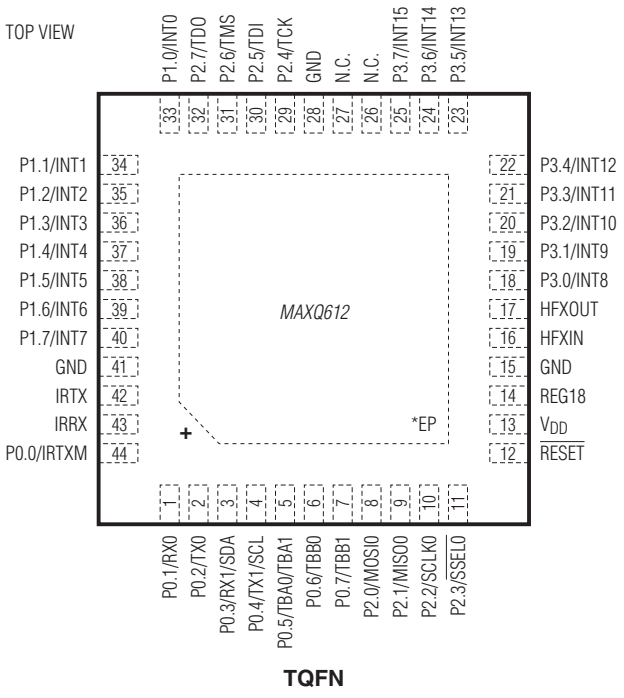
Note 11: The minimum amount of time that V_{DD} must be below V_{PFW} before a power-fail event is detected.

Note 12: The maximum total current, $I_{OH(MAX)}$ and $I_{OL(MAX)}$, for all listed outputs combined should not exceed 25mA to satisfy the maximum specified voltage drop. This does not include the IRTX output.

Note 13: External clock frequency must be 12MHz to support USB functionality. Full-speed USB(12Mbps)-required bit-rate accuracy is ±2500ppm or ±0.25%. This is inclusive of all potential error sources: frequency tolerance, temperature, aging, crystal capacitive loading, board layout, etc.

Note 14: Programming time does not include overhead associated with utility ROM interface.

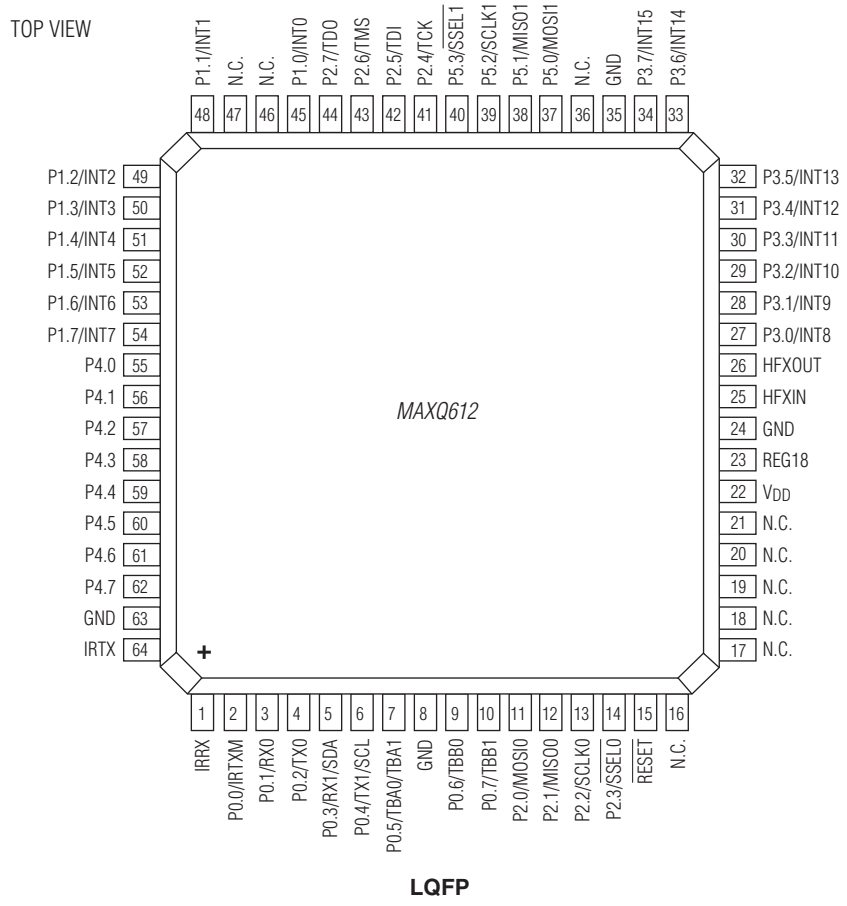
Pin Configurations



TQFN

*EXPOSED PAD.

Pin Configurations (continued)



LQFP

Pin Descriptions—TQFN, LQFP (continued)

PIN			NAME	FUNCTION
MAXQ612 TQFN-EP	MAXQ612 LQFP	MAXQ622 LQFP		
RESET PINS				
12	15	15	$\overline{\text{RESET}}$	Digital, Active-Low, Reset Input/Output. The CPU is held in reset when this pin is low and begins executing from the reset vector when released. The pin includes pullup current source and should be driven by an open-drain, external source capable of sinking in excess of 4mA. This pin is driven low as an output when an internal reset condition occurs.
CLOCK PINS				
16	25	25	HFXIN	High-Frequency Crystal Input. Connect an external crystal or resonator between HFXIN and HFXOUT as the high-frequency system clock. Alternatively, HFXIN is the input for an external, high-frequency clock source when HFXOUT is shorted to ground during POR.
17	26	26	HFXOUT	
USB FUNCTION PINS				
—	—	19	V_{BUS}	USB V_{BUS} Supply Voltage. Connect V_{BUS} to a positive 5.0V power supply. Bypass V_{BUS} to ground with a 1.0µF ceramic capacitor as close to the V_{BUS} pin as possible.
—	—	16	DP	USB D+ Signal. This bidirectional pin carries the positive differential data or single-ended data. Connect this pin to a USB “B” connector. This pin is weakly pulled high internally when the USB is disabled.
—	—	18	DM	USB D- Signal. This bidirectional pin carries the negative differential data or single-ended data. Connect this pin to a USB “B” connector. This pin is weakly pulled high internally when the USB is disabled.
—	—	20	V_{DDB}	USB Transceiver Supply Voltage. This is the power output of the internal voltage regulator that is used for the USB transceiver (3.3V) block. This pin is bypassed to ground with a 1.0µF capacitor as close as possible to the package. No external circuitry should be powered from this pin.
—	—	21	V_{DDIO}	Switched 3V Power Supply. This is the power output after selection between V_{BUS} and V_{DD}. Must be connected to an external ceramic chip capacitor. The capacitor must be placed as close to this pin as possible. No external devices other than the capacitor should be connected to this pin.
IR FUNCTION PINS				
42	64	64	IRTX	IR Transmit Output. Active-low IR transmit pin capable of sinking 25mA. This pin defaults to three-state input with the weak pullup disabled during all forms of reset. Software must configure this pin after release from reset to remove the three-state input condition.
43	1	1	IRRX	IR Receive Input

Pin Descriptions—TQFN, LQFP (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>MAXQ612 TQFN-EP</th><th>MAXQ612 LQFP</th><th>MAXQ622 LQFP</th></tr>
<tr><td colspan="6">GENERAL-PURPOSE I/O AND SPECIAL FUNCTION PINS</td></tr>
<tr><td rowspan="9">44, 1–7</td><td rowspan="9">2–7, 9, 10</td><td rowspan="9">2–7, 9, 10</td><td rowspan="9">P0.0–P0.7; IRTXM, RX0, TX0, RX1, TX1, SDA, SCL, TBA0, TBA1, TBB0, TBB1</td><td>General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. All port pins default to three-state mode after a reset. All alternate functions must be enabled from software.
MAXQ612 TQFN-EP | MAXQ612 LQFP | MAXQ622 LQFP | PORT | SPECIAL FUNCTION
44 | 2 | 2 | P0.0 | IRTXM
1 | 3 | 3 | P0.1 | RX0
2 | 4 | 4 | P0.2 | TX0
3 | 5 | 5 | P0.3 | RX1/SDA
4 | 6 | 6 | P0.4 | TX1/SCL
5 | 7 | 7 | P0.5 | TBA0/TBA1
6 | 9 | 9 | P0.6 | TBB0
7 | 10 | 10 | P0.7 | TBB1</td></tr>
<tr><td rowspan="9">33–40</td><td rowspan="9">45, 48–54</td><td rowspan="9">45, 48–54</td><td rowspan="9">P1.0–P1.7; INT0–INT7</td><td>General-Purpose, Digital, I/O, Type D Port; External Edge-Selectable Interrupt. These port pins function as bidirectional I/O pins or as interrupts. All port pins default to three-state mode after a reset. All interrupt functions must be enabled from software.
MAXQ612 TQFN-EP | MAXQ612 LQFP | MAXQ622 LQFP | PORT | SPECIAL FUNCTION
33 | 45 | 45 | P1.0 | INT0
34 | 48 | 48 | P1.1 | INT1
35 | 49 | 49 | P1.2 | INT2
36 | 50 | 50 | P1.3 | INT3
37 | 51 | 51 | P1.4 | INT4
38 | 52 | 52 | P1.5 | INT5
39 | 53 | 53 | P1.6 | INT6
40 | 54 | 54 | P1.7 | INT7</td></tr>
</table>

Pin Descriptions—Bare Die

PIN		NAME	FUNCTION
MAXQ612	MAXQ622		
POWER PINS			
28	28	V_{DD}	Supply Voltage
8, 30, 45, 73	8, 23, 30, 45, 73	GND	Ground
29	29	REG18	Regulator Capacitor. This pin must be connected to ground through a 1.0µF external ceramic-chip capacitor. The capacitor must be placed as close to this pin as possible. No external devices other than the capacitor should be connected to this pin.
RESET PINS			
21	21	$\overline{RESET}$	Digital, Active-Low, Reset Input/Output. The CPU is held in reset when this pin is low and begins executing from the reset vector when released. The pin includes pullup current source and should be driven by an open-drain, external source capable of sinking in excess of 4mA. This pin is driven low as an output when an internal reset condition occurs.
CLOCK PINS			
31	31	HFXIN	High-Frequency Crystal Input. Connect an external crystal or resonator between HFXIN and HFXOUT as the high-frequency system clock. Alternatively, HFXIN is the input for an external, high-frequency clock source when HFXOUT is shorted to ground during POR.
32	32	HFXOUT	
USB FUNCTION PINS			
—	25	V_{BUS}	USB V_{BUS} Supply Voltage. Connect V_{BUS} to a positive 5.0V power supply. Bypass V_{BUS} to ground with a 1.0µF ceramic capacitor as close to the V_{BUS} pin as possible.
—	22	DP	USB D+ Signal. This bidirectional pin carries the positive differential data or single-ended data. Connect this pin to a USB “B” connector. This pin is weakly pulled high internally when the USB is disabled.
—	24	DM	USB D- Signal. This bidirectional pin carries the negative differential data or single-ended data. Connect this pin to a USB “B” connector. This pin is weakly pulled high internally when the USB is disabled.
—	26	V_{DDB}	USB Transceiver Supply Voltage. This is the power output of the internal voltage regulator that is used for the USB transceiver (3.3V) block. This pin is bypassed to ground with a 1.0µF capacitor as close as possible to the package. No external circuitry should be powered from this pin.
—	27	V_{DDIO}	Switched 3V Power Supply. This is the power output after selection between V_{BUS} and V_{DD}. Must be connected to an external ceramic chip capacitor. The capacitor must be placed as close to this pin as possible. No external devices other than the capacitor should be connected to this pin.

Pin Descriptions—Bare Die (continued)

<table>
<tr><th colspan="2">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>MAXQ612</th><th>MAXQ622</th></tr>
<tr><td rowspan="11">16, 18, 19, 20, 50, 51, 53, 54</td><td rowspan="11">16, 18, 19, 20, 50, 51, 53, 54</td><td rowspan="11">P2.0–P2.7; MOSI0, MISO0, SCLK0, $\overline{SSEL0}$, TCK, TDI, TMS, TDO</td><td>General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. P2.0 to P2.3 default to three-state mode after a reset. All alternate functions must be enabled from software. Enabling the pin's special function disables the general-purpose I/O on the pin.
The JTAG pins (P2.4 to P2.7) default to their JTAG function with weak pullups enabled after a reset. The JTAG function can be disabled using the TAP bit in the SC register.
P2.7 functions as the JTAG test-data output on reset and defaults to an input with a weak pullup. The output function of the test data is only enabled during the TAP's shift_IR or shift_DR states.</td></tr>
<tr><td>
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<tr><th>MAXQ612</th><th>MAXQ622</th><th>PORT</th><th>SPECIAL FUNCTION</th></tr>
<tr><td>16</td><td>16</td><td>P2.0</td><td>MOSI0</td></tr>
<tr><td>18</td><td>18</td><td>P2.1</td><td>MISO0</td></tr>
<tr><td>19</td><td>19</td><td>P2.2</td><td>SCLK0</td></tr>
<tr><td>20</td><td>20</td><td>P2.3</td><td>$\overline{SSEL0}$</td></tr>
<tr><td>50</td><td>50</td><td>P2.4</td><td>TCK</td></tr>
<tr><td>51</td><td>51</td><td>P2.5</td><td>TDI</td></tr>
<tr><td>53</td><td>53</td><td>P2.6</td><td>TMS</td></tr>
<tr><td>54</td><td>54</td><td>P2.7</td><td>TDO</td></tr>
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</td></tr>
<tr><td rowspan="11">33–37, 39, 40, 42</td><td rowspan="11">33–40</td><td rowspan="11">P3.0–P3.7; INT8–INT15</td><td>General-Purpose, Digital, I/O, Type D Port; External Edge-Selectable Interrupt. These port pins function as bidirectional I/O pins or as interrupts. All port pins default to three-state mode after a reset. All interrupt functions must be enabled from software.</td></tr>
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<tr><td>34</td><td>34</td><td>P3.1</td><td>INT9</td></tr>
<tr><td>35</td><td>35</td><td>P3.2</td><td>INT10</td></tr>
<tr><td>36</td><td>36</td><td>P3.3</td><td>INT11</td></tr>
<tr><td>37</td><td>37</td><td>P3.4</td><td>INT12</td></tr>
<tr><td>39</td><td>38</td><td>P3.5</td><td>INT13</td></tr>
<tr><td>40</td><td>39</td><td>P3.6</td><td>INT14</td></tr>
<tr><td>42</td><td>40</td><td>P3.7</td><td>INT15</td></tr>
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<tr><td rowspan="11">65–72</td><td rowspan="11">65–72</td><td rowspan="11">P4.0–P4.7</td><td>General-Purpose, Digital, I/O, Type C Port. These port pins function as bidirectional I/O pins. All port pins default to three-state mode after a reset.</td></tr>
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<tr><td>65</td><td>65</td><td>P4.0</td><td>—</td></tr>
<tr><td>66</td><td>66</td><td>P4.1</td><td>—</td></tr>
<tr><td>67</td><td>67</td><td>P4.2</td><td>—</td></tr>
<tr><td>68</td><td>68</td><td>P4.3</td><td>—</td></tr>
<tr><td>69</td><td>69</td><td>P4.4</td><td>—</td></tr>
<tr><td>70</td><td>70</td><td>P4.5</td><td>—</td></tr>
<tr><td>71</td><td>71</td><td>P4.6</td><td>—</td></tr>
<tr><td>72</td><td>72</td><td>P4.7</td><td>—</td></tr>
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</td></tr>
</table>

The IR timer is composed of a carrier generator and a carrier modulator. The carrier generation module uses the 16-bit IR carrier register (IRCA) to define the high and low time of the carrier through the IR carrier high byte (IRCAH) and IR carrier low byte (IRCAL). The carrier modulator uses the IR data bit (IRDATA) and IR modulator time register (IRMT) to determine whether the carrier or the idle condition is present on IRTX.

Carrier Generation Module

The IRCAH byte defines the carrier high time in terms of the number of IR input clocks, whereas the IRCAL byte defines the carrier low time.

- IR Input Clock (f_{IRCLK}) = $f_{SYS}/2^{IRDIV[1:0]}$
- Carrier Frequency ($f_{CARRIER}$) = f_{IRCLK}/(IRCAH + IRCAL + 2)
- Carrier High Time = IRCAH + 1
- Carrier Low Time = IRCAL + 1
- Carrier Duty Cycle = (IRCAH + 1)/(IRCAH + IRCAL + 2)

During transmission, the IRCA register is latched for each IRV downcount interval, and is sampled along with the IRTXPOL and IRDATA bits at the beginning of each new IRV downcount interval so that duty-cycle variation and frequency shifting is possible from one interval to the next. The starting/idle state and the carrier polarity of the IRTX pin can be configured when the IR timer is enabled.

IR Transmission

During IR transmission (IRMODE = 1), the carrier generator creates the appropriate carrier waveform, while the carrier modulator performs the modulation. The carrier modulation can be performed as a function of carrier cycles or IRCLK cycles dependent on the setting of the IRCFME bit. When IRCFME = 0, the IRV down counter is clocked by the carrier frequency and thus the modulation is a function of carrier cycles. When IRCFME = 1, the IRV down counter is clocked by IRCLK, allowing carrier modulation timing with IRCLK resolution.

The IRTXPOL bit defines the starting/idle state as well as the carrier polarity for the IRTX pin. If IRTXPOL = 1, the IRTX pin is set to a logic-high when the IR timer module is enabled. If IRTXPOL = 0, the IRTX pin is set to a logic-low when the IR timer is enabled.

A separate register bit, IR data (IRDATA), is used to determine whether the carrier generator output is output to the IRTX pin for the next IRMT carrier cycles. When IRDATA = 1, the carrier waveform (or inversion of this waveform if IRTXPOL = 1) is output on the IRTX pin during the next IRMT cycles. When IRDATA = 0, the idle condition, as defined by IRTXPOL, is output on the IRTX pin during the next IRMT cycles.

The IR timer acts as a down counter in transmit mode. An IR transmission starts when the IREN bit is set to 1 when IRMODE = 1; when the IRMODE bit is set to 1 when IREN = 1; or when IREN and IRMODE are both set to 1 in the same instruction. The IRMT and IRCA registers, along with the IRDATA and IRTXPOL bits, are sampled at the beginning of the transmit process and every time the IR timer value reload its value. When the IRV reaches 0000h value, on the next carrier clock, it does the following:

1) Reloads IRV with IRMT.
2) Samples IRCA, IRDATA, and IRTXPOL.
3) Generates IRTX accordingly.
4) Sets IRIF to 1.
5) Generates an interrupt to the CPU if enabled (IRIE = 1).

IR Transmit—Independent External Carrier and Modulator Outputs

The normal transmit mode modulates the carrier based upon the IRDATA bit. However, the user has the option to input the modulator (envelope) on an external pin if desired. The IRDATA bit is output directly to the IRTXM pin (if IRTXPOL = 0) on each IRV downcount interval boundary just as if it were being used to internally modulate the carrier frequency. If IRTXPOL = 1, the inverse of the IRDATA bit is output to the IRTXM pin on the IRV interval downcount boundaries. When the envelope mode is enabled, it is possible to output either the modulated (IRENV[1:0] = 01b) or unmodulated (INENV[1:0] = 10b) carrier to the IRTX pin.

IR Receive

When configured in receive mode (IRMODE = 0), the IR hardware supports the IRRX capture function. The IRRXSEL[1:0] bits define which edge(s) of the IRRX pin should trigger the IR timer capture function. Once started, the IR timer (IRV) starts up counting from 0000h when a qualified capture event as defined by IRRXSEL happens. The IRV register is, by default, counting carrier cycles as defined by the IRCA register. However, the IR carrier frequency detect (IRCFME) allows clocking of the IRV register directly with the IRCLK for finer resolution. When IRCFME = 0, the IRCA defined carrier is counted by IRV. When IRCFME = 1, the IRCLK clocks the IRV register.

On the next qualified event, it does the following:

1) Captures the IRRX pin state and transfers its value to IRDATA. If a falling edge occurs, IRDATA = 0. If a rising edge occurs, IRDATA = 1.

2) Transfers its current IRV value to the IRMT.

3) Resets IRV content to 0000h (if IRXRL = 1).

4) Continues counting again until the next qualified event.

If the IR timer value rolls over from 0FFFFh to 0000h before a qualified event happens, the IR timer overflow (IROV) flag is set to 1 and an interrupt is generated, if enabled. The IR module continues to operate in receive mode until it is stopped by switching into transmit mode or clearing IREN = 0.

Carrier Burst-Count Mode

A special mode reduces the CPU processing burden when performing IR learning functions. Typically, when operating in an IR learning capacity, some number of carrier cycles are examined for frequency determination. Once the frequency has been determined, the IR receive function can be reduced to counting the number of carrier pulses in the burst and the duration of the combined mark-space time within the burst. To simplify this process, the receive burst-count mode can be used. When RXBCNT = 0, the standard IR receive capture functionality is in place. When RXBCNT = 1, the IRV capture operation is disabled and the interrupt flag associated with the capture no longer denotes a capture. In the carrier burst-count mode, the IRMT register only counts qualified edges. The IRIF interrupt flag now sets if two IRCA cycles elapse without getting a qualified edge. The IRIF interrupt flag thus denotes absence of the carrier and the beginning of a space in the receive signal. The IRCFME bit is still used to define whether the IRV register is counting system IRCLK clocks or IRCA-defined carrier cycles. The IRXRL bit defines whether the IRV register is reloaded with 0000h on detection of a qualified edge (per the IRXSEL[1:0] bits).

16-Bit Timers/Counters

The microcontroller provides two general-purpose timers/counters that support the following functions:

- 16-bit timer/counter
- 16-bit up/down autoreload
- Counter function of external pulse
- 16-bit timer with capture
- 16-bit timer with compare
- Input/output enhancements for pulse-width modulation
- Set/reset/toggle output state on comparator match
- Prescaler with 2n divider (for n = 0, 2, 4, 6, 8, 10)

General-Purpose I/O

The microcontroller provides port pins for general-purpose I/O that have the following features:

- CMOS output drivers
- Schmitt trigger inputs
- Optional weak pullup to V_{DD} when operating in input mode

While the microcontroller is in a reset state, all port pins become three-state with both weak pullups and input buffers disabled, unless otherwise noted.

From a software perspective, each port appears as a group of peripheral registers with unique addresses. Special function pins can also be used as general-purpose I/O pins when the special functions are disabled. For a detailed description of the special functions available for each pin, refer to the IC-specific user's guide, e.g., the *MAXQ622 User's Guide* describes all special functions available on the MAXQ612/MAXQ622.

Serial Peripherals

The microcontroller supports two independent USARTs, two SPI master/slave communications ports, and an I^2C bus.

USART

The USART units are implemented with the following characteristics:

- 2-wire interface
- Full-duplex operation for asynchronous data transfers
- Half-duplex operation for synchronous data transfers
- Programmable interrupt for receive and transmit
- Independent baud-rate generator

Table 3. USART Mode Details

MODE	TYPE	START BITS	DATA BITS	STOP BITS
Mode 0	Synchronous	N/A	8	N/A
Mode 1	Asynchronous	1	8	1
Mode 2	Asynchronous	1	8 + 1	1
Mode 3	Asynchronous	1	8 + 1	1

- Programmable 9th bit parity support
- Start/stop bit support

Serial Peripheral Interface (SPI)

The dual-integrated SPI interfaces provide independent serial communication channels that communicate synchronously with peripheral devices in a multiple master or multiple slave system. The interface allows access to a 4-wire, full-duplex serial bus, and can be operated in either master mode or slave mode. Collision detection is provided when two or more masters attempt a data transfer at the same time.

The maximum SPI master transfer rate is Sysclk/2. When operating as an SPI slave, the MAXQ612/MAXQ622 can support up to Sysclk/4 SPI transfer rate. Data is transferred as an 8-bit or 16-bit value, MSB first. In addition, the SPI module supports configuration of an active $\overline{SSEL}$ state through the slave active select. Separate pins and registers are used to differentiate between the two SPI ports.

I²C Bus

The microcontroller integrates an internal I²C bus master/slave for communication with a wide variety of other I²C–enabled peripherals. The I²C bus is a 2-wire, bidirectional bus using two bus lines—the serial data line (SDA) and the serial clock line (SCL)—and a ground line. Both the SDA and SDL lines must be driven as open-collector/drain outputs. External resistors are required as shown in Figure 1 to pull the lines to a logic-high state.

The device supports both the master and slave protocols. In the master mode, the device has ownership of the I²C bus, drives the clock, and generates the START and STOP signals. This allows it to send data to a slave or receive data from a slave as required. In slave mode, the device relies on an externally generated clock to drive SCL and responds to data and commands only when requested by the I²C master device.

USB Controller (MAXQ622 Only)

The integrated USB controller is compliant with the USB 2.0 specification, providing full-speed operation with the newest generation of USB peripherals. The USB controller functions as a full-speed USB peripheral device. Integrating the USB physical interface (PHY) allows direct connection to the USB cable, reducing board space and overall system cost. A system interrupt can be enabled to signal that the USB needs to be serviced. The CPU communicates to the USB controller module through the SFR interface. The microcontroller is seen by a USB host as a peripheral, characterized by the following endpoints:

- EP0: Bidirectional CONTROL endpoint with a 64-byte data storage.
- EP1-OUT: BULK (or INT) OUT endpoint. Double-buffered 64 bytes data storage.
- EP2-IN: BULK (or INT) IN endpoint. Double-buffered 64 bytes data storage.
- EP3-IN: BULK (or INT) IN endpoint. Single-buffered 64 bytes data storage.

The choice to use EP1, EP2, and EP3 as BULK or INTERRUPT endpoints is strictly a function of the endpoint descriptors that the USB controller returns to the USB host during enumeration.

The USB controller communicates to a total of 384 bytes of endpoint data memory (2 x 64 bytes for each data moving endpoint EP1 and EP2), 64 bytes for the CONTROL endpoint, and 64 bytes for endpoint EP3.

Double-buffering EP1 and EP2 improves throughput by allowing the CPU to read or load the next packet while the USB controller is moving the current packet over USB. EP3-IN is intended to serve as a large interrupt endpoint for various USB class specifications such as the Still Image Capture Device. It can also be used as a second BULK IN endpoint.

On-Chip Oscillator

An external quartz crystal or a ceramic resonator can be connected between HFXIN and HFXOUT, as illustrated in Figure 3.

To operate the core from an external clock, connect the clock source to the HFXIN pin and connect the HFXOUT

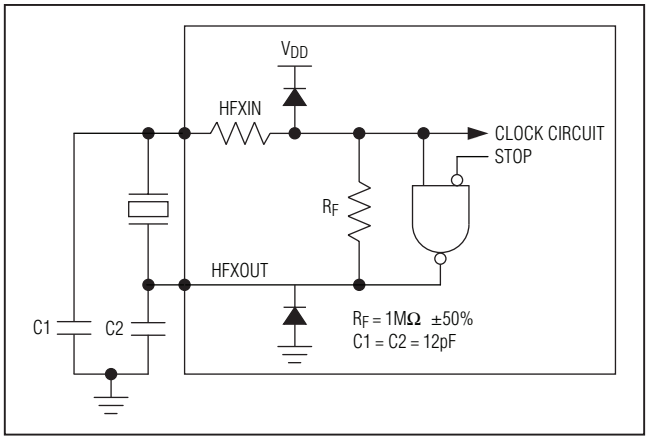


Figure 3. On-Chip Oscillator

pin to GND. The clock source should be driven through a CMOS driver. If the clock driver is a TTL gate, its output must be connected to V_{DD} through a pullup resistor to ensure a satisfactory logic level for active clock pulses. To minimize system noise on the clock circuitry, the external clock source must meet the maximum rise and fall times and the minimum high and low times specified for the clock source. The external noise can affect the clock generation circuit if these parameters do not meet the specification.

Noise at HFXIN and HFXOUT can adversely affect on-chip clock timing. It is good design practice to place the crystal and capacitors as near the oscillator circuitry as possible with a direct short trace. The typical values of external capacitors vary with the type of crystal to be used.

ROM Loader

The ROM loader loads program memory and configures loader-specific configuration features. To increase the security of the system, the loader denies access to the system, user loader, or user-application memories unless an area-specific password is provided.

Loading Flash Memory

An internal bootstrap loader allows reloading over a simple JTAG interface. As a result, software can be upgraded in-system, eliminating the need for a costly hardware retrofit when updates are required. Remote software uploads are possible that enable physically inaccessible applications to be frequently updated. The interface hardware can be a JTAG connection to another microcontroller, or a connection to a PC serial port using a USB-to-JTAG converter such as the MAXQUSBJTAG-KIT#, available from Maxim. If in-system programmability is not required, a commercial gang programmer can be used for mass programming. Activating the JTAG interface and loading the test access port (TAP) with the system programming instruction invokes the bootstrap loader. Setting the SPE bit to one during reset through the JTAG interface executes the bootstrap-loader mode program that resides in the utility ROM. When programming is complete, the bootstrap loader can clear the SPE bit and reset the device, allowing the device to bypass the utility ROM and begin execution of the application software.

In addition, the ROM loader also enforces the memory-protection policies. Passwords that are 16 words are required to access the ROM loader interface.

_In-Application Flash Programming

From user-application code, flash memory can be programmed using the ROM utility functions from either C or assembly language. The function declarations below show examples of some of the ROM utility functions provided for in-application flash memory programming:

```
/* Write one 16-bit word to code address 'dest'.
* Dest must be aligned to 16 bits.
* Returns 0 = failure, 1 = OK.
*/
int flash_write (uint16_t dest, uint16_t data);
```

To erase, the following function would be used:

```
/* Erase the given Flash page
* addr: Flash offset (anywhere within page)
*/
int flash_erasepage(uint16_t addr);
```

The in-application flash memory programming must call ROM utility functions to erase and program any of the flash memory. Memory protection is enforced by the ROM utility functions.

In-Circuit Debug and JTAG Interface

Embedded debug hardware and software are developed and integrated to provide full in-circuit debugging capability in a user-application environment. These hardware and software features include the following:

- Debug engine
- Set of registers providing the ability to set breakpoints on register, code, or data using debug service routines stored in ROM

Collectively, these hardware and software features support two modes of in-circuit debug functionality:

- Background mode:

  CPU is executing the normal user program

  Allows the host to configure and set up the in-circuit debugger
- Debug mode:

  Debugger takes over the control of the CPU

  Read/write accesses to internal registers and memory

  Single-step of the CPU for trace operation

The interface to the debug engine is the TAP controller. The interface allows for communication with a bus

Table 4. Power-Fail Warning Level Selection

PWCN.PFWARNCN[1:0]	PFW THRESHOLD (V)
00	1.8
01	1.9
10	2.55
11	2.75

mode to minimize power consumption. This feature is enabled using the power-fail monitor disable (PFD) bit in the PWCN register. The reset default state for the PFD bit is 1, which disables the power-fail monitor function during stop mode. If power-fail monitoring is disabled (PFD = 1) during stop mode, the circuitry responsible for generating a power-fail warning or reset is shut down and neither condition is detected. Thus, the $V_{DD} < V_{RST}$ condition does not invoke a reset state. However, in the event that V_{DD} falls below the POR level, a POR is generated. The power-fail monitor is enabled prior to stop mode exit and before code execution begins. If a power-fail warning condition ($V_{DD} < V_{PFW}$) is then detected, the power-fail interrupt flag is set on stop mode exit. If a power-fail reset condition is detected ($V_{DD} < V_{RST}$), the CPU goes into reset.

Power-Fail Warning

The power-fail monitor can assert an interrupt if the voltage falls below a configurable threshold between the operating voltage and the reset voltage. This, if enabled, can allow the firmware to perform housekeeping tasks if the voltage level decays below the warning threshold. The power-fail threshold value should only be changed when the power-fail warning interrupt is disabled (CKCN. PFIE = 0) to prevent unintended triggering of the power-fail warning condition.

The power-fail warning threshold is reset to 1.8V by a POR and is not affected by other resets. See Table 4.

Power-Fail Detection

Figures 5, 6, and 7 show the power-fail detection and response during normal and stop-mode operation.

If a reset is caused by a power-fail, the power-fail monitor can be set to one of the following intervals:

- Always on—continuous monitoring
- 2^{11} nanopower ring oscillator clocks (~256ms)
- 2^{12} nanopower ring oscillator clocks (~512ms)
- 2^{13} nanopower ring oscillator clocks (~1.024s)

In the case where the power-fail circuitry is periodically turned on, the power-fail detection is turned on for two

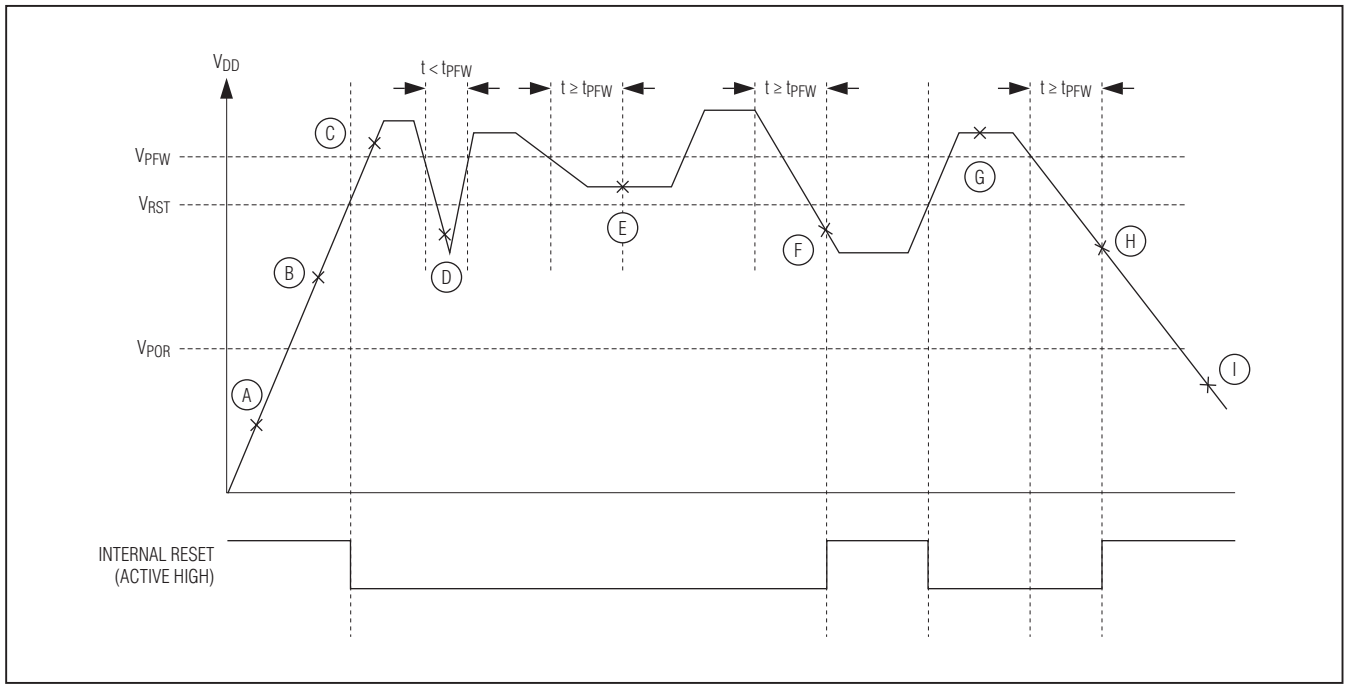


Figure 5. Power-Fail Detection During Normal Operation

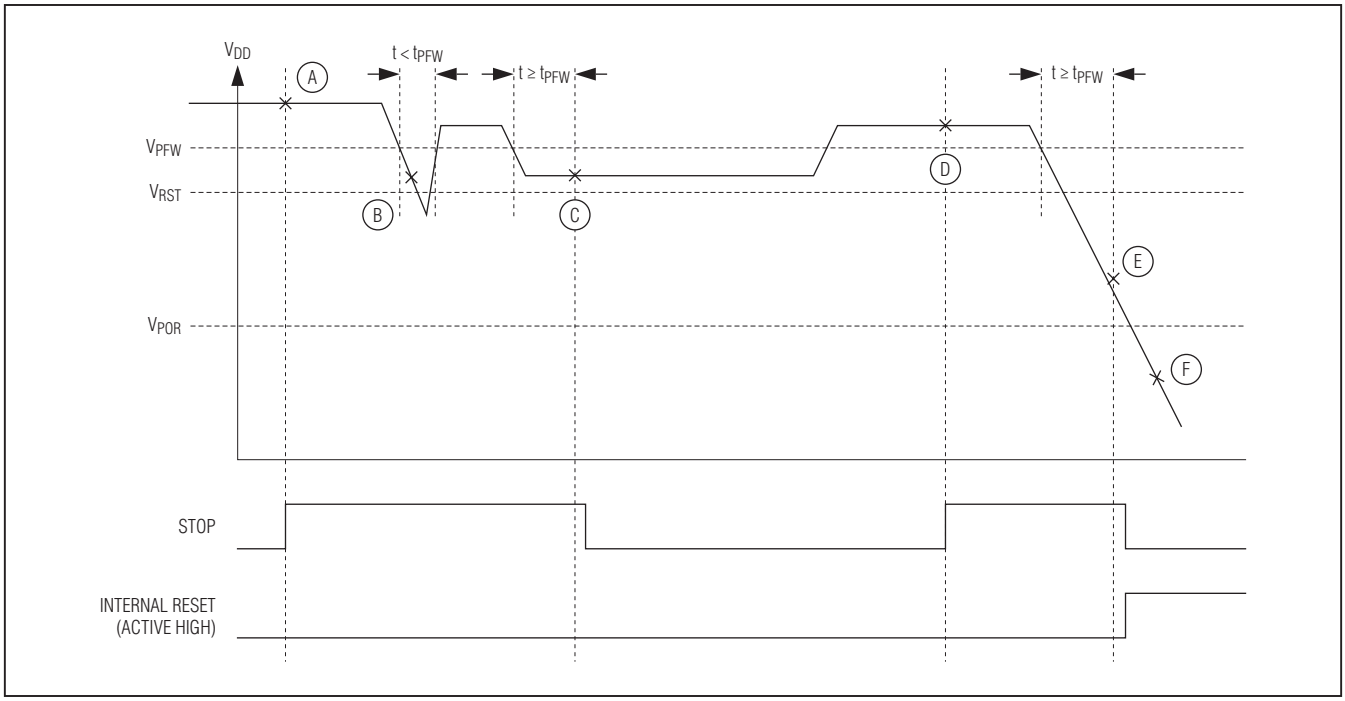


Figure 6. Stop Mode Power-Fail Detection States with Power-Fail Monitor Enabled

Table 6. Stop Mode Power-Fail Detection States with Power-Fail Monitor Enabled

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	On	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
B	On	Off	Off	Yes	Power drop too short. Power-fail not detected.
C	On	On	On	Yes	$V_{RST} < V_{DD} < V_{PFW}$. Power-fail warning detected. Turn on regulator and crystal. Crystal warmup time, t_{XTAL_RDY}. Exit stop mode.
D	On	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
E	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. Power-fail detected. CPU goes into reset. Power-fail monitor turns on periodically.
F	Off	Off	Off	—	$V_{DD} < V_{POR}$. Device held in reset. No operation allowed.

Table 7. Stop Mode Power-Fail Detection States with Power-Fail Monitor Disabled (continued)

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
D	Off	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
E	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. An interrupt occurs that causes the CPU to exit stop mode. Power-fail monitor is turned on, detects a power-fail, and puts CPU in reset. Power-fail monitor is turned on periodically.
F	Off	Off	Off	—	$V_{DD} < V_{POR}$. Device held in reset. No operation allowed.

Applications Information

The low-power, high-performance RISC architecture of this device makes it an excellent fit for many portable or battery-powered applications. It is ideally suited for applications such as universal remote controls that require the cost-effective integration of IR transmit/receive capability.

Grounds and Bypassing

Careful PCB layout significantly minimizes system-level digital noise that could interact with the microcontroller or peripheral components. The use of multilayer boards is essential to allow the use of dedicated power planes. The area under any digital components should be a continuous ground plane if possible. Keep bypass capacitor leads short for best noise rejection and place the capacitors as close to the leads of the devices as possible.

CMOS design guidelines for any semiconductor require that no pin be taken above V_{DD} or below GND. Violation of this guideline can result in a hard failure (damage to the silicon inside the device) or a soft failure (unintentional modification of memory contents). Voltage spikes above or below the device's absolute maximum ratings can potentially cause a devastating IC latchup.

Microcontrollers commonly experience negative voltage spikes through either their power pins or general-purpose I/O pins. Negative voltage spikes on power pins are especially problematic as they directly couple to the internal power buses. Devices such as keypads can conduct electrostatic discharges directly into the microcontroller and seriously damage the device. System designers must protect components against these transients that can corrupt system memory.

Additional Documentation

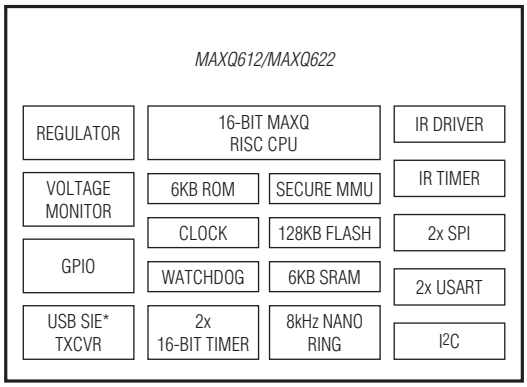
Designers must have the following documents to fully use all the features of this device. This data sheet contains pin descriptions, feature overviews, and electrical specifications. Errata sheets contain deviations from published specifications. The user's guides offer detailed information about device features and operation. The following documents can be downloaded from **www.maximintegrated.com/microcontrollers**.

- This MAXQ612/MAXQ622 data sheet, which contains electrical/timing specifications and pin descriptions.
- The MAXQ612/MAXQ622 revision-specific errata sheet (**www.maximintegrated.com/errata**).
- The *MAXQ622 User's Guide*, which contains detailed information on features and operation, including programming.

MAXQ612/MAXQ622

16-Bit Microcontrollers with Infrared Module and Optional USB

Block Diagram



Development and Technical Support

Maxim and third-party suppliers provide a variety of highly versatile, affordably priced development tools for this microcontroller, including the following:

- Compilers
- In-circuit emulators
- Integrated Development Environments (IDEs)
- JTAG-to-serial converters for programming and debugging

A partial list of development tool vendors can be found at **www.maximintegrated.com/MAXQ_tools**.

For technical support, go to **https://support.maximintegrated.com/micro**.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
64 LQFP	C64+5	21-0083	90-0141
44 TQFN-EP	T4477+2	21-0144	90-0127

Ordering Information/Selector Guide

PART	TEMP RANGE	OPERATING VOLTAGE (V)	PROGRAM MEMORY (KB)	DATA MEMORY (KB)	USB FULL SPEED	PIN-PACKAGE
MAXQ612J-0000+	0°C to +70°C	1.7 to 3.6	128 Flash	6	No	44 TQFN-EP*
MAXQ612G-0000+	0°C to +70°C	1.7 to 3.6	128 Flash	6	No	64 LQFP
MAXQ622G-0000+	0°C to +70°C	1.7 to 3.6	128 Flash	6	Yes	64 LQFP

Note: *The 4-digit suffix "-0000" indicates a microcontroller in the default state with the flash memory unprogrammed. Any value other than 0000 indicates a device preprogrammed at Maxim with proprietary customer-supplied software. For more information on factory preprogramming of these devices, contact Maxim at https://support.maximintegrated.com/micro. Information on masked ROM devices and bare die versions for most of these devices are available. Contact the factory for availability.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/10	Initial release	—
1	5/10	Changed the V_{DDIOH} spec for I_{OH} from I_{OH} = 20mA to I_{OH} = 10mA in the *Recommended Operating Conditions* table	5
2	5/11	Added the *Pin Descriptions—Bare Die* table	18–21